The relative permittivity of the ferroelectric film decreases and hence affects the dielectric resonator electric field and changes the resonant frequency.

The TE_010 mode was examined at room temperature using a vector network analyser HP8720C (Hewlett-Packard (Now Agilent), Palo Alto, CA, USA, with 1Hz resolution).

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References

Low power, high speed, charge recycling CMOS threshold logic gate

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A new implementation of a threshold gate based on a capacitive input, charge recycling differential sense amplifier latch is presented. Simulation results indicate that the proposed structure has very low power dissipation and high operating speed, as well as robustness under process, temperature and supply voltage variations, and is therefore highly suitable as an element in digital integrated circuit design.

Introduction: As the demand for higher performance, very large scale integration processors with increased sophistication grows, continuing research is focused on improving the performance, area efficiency, and functionality of the arithmetic and other units contained therein. Low power dissipation has become a major issue demanded by the high performance processor market to meet the high density requirements of advanced VLSI processors. The importance of low power is also evident in portable and aerospace applications, and is related to issues of reliability, packaging, cooling and cost.

Threshold logic (TL) was first introduced over four decades ago, and over the years has promised much in terms of reduced logic depth and gate count compared to traditional AND-OR-NOT (AON) logic-gate based design. However, lack of efficient physical realisations has meant that TL has, until recently, had little impact on VLSI. Efficient TL gate realisations have recently become available, and a number of applications based on TL gates have demonstrated its ability to achieve high operating speed and significantly reduced area [1].

Both static and dynamic TL gate implementations have been devised. Purely static gates such as neuron-MOS suffer from lim-
functions can be realised by a threshold gate network of depth at
vated after the delay of the enable inverters and an,iplifies the dif-
ipation, and some require multiple clock phases [I, 2], introducing
ited Fan in [1], typically less than 12 inputs. In addition, some of
the existing dynamic gates have relatively high static power dissi-
pation, and some require multiple clock phases [1, 2], introducing
the drawbacks associated with clock signal routing cost, clock
skew and clock power dissipation. Although the dynamic
approach proposed in [3] dissipates no static power, it will be
shown that its dynamic power dissipation is comparable to the
total power dissipation of other existing approaches.

In this Letter we propose a new realisation for CMOS threshold
gates which operates on a single phase clock, is capable of high-
speed operation, is suitable for high fan-in gate implementation
and has a very low overall power dissipation.

Threshold logic: A threshold logic gate is functionally similar to a
hard limiting neuron. The gate takes n binary inputs $X_1, X_2, ..., X_n$
and produces a single binary output $Y$. A linear weighted sum of
the binary inputs is computed followed by a thresholding operation.
The Boolean function computed by such a gate is called a threshold
function and it is specified by the gate threshold $T$ and the
weights $w_1, w_2, ..., w_n$, where $w_i$ is the weight corresponding to
the $i$th input variable $X_i$ [4]. The output $Y$ is 1 if $\sum w_i X_i \geq T$; and
0 otherwise. Any threshold function may be computed with posi-
tive integral weights and a positive real threshold, and all Boolean
functions can be realised by a threshold gate network of depth at
most two [4]. A TL gate can be programmed to realise many distin-
gt Boolean functions by adjusting the threshold $T$. For example,
an n-input TL gate with $T = n$ will realise an n-input AND gate
and by setting $T = n/2$, the gate computes a majority function.

Charge recycling threshold logic (CRTL): Fig. 1 shows the pro-
posed circuit structure for implementing a threshold gate with posi-
tive weights and threshold. It is based on the charge recycling
asynchronous sense differential logic (ASDL) developed by Rui-
Sun et al. [5]. The main element is the sense amplifier (cross-cou-
pled transistors M1-M4) which generates output $Y$ and its com-
plement $\bar{Y}$. Precharge and evaluate is specified by the dual enable
clock signals $E$ and its complement $\bar{E}$. The inputs $X_i$ are capaci-
tively coupled onto the floating gate $\phi$ of M5 and the threshold $T$
set by the gate voltage $V$ of M6. The potential $\phi$ is given by
$\phi = \sum w_i X_i / C_{\text{tot}}$, where $C_{\text{tot}}$ is the sum of all capacitances, including
parasitics, at the floating node. Weight values are thus realised by
setting capacitors $C_i$ to appropriate values. Typically, these capac-
itors are implemented between the polysilicon 1 and polysilicon 2
layers, although alternatives, such as trench capacitors available in
DRAM processes, may obviously also be used.

The ASDL comparator architecture from which the proposed
CRTL gate is derived implements high performance, energy effi-
cient operation by recycling charge which has already been drawn
from the supply. The enable signal $E$ controls the precharge and
activation of the sense circuit. Transistors M8 and M9 equalise
the outputs. The logic gate has two phases of operation, the evalu-
ate phase and the equalise phase. When $E$ is high the output voltages
are equalised. When $E$ is high, the outputs are disconnected and
the differential circuit (M5-M7) draws different currents from the
formerly equalised nodes $Y$ and $\bar{Y}$. The sense amplifier is acti-
ated after the delay of the enable inverters and amplifies the dif-
ference in potential now present between $Y$ and $\bar{Y}$, accelerating
the transition. In this way the circuit structure evaluates if the
weighted sum of the inputs, $\phi$, is greater or less than the threshold
$T$, and a TL gate is realised.

To ensure reliable operation, the gate layout must be symetri-
ical to minimise the transistor mismatches and interconnects must
be of similar length and width to eliminate interconnect-related
mismatch. The delay of the enable inverter needs to be sufficiently
large so that the output nodes have sufficient voltage difference at
the start of sensing.
To ensure correct behaviour under process and operating point variations, the proposed gate was tested at 45 corners ($V_{dd}$ at 2, 2.5, and 3 V, process Slow-Slow, Slow-Fast, Fast-Slow, and Typical-Typical, and temperature at -25, 75 and 125°C). Fig. 3 shows the transient waveform results from the HSPICE simulation for the 2-V typical-75°C corner at 300 MHz. Simulation results of the 20-input majority gate also indicate that the CRTL gate can operate even at frequencies over 400 MHz with low power dissipation (below 400 mW) under worst case conditions ($V_{dd}$ = 2 V, 125°C, Slow-Slow transistor corner).

Conclusions: A new CMOS threshold-logic gate has been proposed. A 20-input majority gate has been designed and simulated using the proposed CRTL structure to demonstrate its operation. A comparison with other TL realisations shows that this threshold gate has lower power dissipation. The gate is able to operate at clock frequencies of over 400 MHz, and its robust under process, supply voltage and temperature variations.

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References


Effects of temperature on dispersion of high slope dispersion compensating fibres

V.M. Schneider

Several experimental high dispersion and dispersion slope fibres are measured for their temperature dependence. Supemode resonant coupling is responsible for an interesting trend in the dispersion and dispersion slope variation with temperature.

Introduction: The rapid development of the optical layer network and the increase in system transmission rates imposes serious restrictions for residual chromatic dispersion in the optical link. One of the best approaches to minimise the penalty by dispersion for a large bandwidth of wavelengths is the use of dispersion-compensating fibres. It is known that very high dispersion values can be achieved by supermode coupling in planar waveguides [1]. The same principle can be used to explain the high chromatic dispersion achieved in coaxial-like fibres [2] and the sensitivity of these profiles to macro-bending [3]. Recently, chromatic dispersion measurements, for a range of different class of fibres that are not exclusively dispersion-compensating fibres, showed an interesting trend [4]. It was found that an increase in the temperature dependence of the chromatic dispersion was related to the dispersion slope of the fibre. However, most of the fibres measured did not have very large dispersion and dispersion slope values, unlike those typically governed by supermode coupling.

In this Letter, several experimental fibres that presented high dispersion and dispersion slopes based on supermode resonance are measured, and the results are discussed. It is shown that the thermal characteristics of this class of fibres can vary widely, even when there is only a small change in the profile.

Fig. 1 Measured dispersion against wavelength at different temperatures for coaxial-like fibre

![Graph showing dispersion against wavelength](image)

Origin of the effect: A simple approach to analyse the dispersion characteristics of a fibre with a coaxial structure, such as the dispersion compensating fibres, is the use of supermode theory. In this case, the coaxial fibre is broken into two individual guides, the core and the ring guide. This is the analogy in cylindrical co-ordinates to a simple directional coupler in rectangular co-ordinates. A coupling coefficient $\kappa$ is assumed between the core and the ring, as well as a dephasing term.

Since these individual guides have different group velocities and dispersion characteristics, the coupled system usually experiences a phenomenal increase in negative dispersion for the antisymmetric supermode. This happens near the critical resonant wavelength $\lambda_c$, where the dephasing is null, leading to resonant coupling. Very high negative dispersion and dispersion slope values can be achieved by careful design for appropriate coupling coefficients $\kappa$, group velocities differences, and resonant wavelength. For the fibres shown here, the theoretical $\lambda_c$ was in the range of 1600 to 1700 nm.

However, due to this same resonant nature of the coupling, any small shift mainly in $\lambda_c$, or secondarily in the previously mentioned parameters, that are all a function of the chosen designed profile, will lead to considerable shifts in dispersion values. This can be observed in Fig. 1, for an experimental fibre with a minor plot showing the typical shape around $\lambda_c$, where large dispersion changes arise from temperature variations with typical operating ranges. Percentage variations of dispersion or dispersion slope related to ambient temperature at a certain wavelength can be calculated using

$$D(\%) = \left[ \frac{D(55°C) - D(25°C)}{D(25°C)} \right] \times 100$$

This effect near $\lambda_c$ is a major direct consequence of the changes in waveguide dispersion of the coupled system, and not in the minor material dispersion variation around the zero dispersion wavelength $\lambda_c$ [4].

Experimental setup and results: To confirm this hypothesis, a number of experimental coaxial-like fibres with different profiles and reasonably high dispersion values per kilometre were chosen. The samples were allocated in a thermal chamber and dispersion measurements taken at the temperatures of -5, 25 and 55°C. A