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A novel topology for grounded-to-floating resistor conversion in CMOS technology

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Abstract

A new circuit topology to convert grounded resistors to an equivalent floating resistor is presented and discussed. The value of the resulting floating resistor equals the sum of the two grounded resistors. The new topology can be used to convert either passive, active grounded resistors or active grounded conductances. The new topology is used in the design of a current controlled very high value floating resistor in the range of GΩ. This was achieved by utilising the output conductance of two matched transistors operating in the subthreshold region and biased using a 500 nA current. The practicality of the new topology is demonstrated through the design of a very low frequency bandpass filter for artificial insect vision and pacemaker applications. Simulations results using Level 49 model parameters in HSPICE show an introduced total harmonic distortion of less than 0.25% for a 1 V_{pp} input signal in a 3.3 V 0.25 μm CMOS technology. Statistical modelling of the new topology is also presented and discussed.

Keywords: Active floating resistors; Very low frequency BP filter; Low frequency differentiator; Artificial insect vision; Pacemaker

1. Introduction

Resistors and transconductors have a very important role in a wide variety of applications such as signal processing and neural networks, which rely heavily on the design of analog VLSI circuits. Due to the large area penalty of using passive resistors, wide spread, lack of accuracy and programmability [1,2], a large number of implementations of active resistors and transconductors using MOS transistors have been discussed in literature [3–11]. Some of these techniques exploit the MOS transistor characteristic in the triode [2,12,13], saturation regions [2] and few exploit the subthreshold region of operation [14,15]. The new topology can be used to obtain low-power high-value floating resistors with high linearity and wide dynamic range.

Section 2 of this paper presents and discusses the theoretical background and the implementation of the new circuit topology in standard CMOS technologies. Section 3 demonstrates the use of the new topology in converting voltage controlled grounded resistors to a voltage controlled floating resistor. Section 4 discusses the use of the new topology in the design of a current controlled very high value floating (VHVF) resistor. Section 5 presents and discusses statistical modelling of the new topology using passive resistors. Section 6 presents a practical example of using the new current controlled very high value resistor in the design of a current controlled differentiator circuit, which has practical use in artificial insect vision [16] and pacemaker applications.

In the following analysis it is assumed that the source and the back gate for the corresponding n and p type MOS transistors are connected together, unless mentioned otherwise.

2. A new circuit topology

2.1. Theoretical analysis

The new topology is based on two-diode connected matched transistors operating in the saturation region [17] as shown in Fig. 1. V_x and V_y are the floating resistor terminal voltages, and $I_{in} = I_{out}$ is the current passing through

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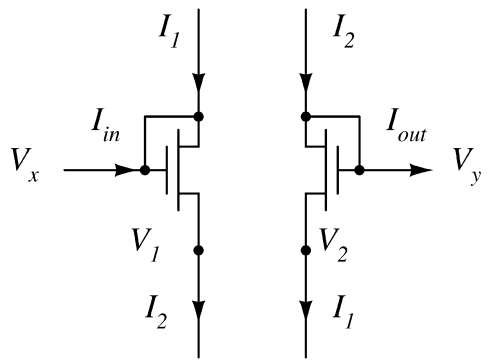

Fig. 1. The basic MOS transistor cell.

the terminals. The current equation for the transistors in Fig. 1 can be written as

$$I_1 = \frac{K}{2}(V_y - V_2 - V_{th})^2, \tag{1}$$

$$I_2 = \frac{K}{2}(V_x - V_1 - V_{th})^2, \tag{2}$$

where K is defined as $\mu_o C_{ox}(W/L)$; μ_o, the carrier mobility; C_{ox}, the oxide capacitance per unit area; V_{th}, the MOS transistor threshold voltage and W/L is the width to length ratio of the transistor. The current passing through the circuit topology can be written as

$$I_{in} = I_{out} = I_2 - I_1. \tag{3}$$

Substituting Eqs. (1) and (2) into Eq. (3), and simplifying the results, I_{out} can be written as

$$I_{out} = \frac{K}{2}[(V_x - V_y) - (V_1 - V_2)][(V_x + V_y) - (V_1 + V_2) - 2V_{th}]. \tag{4}$$

The equivalent resistance, R_{eqv}, is defined as

$$R_{eqv} = \frac{V_x - V_y}{I_{in}} = \frac{V_x - V_y}{I_{out}}. \tag{5}$$

In order to achieve a circuit topology independent of the MOS transistor threshold voltage, let

$$V_1 = V_x - V_{th} + f(V_x), \tag{6}$$

$$V_2 = V_y - V_{th} + f(V_y). \tag{7}$$

The sum and the difference of V_1 and V_2 can be written as

$$V_1 + V_2 = V_x + V_y - 2V_{th} + f(V_x) + f(V_y), \tag{8}$$

$$V_1 - V_2 = V_x - V_y + f(V_x) - f(V_y). \tag{9}$$

By substituting Eqs. (8) and (9) in Eq. (4), I_{out} can be written as

$$I_{out} = \frac{K}{2}(f(V_x)^2 - f(V_y)^2). \tag{10}$$

Eq. (10) shows that the current passing through the topology is independent of the MOS transistor threshold voltage, a square function of V_x and V_y and is proportional to K.

2.2. Topology implementation

A possible implementation of Eqs. (6) and (7), is shown in Fig. 2. In this topology the current passing through mn_1 is mirrored by mn_2 and feeds back to the V_y terminal of mn_3 using mp_1. In a similar way, the current passing through mn_3 is mirrored by mn_4 and feeds back to the V_x terminal of mn_1 using mp_3. The relation between V_x and V_1, while assuming a passive resistor connected between V_1 and ground, can be written as

$$V_1 = R(2I_2) = KR(V_x - V_1 - V_{th})^2, \tag{11}$$

where R is the resistor value. Solving Eq. (11) for V_1 gives two solutions, the feasible one is

$$V_1 = V_x - V_{th} + \frac{1 - \sqrt{1 + 2KR(V_x - V_{th})}}{2KR}. \tag{12}$$

A similar expression for V_2 can be written as

$$V_2 = V_y - V_{th} + \frac{1 - \sqrt{1 + 2KR(V_y - V_{th})}}{2KR}. \tag{13}$$

Comparing Eqs. (12) and (13) with Eqs. (6) and (7), respectively, $f(V_x)$ and $f(V_y)$ can be written as

$$f(V_x) = \frac{1 - \sqrt{X}}{2KR}, \tag{14}$$

$$f(V_y) = \frac{1 - \sqrt{Y}}{2KR}, \tag{15}$$

where

$X = 1 + 2KR(V_x - V_{th})$ and $Y = 1 + 2KR(V_y - V_{th})$.

Substituting the values of $f(V_x)$ and $f(V_y)$ from Eqs. (14) and (15) in Eq. (10), I_{out} can be written as

$$I_{out} = \frac{1}{8KR^2}[(1 - \sqrt{X})^2 - (1 - \sqrt{Y})^2]. \tag{16}$$

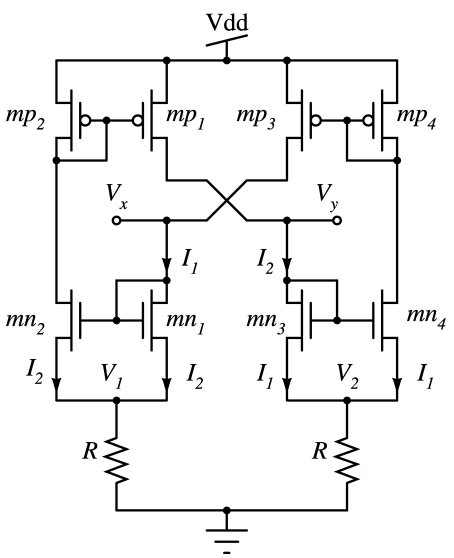

Fig. 2. The new topology with two passive resistor connected at V_1 and V_2 and ground.

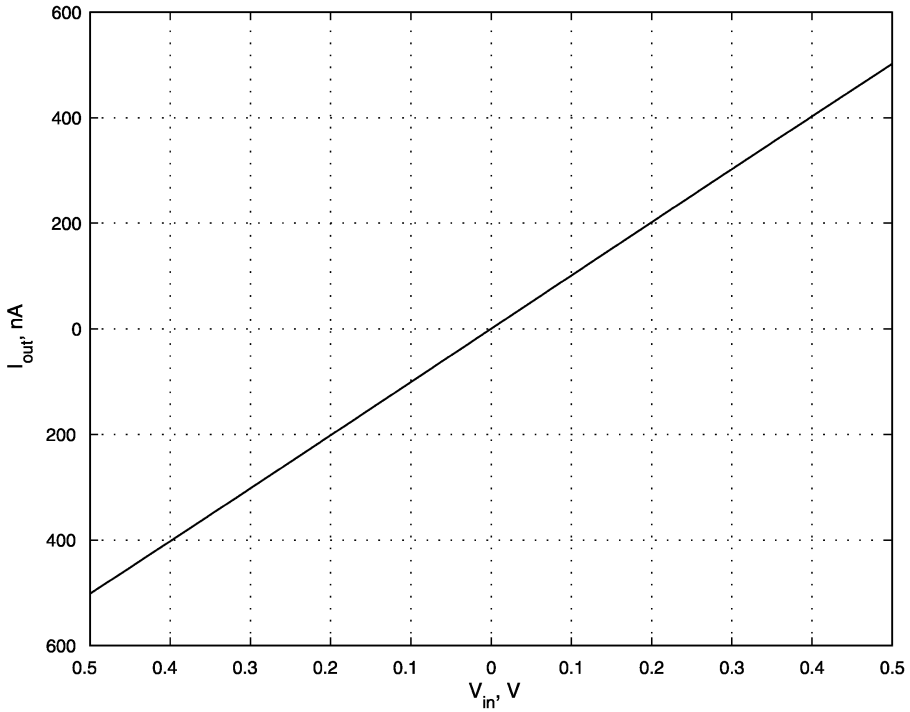

Fig. 3. The simulation results of the new circuit topology with two 1 MΩ passive resistors connected at V_1 and at V_2.

Assuming $\sqrt{X} \gg 1$ and $\sqrt{Y} \gg 1$, which is a valid assumption for large values of R, then Eq. (16) is reduced to

$$I_{\text{out}} = \frac{1}{8KR^2}(X - Y). \tag{17}$$

Substituting the values of X and Y in Eq. (17), with $V_x = V_{\text{B}} + V_{\text{in}}/2$ and $V_y = V_{\text{B}} - V_{\text{in}}/2$, Eq. (17) is reduced to

$$I_{\text{out}} = \frac{V_{\text{in}}}{2R}. \tag{18}$$

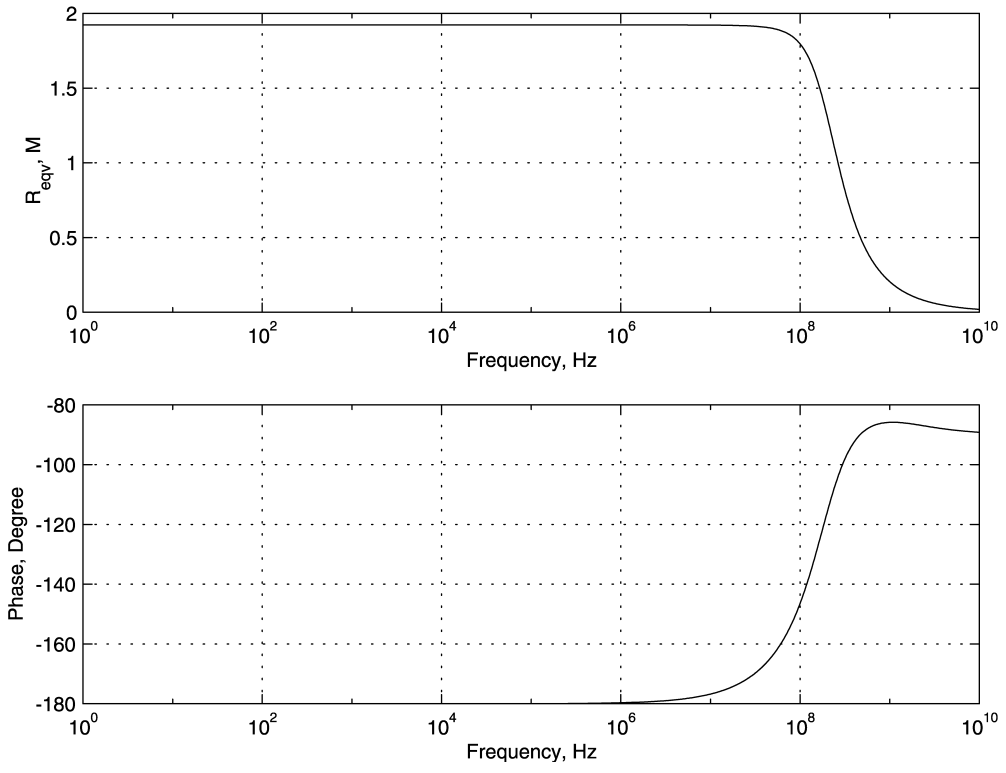

Fig. 4. The frequency response of the new circuit topology with two 1 MΩ passive resistors connected at V_1 and V_2.

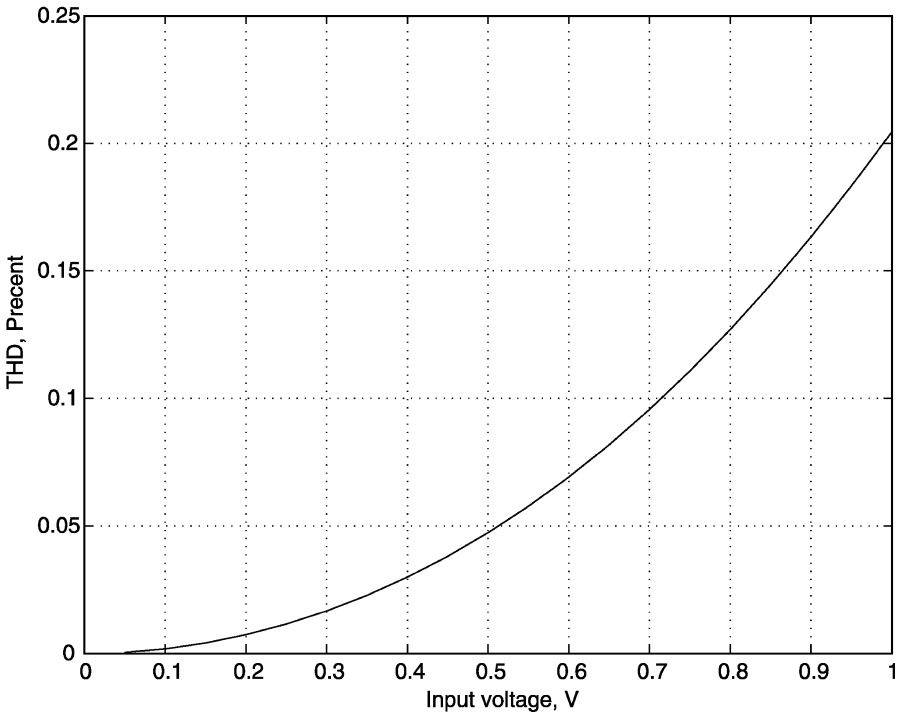

Fig. 5. THD introduced by the new circuit topology as function of the input signal amplitude.

An expression for the equivalent resistance R_{eqv} can be written by substituting Eq. (18) into Eq. (5), as given by

$$R_{eqv} = \frac{V_{in}}{I_{out}} = 2R. \tag{19}$$

Eq. (19) shows that the equivalent floating resistor value is independent of the process model parameters and the threshold voltage of the MOS transistor. Eq. (19) also shows that the V–I relation of this topology resembles an ideal resistor with an equivalent floating resistor equal to the sum of the grounded resistors.

The circuit shown in Fig. 2 was simulated with the length and width of all transistor sizes are set to 12 μm as shown in Fig. 3. These simulations were conducted using HSPICE simulator with Level 49 process model parameters for 0.25 μm single poly, 5 metal n-well process. The simulated I–V characteristics with passive input resistors show a very wide dynamic range and very linear characteristics. The frequency response of the topology using passive resistors is shown in Fig. 4. The AC simulations show a frequency response that extends to the MHz range with constant resistance value. The introduced total harmonic distortion (THD) by the new topology for 1 V_{pp} input signal is less than 0.25% as shown in Fig. 5.

3. Converting a grounded resistor to a floating resistor

The analysis presented in Section 2 is still also valid when the passive resistors are replaced by active grounded resistors or conductances. As an example, the grounded resistor [18] shown in Fig. 6 is used. This grounded resistor was chosen because of its simplicity, very high linearity and controllability. Other grounded resistors such as the ones described in Refs. [6,19] can also be used.

The resistor shown in Fig. 6 was simulated using the previously mentioned technology, with $W_1/L_1 = 48$ μm/6 μm and $W_2/L_2 = 6$ μm/48 μm. The control voltage V_c was swept from 1 to 3.5 V in a 0.5 V step, while V_0 was swept from 0 to 5 V for every V_c, as shown in Fig. 7. The resistor shown in Fig. 6, was integrated in the new topology as shown in Fig. 8, and simulated with all transistor sizes in the topology and the grounded resistors are kept as before. The simulation results for the new

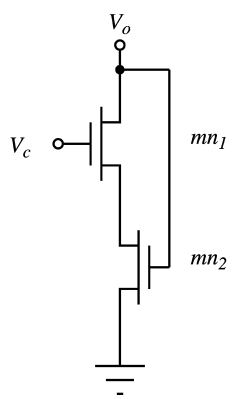

Fig. 6. A very linear grounded resistor.

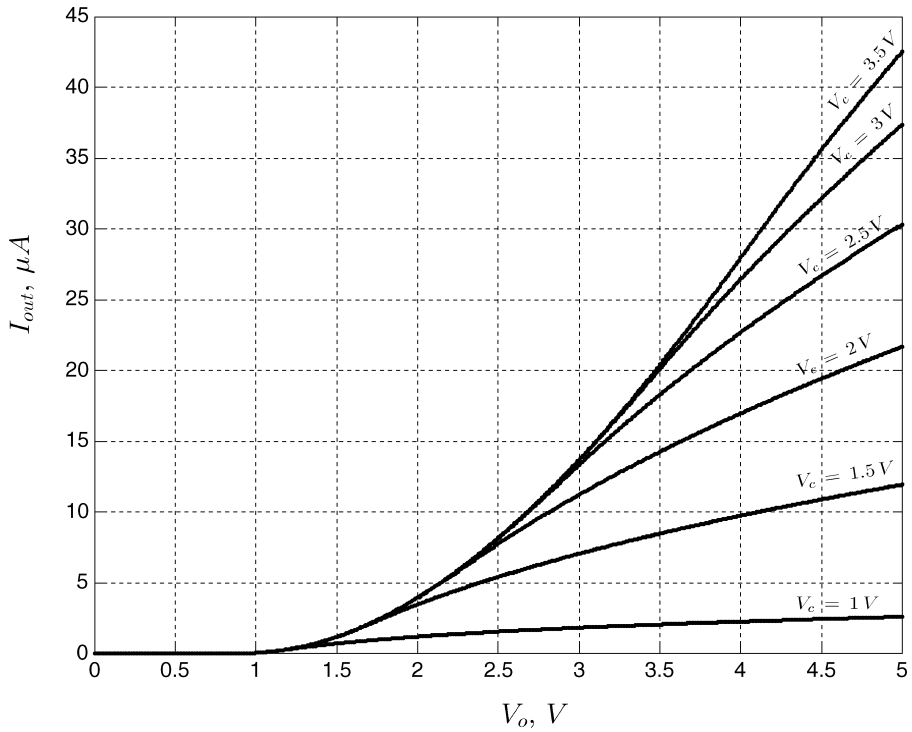

Fig. 7. Simulation results of the grounded resistor shown in Fig. 6 with the control voltage V_c swept from 1 to 3.5 V in a 0.5 V step.

floating resistor are shown in Fig. 9. The figure shows that the resultant voltage controlled floating resistor is also very linear.

4. Very high value floating resistor

A VHVF resistor can be designed using the previous topology if starting with very high value resistors or output conductances. To demonstrate the technique with a high output conductance configuration, the output conductance of the MOS transistor in the saturation region is used as shown in Fig. 10. A MOS transistor biased with small value current provides a very high output conductance in the range of GΩ. The main concern about using the MOS transistor output conductance is that it depends on the channel length modulation parameter λ, which is defined [20] as

$$\lambda = \frac{\sqrt{\dfrac{\varepsilon_{si}}{qN_{eff}(V_{DS} - V_{Dsat})}}}{L}, \tag{20}$$

where drain saturation voltage V_{Dsat} is defined as $V_{gs} - V_{th}$, ε_{si} is the dielectric constant of silicon, N_{eff} is the substrate doping density, q is the electron charge, V_{DS} is the drain to source voltage and L is the transistor length. From Eq. (20), it is clear that λ is a process dependent parameter and it is not a favourable parameter to use in circuit design. However, such dependence does not exclude λ as a design parameter [21], and in this case the dependence on λ can be compensated for by the current programmability of the VHVF resistor. Furthermore, other high output conductance current configuration can be used instead of the two transistor current mirrors. Using the simple transistor model that includes the channel length modulation effect, the output conductances, g_d of mn_5 or mn_6 at constant gate

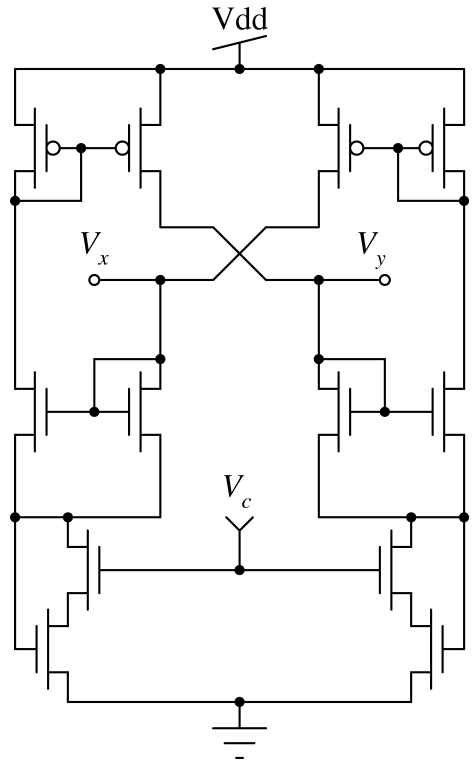

Fig. 8. A voltage controlled floating resistor generated by replacing the passive resistors in Fig. 2 with two matched voltage controlled grounded resistors.

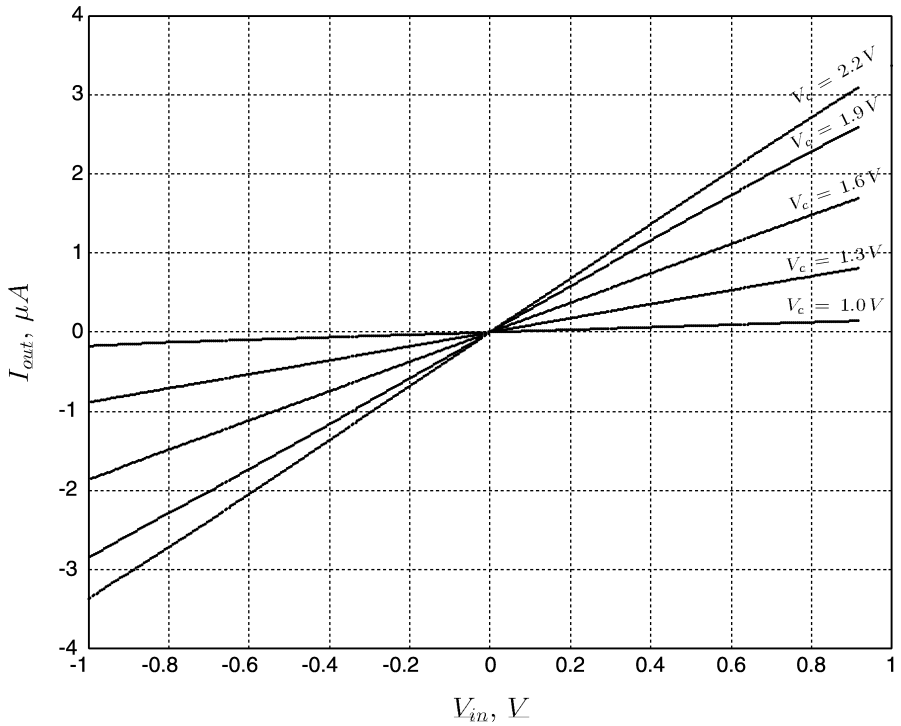

Fig. 9. Simulation results of the new voltage controlled floating resistor shown in Fig. 8 with the control voltage V_c was swept from 1 to 2.2 V in a 0.3 V step.

to source voltage is given by

$$g_d = \frac{\lambda I_d}{(1 + \lambda V_{ds})} \simeq \lambda I_d. \quad (21)$$

For an $I_d = 1\ \mu A$ and $\lambda = 1\ mV^{-1}$ (extracted from the Level 49 model parameters at 1 μA bias current), the equivalent floating resistor is 2 GΩ.

The circuit shown in Fig. 10 was simulated using a large value of reference current in the μA range, to demonstrate the circuit performance when transistors are operating in the saturation region. The simulation results, with the reference current I_0 was swept from 7.5 to 20 μA in a 2.5 μA step, are shown in Fig. 11. The circuit shown in Fig. 10 was resimulated using a small bias current in the nA range, to ensure that all transistors are operating in the subthreshold region of operation. The simulation results, with I_0 was swept from 500 nA to 1 μA in a 100 nA step, are shown in Fig. 12. Figs. 11 and 12 show that the resistor exhibits very linear characteristics in saturation and subthreshold regions of operation. The frequency response of the very high value resistor is shown in Fig. 13. The simulations show that the bandwidth of the active floating resistor is reduced compared to the passive floating resistor case presented earlier with constant resistance. The reduction significance is application dependence. For the targeted applications the bandwidth is still within the operational frequency range.

5. Statistical modelling

To evaluate the performance of the circuit topology discussed in Section 2 Monte Carlo analysis was performed. This analysis provides an insight into the topology sensitivity to process parameters. This section addresses issues related to (i) threshold voltage mismatch effect on the resultant equivalent floating resistor, (ii) transistor dimension effect on the equivalent resistor value. These effects are evaluated using Level 49 model parameters

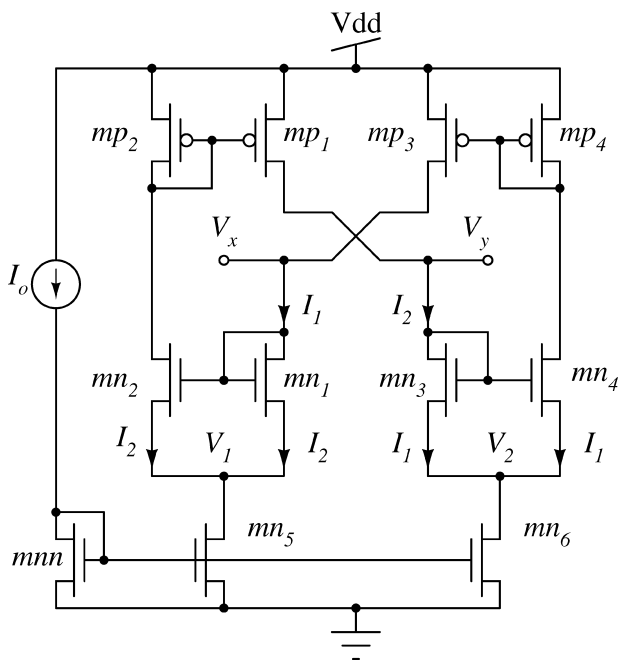

Fig. 10. A very high value current controlled floating resistor that uses output conductance of MOS transistor operating in the saturation region of operation.

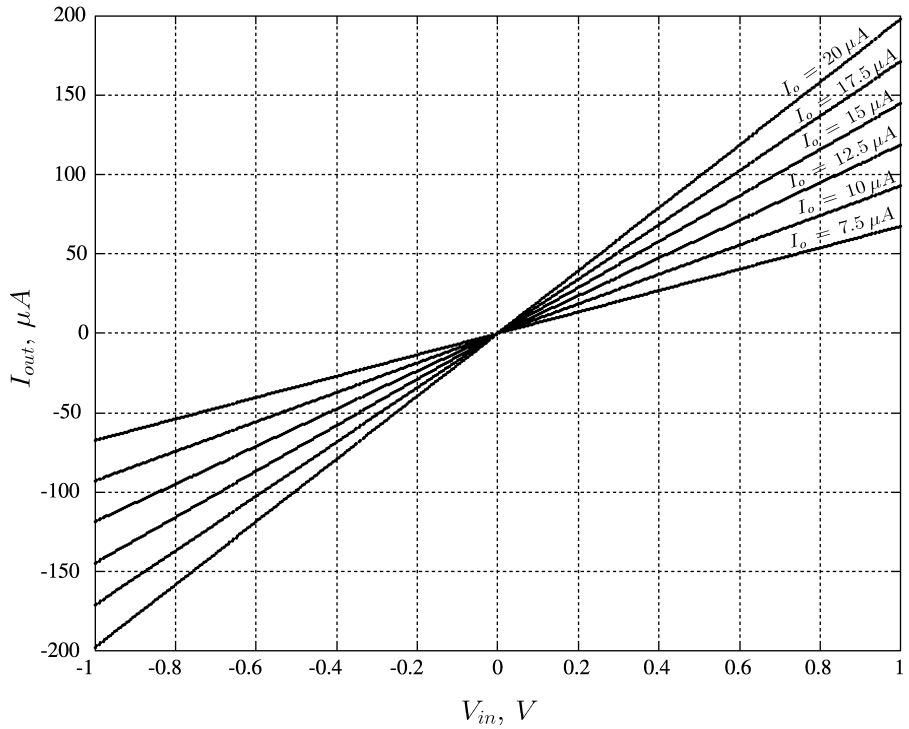

Fig. 11. The simulation results of the current controlled VHVF resistor with the reference current I_0 swept from 7.5 to 20 μA in 2.5 μA step.

for an industrial 0.25 μm CMOS process. In the following simulations passive resistors are used as input for the topology.

Monte Carlo analysis in HSPICE simulator is used to show the effect of threshold voltage mismatch on the resistor value. The simulation was conducted by adding a small voltage to the threshold voltage calculated by the simulator. A Gaussian distribution with zero mean and a 5-mV standard deviation was used. The 5 mV value was chosen based on the relation between

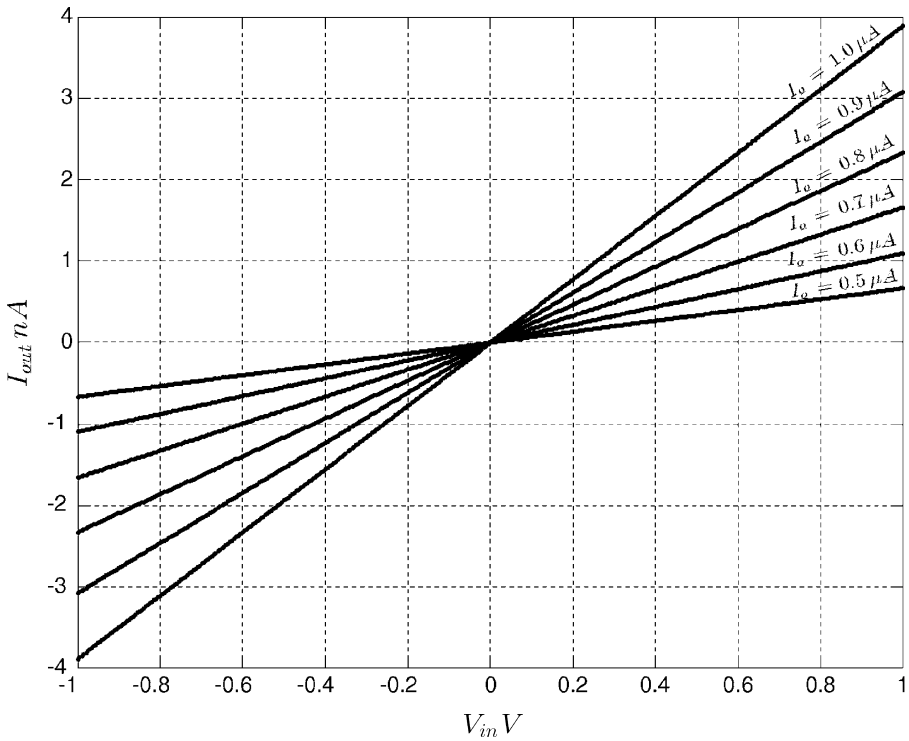

Fig. 12. The simulation results of the VHVF resistor with the reference current I_0 swept from 500 nA to 1 μA in a 200 nA step.

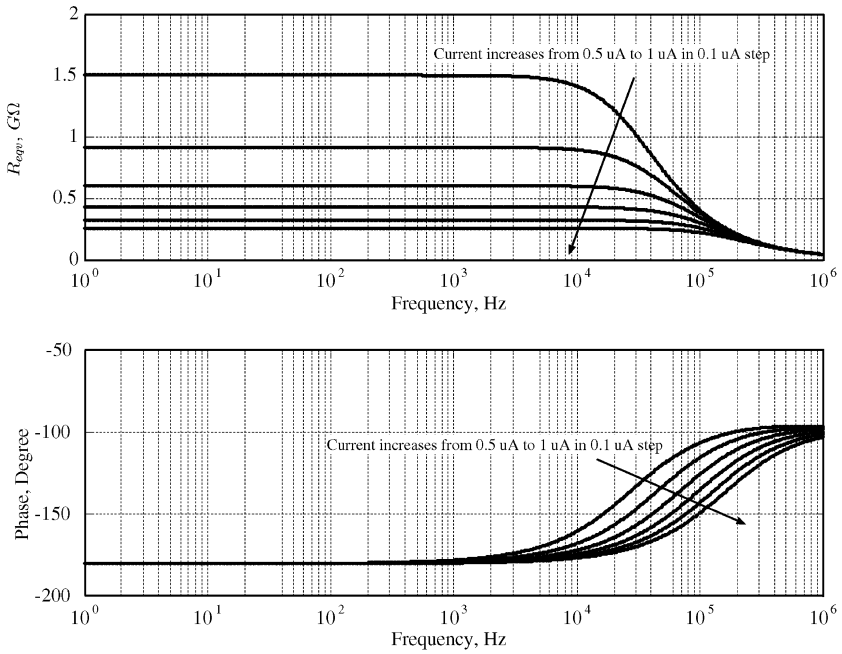

Fig. 13. The frequency response of the VHVF resistor with the reference current I_0 swept from 500 nA to 1 μA in a 200 nA step.

transistors area and threshold voltage mismatch measurements given in Ref. [22]. Two 1 MΩ passive resistors were used as input for the topology. All the transistors width and lengths were set to 4 μm. Fig. 14 shows the equivalent floating resistor value for each iteration of Monte Carlo analysis. The measured mean value of the equivalent floating resistor is 1.9709 MΩ and the standard deviation is 98 kΩ. The programmability of the resistor can be used to fine tune the resistor value.

Fig. 15 shows the effect of sizes of the transistors on the effective value of the floating resistor. Two 1 MΩ resistors are used as inputs for the topology and

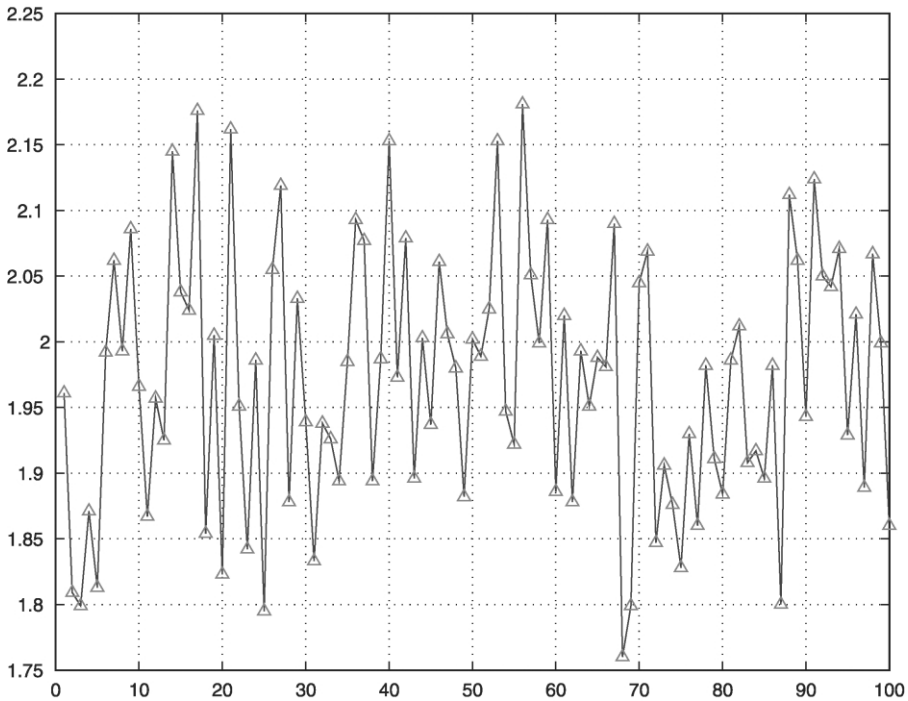

Fig. 14. Monte Carlo analysis of the new circuit topology shown in Fig. 2. These simulations show equivalent floating resistor value as a result of threshold voltage mismatch for each Monte Carlo iteration.

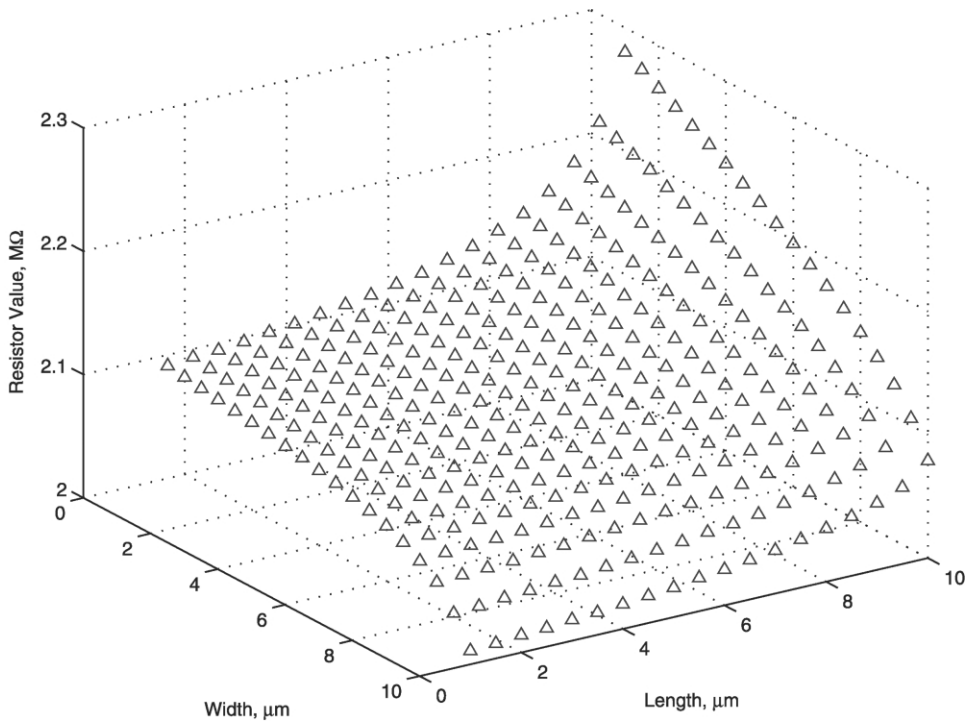

Fig. 15. The effect of the transistors width and length on the circuit topology effective floating resistance.

the width and length of all the transistors in the topology were sweeped from 1 to 10 μm in 0.5 μm step. These simulations show that the transistors sizes have an effect on the effective floating resistor value. This effect can be minimised by choosing wide transistors with moderate lengths.

6. A design example

To demonstrate the use of the new very high value resistor in a practical design example, the new topology was used in the design of a low frequency, current controlled, bandpass filter which present a major problem in motion detection systems because of the challenging requirements [17]. The bandpass filter requirements are: (i) 100 Hz bandwidth, (ii) the first cut-off frequency at 10 Hz while the second at 100 Hz, (iii) very high gain, (iv) very small area, (v) moderate to low power consumption. A bandpass filter with these requirements can be designed as shown in Fig. 16. The lower cut-off frequency of the filter is set by the differentiator configuration and upper cut-off frequency is limited by the opamp gain, which is function of the opamp bias current. The voltage at nodes V_1 and V_2 can be written as

$$V_1 = V_{\text{in}} \frac{RC\,s}{1 + RC\,s} + V_{\text{out}} \frac{1}{1 + RC\,s}, \tag{22}$$

$$V_2 = V_{\text{out}} \frac{1}{1 + RC\,s}. \tag{23}$$

The relation between the differential inputs V_1 and V_2 and V_{out} is given as

$$V_{\text{out}} = A(s)(V_2 - V_1). \tag{24}$$

Substituting Eqs. (22) and (23) in Eq. (24), the circuit transfer characteristics can be written as

$$H(s) = -A(s) \frac{RC\,s}{1 + RC\,s}, \tag{25}$$

where $A(s)$ is the operational amplifier gain.

Two versions of the differentiator shown in Fig. 16, were simulated at 5 volt supply. The first circuit uses a passive resistor, while the second uses VHVF resistors. The frequency responses of the two versions are shown in Fig. 17. In addition, the transient analysis simulation results for the two versions are shown in Fig. 18.

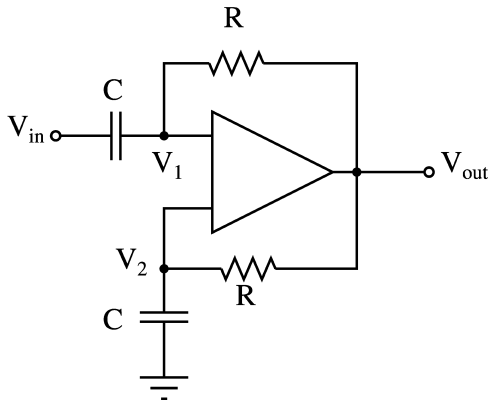

Fig. 16. A circuit diagram of a low frequency differentiator circuit.

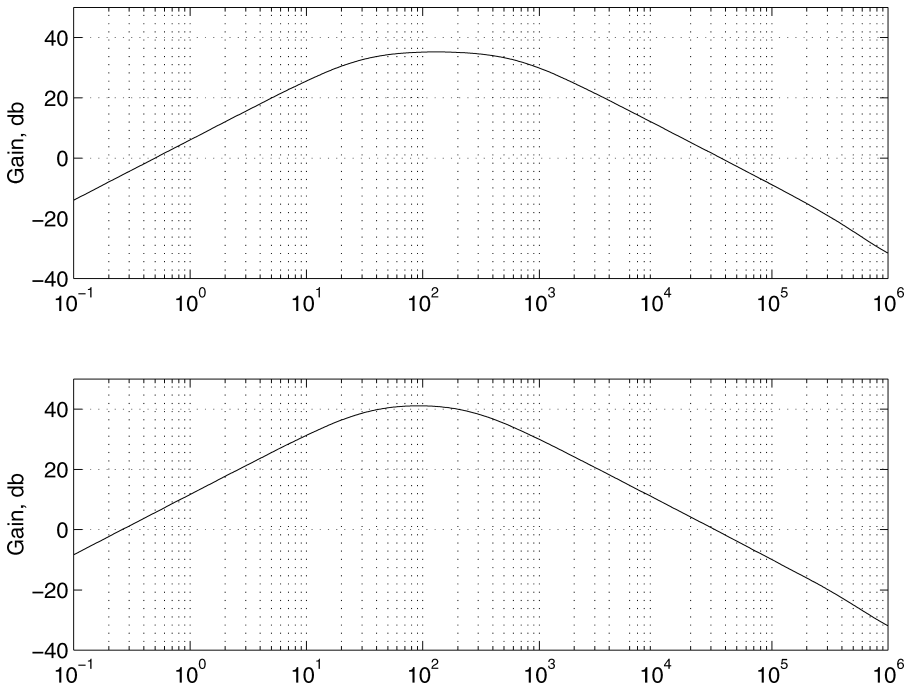

Fig. 17. The frequency response of the bandpass filter circuit using passive resistors and the current controlled very high value resistor.

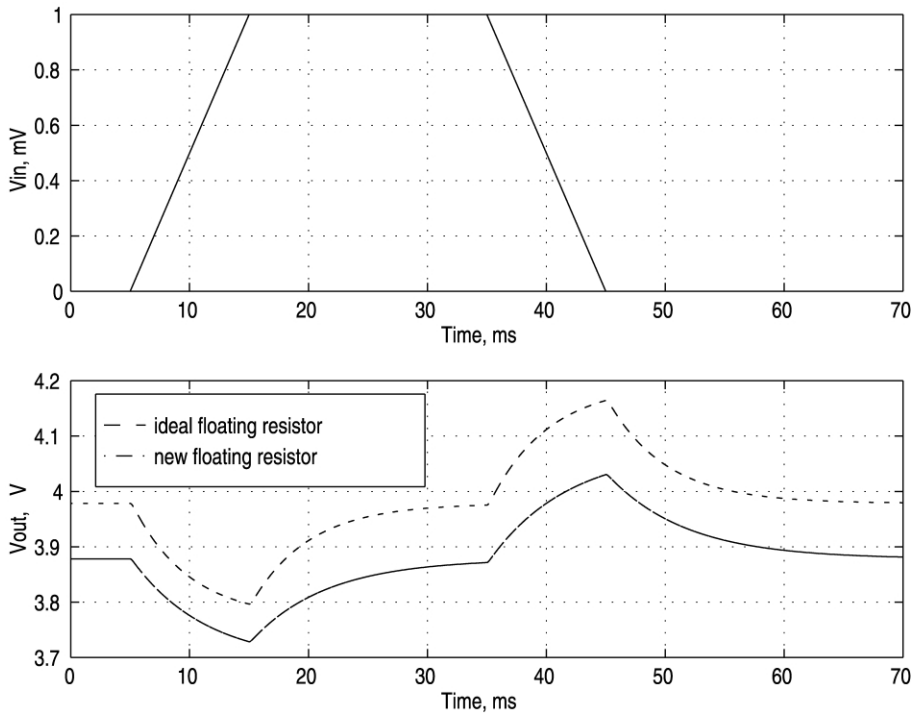

Fig. 18. The simulation results of the bandpass filter circuit for an input pulse with 10 ms raise and fall time delayed by 5 ms (upper) using an passive resistors and VHVF resistors (lower).

The difference in the simulation results between the two versions of the differentiator is due to a larger resistance value of the VHVF resistor.

7. Conclusion

A new circuit topology to convert grounded resistors to a floating resistor is presented and discussed. The use of the new topology in the conversion of passive, voltage and current controlled resistors was demonstrated in the design a current controlled very high value resistor, in GΩ the range. The floating resistor is electrically programmable, has a small number of transistors and consumes very small amount of current from the power supply. The sensitivity of the circuit against threshold voltage mismatch was

examined using Monte Carlo analysis in HSPICE. The practicality of the new resistor is demonstrated through the design of a very low frequency bandpass filter for pacemaker and artificial insect vision applications.

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