INSTITUTE OF PHYSICS PUBLISHING SMART MATERIALS AND STRUCTURES
Smart Mater. Struct. **14** (2005) 569–574 doi:10.1088/0964-1726/14/4/015

Dynamic bootstrapped shift register for smart sensor arrays

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Received 24 September 2003, in final form 27 September 2004
Published 4 May 2005
Online at stacks.iop.org/SMS/14/569

Abstract
In this paper we demonstrate the operation of a dynamic serial-to-parallel shift register, with only four transistors per stage. A bootstrap capacitor is used to overcome the problem of transistor threshold voltage drop. We will refer to this new logic family as non-ratioed bootstrap logic (NRBL). Simulation results are presented showing the operation of the shift register along with Monte Carlo analysis to demonstrate the robustness of the circuit. A key application area for this novel shift register is in the addressing and read out of high-density smart sensor arrays.

1. Introduction

The shift register is perhaps the most common structure for enabling the movement of a data bit in VLSI systems [1]. Shift registers have many applications ranging from producing time delay by using serial-in serial-out shift registers, or converting serial data to parallel data using a serial-in parallel-out shift register. Serial-in parallel-out shift registers are commonly used in image sensors to control the analogue multiplexer, which transmits data from the photodiode pixel to the A/D converter where they are then processed into an image, as shown in figure 1.

There has been recent interest in using capacitors to reduce the size of VLSI circuits [2]. Here we present a different capacitive approach to produce a very compact serial–parallel shift register. We demonstrate functionality with four transistors per stage and no DC power rails. There are a number of applications where both low power and compactness are required. These include dense optical smart sensors [3] and gate control of solid-state quantum computers [4]. A special feature of this shift register is that the output amplitude can be externally controlled by adjusting the height of the two-phase non-overlapping clock; this feature is important for these target applications.

As shown in figure 2, each stage of the low power serial-to-parallel dynamic shift register consists of four non-ratioed minimum sized n-channel transistors and can be implemented in any standard CMOS process. A bootstrapping capacitor is used to overcome the threshold voltage drop of the n-channel pass transistor. The register has no DC power supply and is driven entirely by the two-phase clock, leading to low power dissipation. The clocks should be non-overlapping, and if this requirement is not met, the register will not perform correctly [5]. Non-overlapping clocks are advantageous as fixed pattern noise (fpn), due to capacitive clock feedthrough, can be more easily controlled [6]. Power consumption and dissipation is an important parameter in modern VLSI design, as more electronic devices increasingly become portable [7]. Power consumption therefore needs to be minimized, keeping the battery size practical for portable electronic devices.

2. Operation of the shift register

With reference to figure 2, the operation of the circuit is as follows. The drain of each enable transistor is pulsed every clock period. The output of each shift element remains low until a high is enabled by the previous stage or the serial I/P. The output is charged up by the clock pulse when a high appears at the gate of the enable transistor. The output pulse does not drop, by the threshold voltage V_t of the n-transistor, due to the bootstrap action of the capacitor C_b. Moreover, C_b pulls up the enable transistor by V_{boot}, holding it at $V_{clk} + V_{boot}$,

$$V_{boot} = \frac{C_p}{C_b + C_p} V_{clk} \tag{1}$$

where C_p is the parasitic capacitance to ground at the input and V_{clk} is the clock high level. As the output is charged up to V_{clk}, $V_{clk} - V_t$ appears at the gate of the reset transistor and the following enable transistor via the pass transistor. As `Clk 1` starts going low, the output drops accordingly. When the output is $2V_t$ below V_{Clk}, the reset transistor turns on and

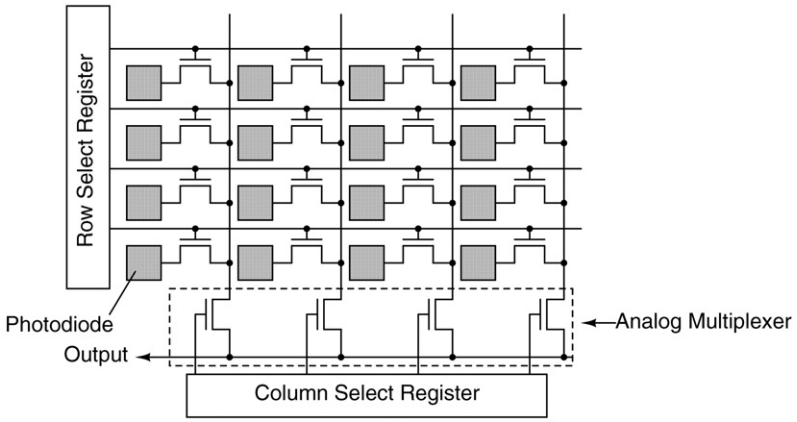

Figure 1. Photodiode array. The row select register is required to drive the gates of the photodiode address transistors on each row, therefore it has a larger load to drive than the column select register, which is only required to drive the gate of one transistor in the analogue multiplexer.

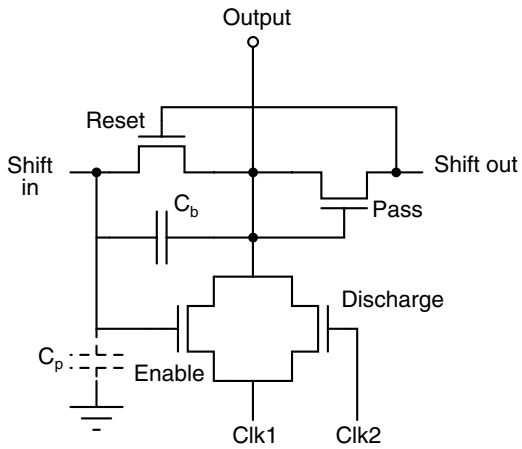

Figure 2. One stage of the shift register, with only four transistors and a capacitor C_b to provide bootstrapping action to overcome the MOSFET threshold voltage drop in the enable transistor. The register has no DC supply and is driven entirely by two non-overlapping clocks.

resets the bootstrap capacitor. This causes the enable transistor to turn off when the output is at this level. When the next clock phase comes on (`Clk 2`), the discharge transistor turns on and completes the discharge of the output. The bootstrap capacitor of the next stage is not charged as the gate of the pass transistor is now at a lower potential than its source. The same cycle repeats for the subsequent stages of the shift register. Note that the connection of the two clocks alternates between each stage of the shift register. A summary of the functions of each transistor is as follows.

- *Enable transistor:* connects clock to output when enabled by the previous stage.
- *Reset transistor:* resets the bootstrap capacitor.
- *Pass transistor:* (a) passes initial current to charge up the bootstrap capacitor of the next stage, (b) when output discharges, it turns off so that the bootstrap capacitor of the next stage does not discharge, (c) provides a threshold voltage drop so that the reset transistor is kept hard off until the output potential drops.

As the circuit is driven by the two non-overlapping clocks, to ensure the circuit functions as designed, the minimum non-overlapping period of the clocks should be equal to the fall time of the current output stage and the rise time of the following output stage. Furthermore, to ensure the circuit functions, the input pulse should be pulsed in while `Clk 2` is high, to charge the bootstrap capacitor.

3. Structure of the shift register

Each stage of the shift register is non-inverting and consists of four transistors with an extra transistor at the input and output of the shift register, as shown in figure 3. The added transistor at the input stage is required to clock the serial input pulse. The added transistor at the serial output stage is required to discharge the last bootstrap capacitor.

The layout of the shift register, shown in figure 4, displays four stages of the shift register. The two clock lines were designed with an interdigitated structure such that the contacts for both clock lines are at the same level in the layout. This symmetry is important as it balances the parasitic capacitance on the clock lines. This allows us to have the same bootstrap capacitance value for each stage and also allows easier clock buffer designs. Furthermore, if the shift register is used to address an imaging array, as in figure 1, the balanced clock lines will minimize odd/even type fixed-pattern noise on the output.

Note that the bootstrap capacitance is formed by a gate oxide layer sandwiched between poly and diffusion layers. So there is the question of which way around to place the capacitor. Figure 4 shows the poly terminal connected to the gate of the enable transistor and the diffusion terminal connected to an output stage. This orientation has two advantages: (a) it reduces the number of contact cuts by maintaining contiguous layers and (b) the diffusion is kept away from the sensitive node at the gate of the enable transistor (this is important for applications where the shift register might possibly be exposed to light).

4. Bootstrap analysis

Here we show that a first-order circuit analysis of the bootstrapped enabled transistor is fairly straightforward and

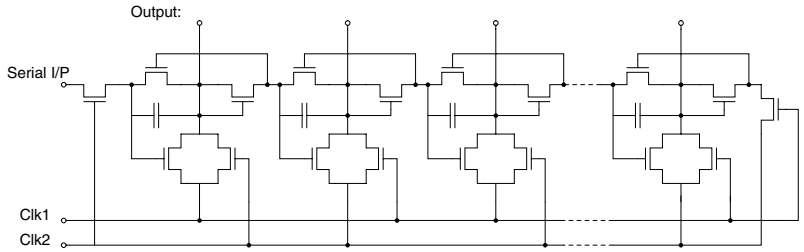

Figure 3. Multiple stages of the NRBL shift register, driven by two non-overlapping clocks. The shift register also requires two extra transistors, one before the first stage for the serial input, and one at the last stage to discharge the last bootstrap capacitance. Note the alternate clock connections between the stages.

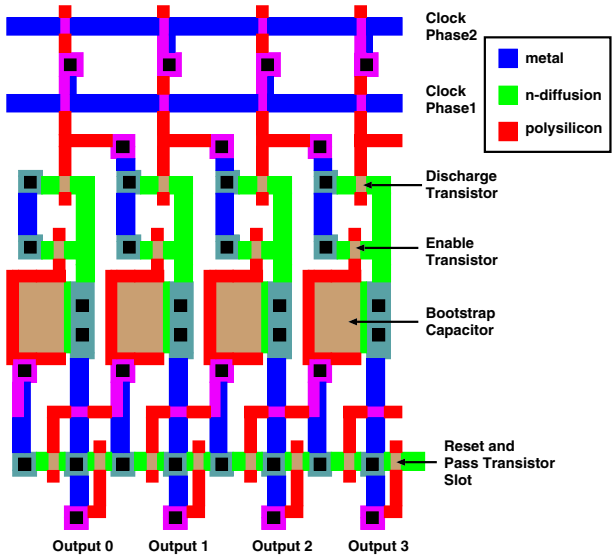

Figure 4. Layout of the dynamic shift register in a standard 0.25 μm CMOS process, where only n-channel transistors are required. Four shift stages are shown and each stage occupies a pitch of only 2.04 μm.

(This figure is in colour only in the electronic version)

roughly agrees with SPICE simulations. We begin the analysis by considering the rising clock edge in figure 5. Now,

$$V_{\mathrm{G}} = V_{\mathrm{clk}} + V_{\mathrm{boot}}$$

where $V_{\mathrm{boot}} = \eta V_{\mathrm{clk}}$ and $\eta = \frac{C_{\mathrm{p}}}{C_{\mathrm{p}}+C_{\mathrm{boot}}}$.

At $t \to \infty$, $V_{\mathrm{GS}} = V_{\mathrm{G}} - V_{\mathrm{S}} = (V_{\mathrm{clk}} + V_{\mathrm{boot}}) - V_{\mathrm{clk}} = V_{\mathrm{boot}}$. Due to the bootstrapping action, V_{S} follows V_D and so V_{DS} is small. This is maintained because η is designed such that $V_{\mathrm{boot}} \geqslant V_{\mathrm{t}}$ to keep the transistor on. As saturation is defined when $V_{DS} > (V_{\mathrm{GS}} - V_{\mathrm{t}})$, we can assume non-saturation due to the small V_{DS} and hence we must use $i_{ds} = K\{(V_{\mathrm{GS}} - V_{\mathrm{t}})V_{DS} - \frac{V_{DS}^2}{2}\}$. The circuit equations are:

$$i_{\mathrm{b}} = C_{\mathrm{p}}\dot{V}_{\mathrm{G}} \tag{2}$$

$$i_{ds} - i_{\mathrm{b}} = C_L\dot{V}_{\mathrm{S}} \tag{3}$$

$$i_{\mathrm{b}} = C_{\mathrm{boot}}(\dot{V}_{\mathrm{G}} - \dot{V}_{\mathrm{S}}). \tag{4}$$

Assuming V_{DS} is very small, we can make the following linear approximation: $g(V_{\mathrm{G}} - V_{\mathrm{S}} - V_{\mathrm{t}}) = i_{ds}$, and choose a constant $g = \frac{K \times V_{\mathrm{clk}}}{2}$.

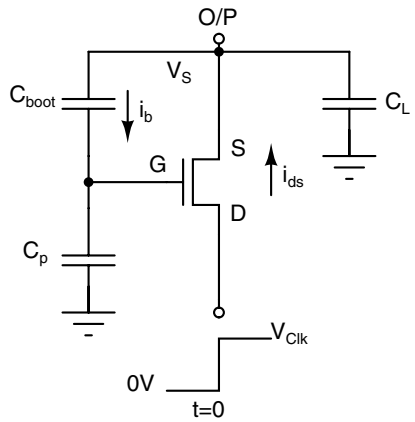

Figure 5. Circuit analysis of the enable transistor, when it receives a rising clock edge.

Equations (2) and (4) give

$$C_{\mathrm{p}}\dot{V}_{\mathrm{G}} = C_{\mathrm{boot}}(\dot{V}_{\mathrm{G}} - \dot{V}_{\mathrm{S}})$$

$$\therefore\ \dot{V}_{\mathrm{S}} = \gamma\dot{V}_{\mathrm{G}} \qquad \text{where } \gamma = 1 - \frac{C_{\mathrm{p}}}{C_{\mathrm{boot}}}.$$

Now, on substituting equation (2) and the linear approximation of i_{ds} into equation (3), we obtain $g(V_{\mathrm{G}} - V_{\mathrm{S}} - V_{\mathrm{t}}) - C_{\mathrm{p}}\dot{V}_{\mathrm{G}} = C_L\dot{V}_{\mathrm{S}}$. Then differentiating with respect to t gives $C_L\ddot{V}_{\mathrm{S}} + C_{\mathrm{p}}\ddot{V}_{\mathrm{G}} = g\dot{V}_{\mathrm{G}} - g\dot{V}_{\mathrm{S}}$. Substituting $\dot{V}_{\mathrm{S}} = \gamma\dot{V}_{\mathrm{G}}$ gives $\gamma C_L\ddot{V}_{\mathrm{G}} + C_{\mathrm{p}}\ddot{V}_{\mathrm{G}} = g\dot{V}_{\mathrm{G}} - \gamma g\dot{V}_{\mathrm{G}}$,

$$\therefore\ \ddot{V}_{\mathrm{G}} = \frac{g - \gamma g}{\gamma C_L + C_{\mathrm{p}}}\dot{V}_{\mathrm{G}}.$$

Now, solving this second-order differential equation gives the circuit time constant τ as $\frac{1}{\tau} = \frac{gC_{\mathrm{p}}}{C_L C_{\mathrm{boot}} - C_L C_{\mathrm{p}} + C_{\mathrm{p}} C_{\mathrm{boot}}}$.

$$\therefore \tau = \frac{C_{\mathrm{boot}}}{g}\left(\frac{C_L}{C_{\mathrm{p}}} - \frac{C_L}{C_{\mathrm{boot}}} + 1\right). \tag{5}$$

From equation (5) the expected operating frequency of the shift register can be calculated using $f = \frac{1}{2\pi\tau}$. The calculated frequency was 116 MHz, at an example 128 transistor load with bootstrap capacitance of 15.46 fF. This frequency is slightly higher than the 100 MHz frequency the circuit operates at. This could be due to g being slightly overestimated, as we picked a mid-point value rather than calculating an integrated average value. Finding the integrated average value of g gives

$$\overline{g} = \frac{1}{V_{\mathrm{clk}}}\int_0^{V_{\mathrm{clk}}} K(V_{\mathrm{GS}} - V_{\mathrm{t}})\,\mathrm{d}V_{\mathrm{GS}} = \frac{KV_{\mathrm{clk}}}{2} - KV_{\mathrm{t}}.$$

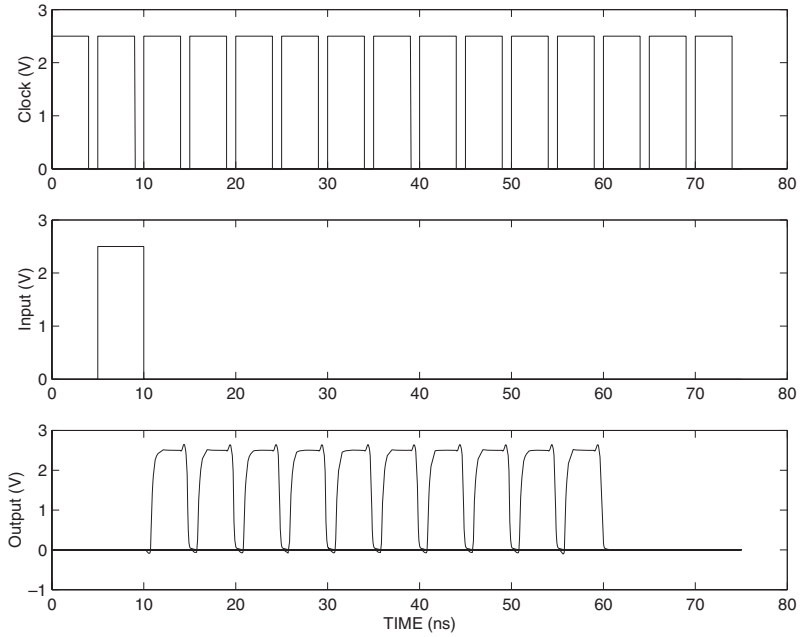

Figure 6. Simulation results of NRBL shift register. The top graph shows the 2.5 V non-overlapping clock pulses at 100 MHz after passing through the clock distribution circuit. The second graph shows a 2.5 V input pulse when `Clk 2` is pulsed. The last graph shows the operation of ten shift register stages, with a bootstrap capacitance of 15.46 fF, and parasitic capacitance of 3 fF. The register drives a load of 128 minimum size transistors for 0.25 μm technology.

Using this integrated average value $\overline{g}$ the calculated frequency with 128 transistor load and bootstrap capacitance of 15.46 fF is 106 MHz. This is closer to the 100 MHz clock frequency we expect the shift register to operate at, by simulation, as shown in the following sections.

5. Simulation

Simulation of the dynamic shift register was performed with HSPICE using an industrial 0.25 μm CMOS process, using Level 49 model parameters with a 2.5 V clock voltage. The value of the bootstrap capacitance is determined by the value of V_{boot} required as shown in equation (1), and it was chosen to be 15.46 fF. Using a bootstrap capacitance value of 15.46 fF, η is calculated to be 0.185; therefore $\eta \times 2.5 = 0.46$ V. This provides the necessary voltage to overcome the threshold voltage drop 0.41 V of the transistor. The shift register was simulated with a load inverter with size equivalent to 128 minimum size load transistors. Figure 6 shows the operation of the shift register, with two non-overlapping clocks at 100 MHz. When the input pulse is clocked at the serial I/P, the output pulses of each stage are as shown in figure 6.

5.1. Distributed clock tree

When one counts up all the capacitances in the registers of a large CMOS design, it often leads to large power dissipation when driven in a small time and at high repetition rate [8]. Long clock lines will also introduce substantial resistance [9]. This introduces an RC delay in the clock lines. To make the simulations more realistic a distributed clock tree is used to distribute the capacitance required to be driven and to also minimize clock skew. A cascade inverter design was used to size the inverter stages of the clock tree. In order to minimize the total delay a width factor of e (base of natural logarithms) is used.

5.2. Power dissipation

The power dissipation of the dynamic shift register is minimal as only one stage is on at a time. The total power dissipation is therefore mainly due to the charging and discharging of the capacitance that each stage drives, C_L. This is equal to $C_L V_{\text{clk}}^2 f$, where f is the clock frequency. From figure 7 it can be observed that the power dissipation of the circuit varies linearly with the clock frequency. The calculated power dissipation at 100 MHz with the load is 0.29 mW; however, this does not take account of the power dissipation due to the distributed clock circuit. Figure 7 shows simulated results of power dissipation versus varying voltage of operation and power dissipation versus varying frequency of operation, with a load of 128 minimum sized transistors.

Table 1 shows a comparison of the NRBL shift register with two other shift registers: a standard dynamic shift register [1] and Shibata's shift register [10]. The standard dynamic shift register is a simple pass transistor and inverter arrangement; however, two stages are required for a non-inverting output. The shift register proposed by Shibata uses a D flip-flop arrangement. From table 1 it can been seen that the NRBL shift register has the lowest transistor count and a low power dissipation.

5.3. Temperature simulation

The temperature dependence of transistors on the shift register performance must be considered. The simulations were performed using the industrially specified temperature range of -40 to 85 °C. The simulations were performed with a 2.5 V

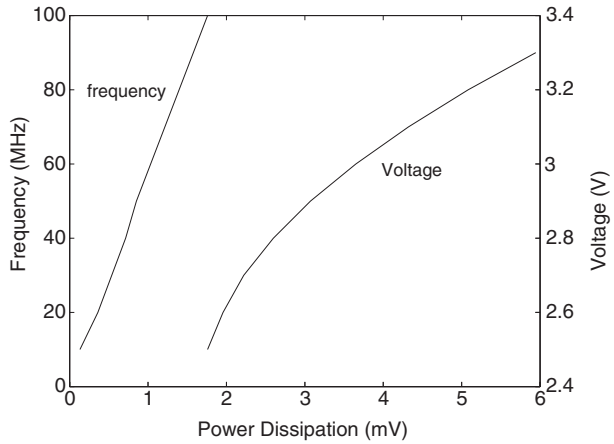

Figure 7. Simulation results of frequency versus power dissipation on the left y-axis and clock voltage versus power dissipation on the right y-axis. Both simulations presented in this diagram were simulated with 128 transistor loading. The frequency plot with clock voltage of 2.5 V indicates that the power dissipation of one stage of the shift register varies linearly with the clock frequency, as expected from the power dissipation formula in section 5.2. The voltage plot shows the power dissipation of one stage of the shift register as the clock voltage is varied with clock frequency of 100 MHz. At a clock voltage of 2.5 V the power dissipation is 1.75 mV.

clock voltage and a frequency of 100 MHz under 128 minimum sized transistor loading. From the simulations, the shift register was found to be functioning correctly within the specified temperature range. Even though the circuit was shown to work within the industrially specified temperature range, the temperature range was further increased in later simulations. Simulations showed that the circuit would still function correctly for a temperature range of -75 to 180 °C, which demonstrates the robustness of the shift register to temperature variations. This temperature range is greater than the standard military specified temperature range of -55 to 125 °C.

5.4. Process variation simulations

The CMOS fabrication process is a long sequence of chemical steps that result in device characteristics that follow a normal or Gaussian distribution [8]. Since the dynamic shift register discussed in this paper only consists of n-type transistors, only the fast and slow parameters are considered, as skew parameters are not relevant. From the simulated results the shift register was shown to be functioning correctly when simulated with one sigma process variations. The simulated outputs are similar to those shown in figure 6. Temperature simulation was repeated for process variation simulations. The simulated results showed the circuit functioning as designed for the extended temperature range as described in section 5.3.

5.5. Monte Carlo analysis

The design goal of this shift register is to minimize power dissipation and also area. The bootstrap capacitor is therefore designed to provide enough bootstrapping to overcome the threshold drop of the transistor, but at the same time keeping the area to a minimum. A Monte Carlo analysis of threshold voltages of the transistors in the circuit was performed to analyse the overall robustness of the shift register and its sensitivity to process parameters.

Table 1. Comparison of different shift register designs. Note that the NRBL shift register case contains only four transistors, no DC power supply and a low power dissipation. The rail voltage for the NRBL shift register is indicated by (—) in the table, as it is driven entirely by the 2.5 V clock. The power dissipation value obtained for the NRBL shift register was under a load of 128 minimum sized transistors, at 100 MHz and a clock voltage of 2.5 V. The simulations were performed using level 49 industrial 0.25 μm CMOS technology. The dynamic shift register in column two shows the simulated results, with the same loading value, frequency and clock voltage of the NRBL shift register. Care should be taken when comparing with Shibata's shift register, as it uses a 0.6 μm CMOS process with 3.3 V power supply and a mean capacitance load of 0.04 pF. This capacitive load is about 0.01 pF less than for the first two cases.

	NRBL shift reg	Dynamic shift reg [1]	Shibata's shift reg [10]
Max speed (MHz)	100	100	100
Technology (μm)	0.25	0.25	0.6
Transistor/stage	4	6	D-FF($\sim$15)
No. power supplies	0	1	1
Rail voltage (V)	—	2.5	3.3
Power dissipation per stage (mW)	1.75	2.98	1.5

The Monte Carlo analysis was performed with a Gaussian distribution with a standard deviation of 10 mV in threshold voltage. The 10 mV standard deviation was chosen from the relation between transistor area and threshold voltage mismatch, given in the manufacturer's data sheets. This voltage is added to the threshold voltage as calculated by the HSPICE simulator. The simulations for the Monte Carlo analysis were performed with a clock voltage of 2.5 V, clock frequency of 100 MHz and with a load of 128 transistors. The simulated mean rise time is 1.64 ns with a standard deviation of 90.54 ps. The simulated mean fall time of the circuit is 0.300 ns with a standard deviation of 3.62 ps. Compared with the rise and fall time of the circuit without the 10 mV standard deviation added to the threshold voltage, the circuit is shown to still function correctly and to not be sensitive to a standard deviation variation in threshold voltage.

6. Conclusion

A four-transistor-per-stage serial-to-parallel dynamic shift register has been designed and simulated with HSPICE using a 2.5 V, 0.25 μm CMOS process. It has been shown to drive a fan out of 128 with a very low power dissipation. The circuit has also been simulated with varying temperature, process variation and also a Monte Carlo analysis to test for the robustness of the design to manufacturing processes and applications. From the results presented, the shift register operates as designed and is robust to temperature and process parameter variation. Although the proposed dynamic shift register works with a low clock speed of 100 MHz, the performance requirement of the shift register is low power and small area. These requirements can be traded to increase the register speed. The present clock speed is suitable for application in the addressing and readout of smart sensor arrays.

Acknowledgments

Funding from the ARC and Sir Ross and Sir Keith Smith Fund is gratefully acknowledged.

References

[1] Mead C and Conway L 1980 *Introduction to VLSI Systems* 1st edn (Reading, MA: Addison-Wesley)
[2] Celinski P, López J F, Al-Sarawi S and Abbott D 2001 Low power, high speed, charge recycling CMOS threshold logic gate *Electron. Lett.* **37** 1067–77
[3] Moini A, Bouzerdoum A, Eshraghian K, Yakovleff A, Nguyen X T, Blanksby A, Beare R, Abbott D and Bogner R E 1997 An insect vision-based motion detection chip *IEEE J. Solid-State Circuits* **32** 279–84
[4] Ng J and Abbott D 2002 Introduction to solid-state quantum computation for engineers *Microelectron. J.* **33** 171–7
[5] Lu S 1988 A safe single-phase clocking scheme for CMOS circuits *IEEE J. Solid-State Circuits* **23** 280–3
[6] Ohba S, Nakai M, Ando H, Hanamura S, Satoh K, Takahashi K, Kubo M, Shimada S and Fujita T 1980 MOS area sensor II low-noise MOS area sensor with antiblooming photodiodes *IEEE Trans. Electron Devices* **27** 1682–7
[7] Sklavos N, Kitsos P, Zervas N and Koufopavlou O 2000 A new low and high speed bidirection shift register architecture *Technical Report* University of Patras, Patras, Greece
[8] Weste N H E and Eshraghian K 1993 *Principles of CMOS VLSI Design, A System Perspective* 2nd edn (Reading, MA: Addison-Wesley)
[9] Rabaey J M 1996 *Digital Integrated Circuits, A Design Perspective* 1st edn (Upper Saddle River, NJ: Prentice-Hall)
[10] Shibata N, Watanabe M and Tanabe Y 2002 A current-sensed high-speed and low-power first-in-first-out using a wordline/bitline-swapped dual-port SRAM cell *IEEE J. Solid-State Circuits* **37** 735–50