

Quality Factor Optimization Process of a Tapered Slow-Wave Coplanar Strips Resonator in CMOS Technology

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Abstract—This paper presents a design procedure for a high quality factor slow-wave tapered coplanar strips (CPS) resonator for application at 60 GHz in a 90 nm standard CMOS process. Utilizing the current and voltage standing wave profile in a quarter wavelength resonator, a slow-wave tapered resonator with an improved quality factor of 28.4 is designed. Due to the slow-wave structure, the resonator is compact and presents a quality factor improvement of 89% compared to the conventional tapered CPS resonator and 220% compared to the conventional uniform CPS resonator.

Index Terms—Quality factor, tapered coplanar strips, resonator, slow-wave, CMOS.

I. INTRODUCTION

Despite the drawbacks associated with the use of low-resistivity silicon substrates, silicon CMOS technology, offer high level of integration at low cost. Furthermore, a direct benefit of using this technology is the exploitation of the fast technology scaling [1]. With the scaling of the CMOS transistors to sub-100 nm dimensions, the intrinsic frequency has increased dramatically, making this technology very attractive to design circuits operating at microwave and mm-wave frequencies. This has assisted with increased market demand for low-cost electronics that operate in the license-free band at 60 GHz [2], [3].

To effectively exploit modern CMOS processes in mm-wave circuits, on-chip passive components such as capacitors, inductors and transmission lines with high quality factors are required [4], [5]. Furthermore, since these passive components tend to occupy a large amount of on-chip area, it is necessary to reduce their dimension to reduce the cost [6].

With their explicitly distributed behavior, transmission lines play a critical role in mm-wave circuits. Moreover, due to the relatively short wavelength in the mm-wave regime, quarter wavelength transmission lines can be realized on-chip [6]. These lines can be used not only to carry signals, but also as reactive components and resonators in oscillators and amplifier circuits. For optimal exploitation of the chip area, it is important to reduce the dimensions and aspect ratio of transmission line-based components while improving their quality factor [6], [7].

Although coplanar transmission lines (TLs) like coplanar strips (CPS) have the advantage of lower resistive loss than microstrip lines, they typically suffer from conductive loss in the silicon substrate. More specifically, this conductive loss is mainly due to the penetration of the electric field of

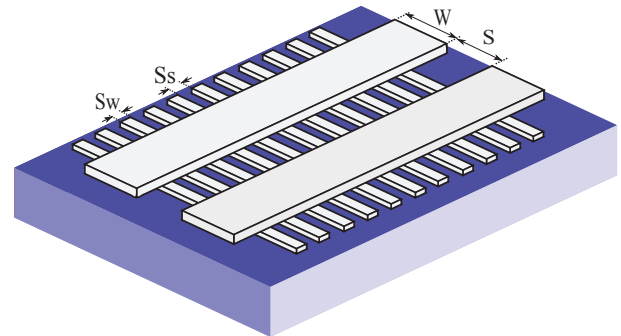


Figure 1. Uniform slow-wave coplanar strips structure.

the coplanar TL into the low resistivity silicon substrate [8]. Reduction of this loss by placing a solid metal shield under the coplanar transmission line is not an effective solution, because a continuous shield introduces eddy current loss [9], [10].

Placing an array of closely spaced narrow floating strips under the coplanar transmission line is an effective method of shielding and it reduces substrate conductive loss. In contrast to the solid metal shield, if the floating strips are narrow enough, eddy current loss becomes negligible because of the suppression of the current component parallel to the transmission line direction. Therefore the shield effectively reduces the substrate losses, by reducing the eddy current loss in the substrate [4].

Figure 1 shows the structure for slow-wave uniform coplanar strips. This is called a slow-wave structure, as it does not only act as a shield but also reduces the propagation velocity of the electromagnetic wave.

Another important feature of the slow-wave coplanar transmission lines in microwave monolithic integrated circuit (MMIC) design is the reduction of the propagation speed, which results in reduction in the effective wavelength [4]. Therefore, more compact components based on shorter transmission lines can be implemented on-chip, hence resulting in a reduction of the required silicon area [5], [11].

A coplanar strip is amenable to a high level of integration. As a balanced structure, it provides a favorable basis for the realization of integrated voltage controlled oscillators (VCOs) [12]. In previous work [13], we introduced design guidelines for optimized slow-wave CPS in terms of quality factor and effective wavelength. Based on these guidelines, in the present article, we demonstrate the optimization of a tapered high

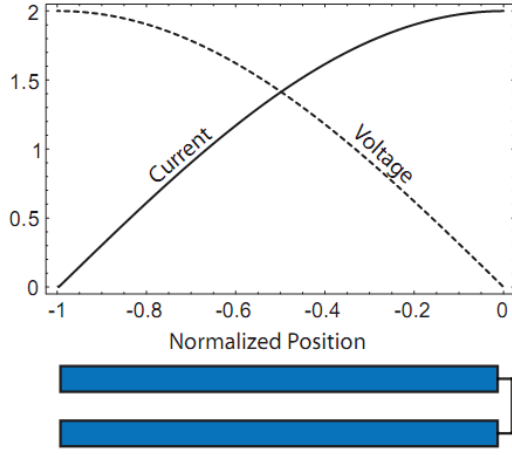


Figure 2. Standing wave voltage and current in a quarter wavelength resonator. Adapted from [7].

quality factor slow-wave CPS. This is achieved by using data from 3D full-wave electromagnetic simulations and applying Harmony Search (HS) numerical optimization method [14].

II. TAPERED TRANSMISSION LINE RESONATOR

A shorted $\lambda/4$ transmission line can be used as a resonator as an alternative to a parallel LC tank resonator in a VCO. For a cross-coupled VCO, a balanced transmission line resonator is needed. So, this paper focuses on tapered slow-wave CPS to design a resonator for 60 GHz CMOS applications and seeks to achieve a high quality factor resonator that consumes small on-chip area.

As explained before, using slow-wave TL-based resonator is an effective solution for reducing substrate losses in CMOS technologies and achieving a high quality factor resonator. Furthermore, the standing wave behavior of the quarter wavelength resonator can be exploited by varying the shape along the transmission line to reduce the effective wavelength and consequently achieve even higher quality factor [7]. A quarter wavelength differential CPS, which is shorted at one end, exhibits a standing wave mode at its resonance frequency, as shown in Figure 2 [7], [15]. Keeping this in mind and considering the Q-factor equation for a TL which is

$$Q = w \frac{E_{\text{stored}}}{P_{\text{diss}}} = \omega \frac{\int_0^l \frac{1}{4} (V^2(x)C(x) + I^2(x)L(x)) dx}{\int_0^l \frac{1}{2} (V^2(x)G(x) + I^2(x)R(x)) dx}, \quad (1)$$

one can conclude that to reach a higher Q-factor, the TL resonator needs to be more capacitive at the beginning of the transmission line, where the voltage is maximum. Also it needs to be more inductive at the end of the transmission line, where the current is maximal. Furthermore, to minimize the dissipated power, the TL needs to have its minimum conductance at the beginning and its minimum resistance at the end of the line. With this explanation, it has been shown in [7] that a maximum Q-factor can be achieved with a numerical

optimization of the width and spacing of two strips of the CPS. A design of optimum CPS is presented in [7].

III. OPTIMIZATION SCHEME

A. Transmission Line Equations

Considering a general RLGC model of a transmission line with all R , L , G and C , functions of position x , the well known telegrapher's equations can be written as [16].

$$\frac{dV(x)}{dx} = -(R(x) + j\omega L(x)) \cdot I(x) \quad (2a)$$

$$\frac{dI(x)}{dx} = -(G(x) + j\omega C(x)) \cdot V(x). \quad (2b)$$

As described in [17] after transformation from physical length into electrical length, the voltage distribution along the line can be described by the differential equation

$$\frac{d^2 V(\theta)}{d\theta^2} - \frac{1}{Z_0(\theta)} \frac{dZ_0(\theta)}{d\theta} \frac{dV(\theta)}{d\theta} - V(\theta) = 0. \quad (3)$$

Solution of this equation can be found analytically if the characteristic impedance profile is a well-behaved function, e.g. linear or exponential. However, for an *a-priori* unknown arbitrary variation of the characteristic impedance along the line, as assumed in the present work, (3) cannot be solved analytically [7].

B. Numerical Optimization

The optimization of the tapering is performed based on the data gathered in a preliminary parametric study of uniform slow-wave CPS segments. Based on the guidelines given in [13], the slow-wave floating strips have been chosen to be $0.2 \mu\text{m}$ wide with a spacing of $2.4 \mu\text{m}$ between each others. Taking on-chip area limitation into account, the maximum of strip with W and spacing S of the CPS are set as $65 \mu\text{m}$. Since the resonator is also used as DC bias line, the minimum width of the lines was set to $5 \mu\text{m}$. The full wave 3D EM simulator, HFSS [18], was first used for ABCD matrix extraction of uniform $100 \mu\text{m}$ long differential coplanar strips. The values of widths and spacings were varied between $5 \mu\text{m}$ and $65 \mu\text{m}$ and simulated at 60 GHz. The computed scattering matrices were saved in a file as a data base for the optimization. Parameters for a standard 90 nm CMOS process were used for modeling the silicon substrate, dielectric and metal layers in HFSS. Top metal was used for CPS paths and metal 5 for the underneath floating strips. The S-parameters were converted to ABCD parameters with Matlab, which is also used in the subsequent optimization of the resonator tapering.

The optimization is initiated from a uniform CPS resonator with $l = \lambda_{\text{eff},1}/4$, where $\lambda_{\text{eff},1}$ is the effective wavelength in the first iteration. Then the resonator is divided into 100 cascaded uniform sections of equal length of $l/100$. After assigning the S and W as depicted in Figure 1 of each section which are determined by the optimization algorithm, the

resonator ABCD parameters are calculated from multiplication of ABCD matrices of all the small sections as shown

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{Tot}} = \prod_{i=1}^{100} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{l/100(S_i, W_i)}. \quad (4)$$

The HFSS simulations of the uniform lines are performed for $100 \mu\text{m}$ long lines, therefore, the ABCD matrix of the corresponding sections with $1 \mu\text{m}$ length is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{1 \mu\text{m}(S_i, W_i)} = \sqrt[100]{\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{100 \mu\text{m}(S_i, W_i)}}, \quad (5)$$

from that the ABCD matrix of the corresponding sections with length $l/100$ needs to be adapted according to

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{l/100(S_i, W_i)} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{1 \mu\text{m}(S_i, W_i)}^{l/1 \mu\text{m}}. \quad (6)$$

From the total ABCD matrix (4) of the tapered resonator, the characteristic impedance Z_c , the propagation constant γ , the effective wavelength λ_{eff} and the quality factor Q can be readily obtained as

$$Z - c = \sqrt{\frac{B}{C}}, \quad (7)$$

$$\gamma = \alpha + j\beta = \cosh^{-1}(A)/l, \quad (8)$$

$$\lambda_{\text{eff}} = \frac{2\pi}{\beta}, \quad (9)$$

$$Q = \frac{\beta}{2\alpha}. \quad (10)$$

It must be mentioned that since the effective wavelength of the tapered transmission line is not constant along the line, the total length varies with the resonator shape, and a scaling factor therefore needs to be introduced for the resonator length. The optimizer starts then from an initial effective wavelength, $\lambda_{\text{eff},1}$, and after calculation of the more accurate effective wavelength ($\lambda_{\text{eff},2}$) of the tapered transmission line from (9), the calculation of the total ABCD matrix is repeated with the new resonator length i.e. $\lambda_{\text{eff},2}/4$. This process continues iteratively until the scaling factor $\lambda_{\text{eff},n}/l$ in the n^{th} iteration converges satisfactorily to one. Then the optimizer starts the next set of W and S to form another tapered resonator and this process continues iteratively until the tapered CPS converges to the optimum resonator with a maximum quality factor.

IV. OPTIMIZATION RESULTS

The optimum tapered shape of the slow-wave coplanar strips resonator derived in this work is shown in Figure 3. To confirm the results of the optimization, simulations of both the optimized tapered slow-wave CPS, and uniform slow-wave CPS resonators are performed using HFSS. Table I

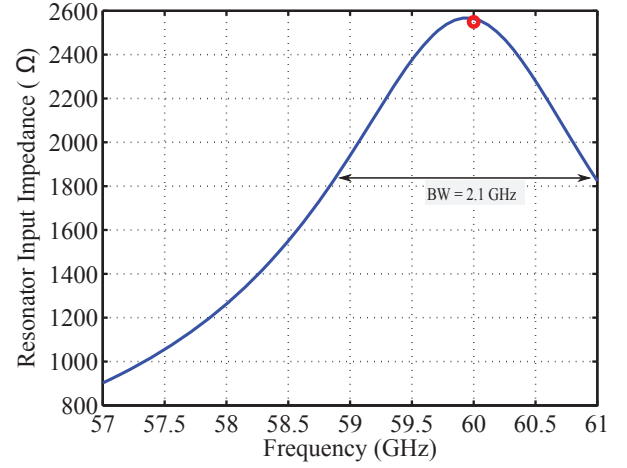


Figure 4. HFSS Simulation results for input impedance for the optimum slow-wave tapered CPS resonator. The single red point shows the calculated input impedance from the optimizer results.

compares the resonance frequency, length and Q-factor of four types of quarter wavelength CPS resonators. The reference for the comparison is the measured characteristics of the conventional uniform CPS resonator which is simulated and fabricated in [7]. This resonator has a length of $635 \mu\text{m}$ to resonate at 57.9 GHz and has a Q-factor of 8.8. All other resonators are also designed to resonate at around 60 GHz. The second resonator in the table is a conventional tapered CPS resonator from [7]. It has a length of $498 \mu\text{m}$ and Q-factor of 15, which shows 70.4% improvement in Q-factor, compared to the uniform resonator. Comparing the simulation and measurement, some variations in the resonance frequency are observed in both cases, however, there is a good match in Q-factors of simulation and measurement results. The table also shows the slow-wave uniform and slow-wave tapered CPS resonators from [13] and this work, respectively. The uniform slow-wave resonator has a length of $222 \mu\text{m}$ and Q-factor of 16. The optimum tapered slow-wave resonator designed in this work has a length of $320 \mu\text{m}$ which is relatively short and reasonable for on-chip implementation. The Q-factor can be found from the resonator input impedance which is shown in Figure 4. The optimum resonator has a Q-factor of 28.4 which is a significant improvement in Q-factor by 220% compared to the conventional uniform resonator, or 89% improvement, compared to the tapered resonator in [7]. Figure 4 also shows the resonator input impedance which is calculated from optimizer results. Since optimization has been done just in one frequency, 60 GHz, the input impedance is shown just in that frequency. The figure shows a very good match between optimization results and HFSS simulation results.

V. CONCLUSION

Using parameters of a standard digital 90 nm CMOS process, the optimization process for quarter wave length slow-wave CPS resonator with an optimum Q-factor at 60 GHz was

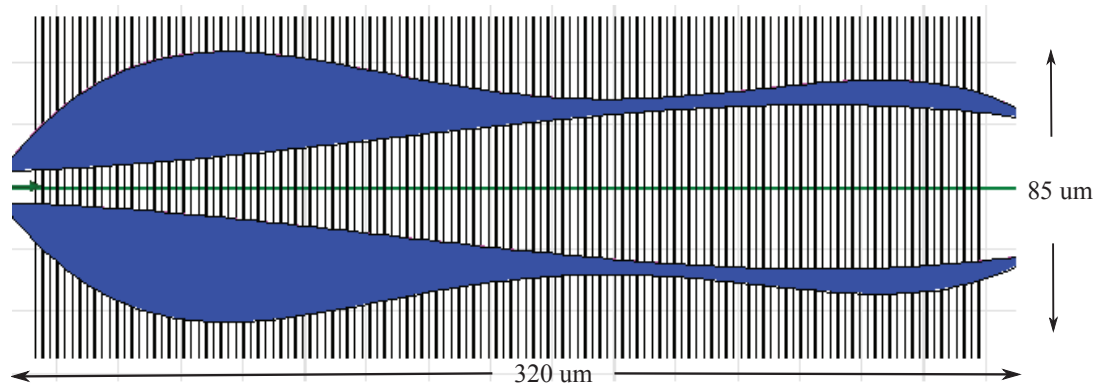


Figure 3. Optimum slow-wave tapered resonator

Table I
COMPARISON OF Q-FACTOR, RESONANCE FREQUENCY AND LENGTH OF DIFFERENT TYPES OF QUARTER WAVELENGTH CPS RESONATORS.

Resonator Type	Length	f_0 (GHz)	Q-factor	Q-factor Improvement
Uniform, Simulated [7]	635 (μm)	62	8.8	reference
Uniform, Measured [7]	635 (μm)	57.9	8.8	reference
Tapered, Simulated [7]	498 (μm)	58	15	70.4%
Tapered, Measured [7]	498 (μm)	54.4	15	70.4%
Slow-wave Uniform, Simulated [13]	222 (μm)	60.5	16	81.8%
Slow-wave Tapered (this work), Simulated	320 (μm)	59.9	28.4	220%

presented. Using the Harmonic Search optimization method a slow-wave tapered resonator was designed, demonstrating a significant Q-factor improvement of 220% compared to the conventional uniform resonator and 89% improvement compared to the optimum conventional tapered resonator in [7]. Because of the limitations we applied in optimization process, and using slow-wave structure, the on-chip area of the optimized resonator remains reasonable. The minimum width of the signal paths was also limited to $5\mu\text{m}$, to guarantee a sufficient width for safe use as DC bias of the VCO core.

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