mm-Wave Systems for High Data Rate Wireless Consumer Applications

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***Abstract*— ISM spectrum at 60GHz has attracted attention for possible high-speed applications in wireless communications for well over ten years. However, no high volume applications have emerged. Despite progress in mm-wave ICs, the power and cost of these efforts have not reached the level needed for mass deployment.**

This paper summarises the ARC funded GLIMMR project which aims to remedy this situation by designing systems on silicon that have both low cost and low power. In particular, the paper presents design work done to date that indicate that silicon (particularly SiGe) is on the cusp of being able to provide economical mm-wave systems.

***Index Terms*— mm-wave, 60GHz, SiGe, OFDM**

I. Introduction

The GLIMMR project is based on an Australian Research Council (ARC) funded linkage project that is being carried out at Macquarie University, the University of Adelaide and the University of South Australia. The main commercial sponsor is NHEW R&D Pty Ltd, with supporting sponsors Cadence Design Systems, Jazz Semiconductor, Peregrine Semiconductor, Intel Corporation and AWR.

The aim of the project is to design a complete mm-wave system for high bandwidth communication using the ISM band at 60GHz[1]. In some ways, this is a continuation of a project started in the late 1980's by the CSIRO and Macquarie University [2] that led to successful commercialisation of the IEEE 802.11a standard at 5GHz. The focus of the previous project was for the most around 40GHz, a frequency for which the CSIRO had designed various GaAs mm-wave building blocks. Currently, there is somewhat of a resurgence of interest in high-speed systems at 60GHz [3-12].

In this project, the main target is a "system-on-silicon", designed to achieve a low cost and low power solutions. This requires new innovations in circuit design, antenna design and communications architecture to produce a suitable system. We are attacking the RF, analog and baseband in parallel so that we achieve an overall integrated system.

Manuscript received December 9th, 2005. This work was supported in part by an ARC Linkage Grant.

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II. A Strawman Specification

In this section, the current baseline specification for a 60GHz wireless unit is outlined. The basic concept is to design a self-contained transceiver with approximately 1Gb/s throughput, 1mW transmit power output, 10dB receiver noise figure and low gain omni-directional antennas. With such a specification, a link budget shows that a range of a few metres is possible. This basic unit may be augmented by combining with a high-gain antenna (horn, dish, etc.) or placing in a beam steering array to improve distance or combining in parallel to increase the bandwidth. A power consumption of the overall unit is set at below 200mW (for 1mW TX power). The cost of the unit (antenna to bytes) should be around $10-20 with an end target of $5.

Typical uses include desktop wireless busses for disks, video and still cameras and multimedia video connections for home entertainment systems (e.g. from media source to ceiling mounted projector).

III. Issues

A. Cost

The low cost target we have set for the system dictates

perhaps a two-chip solution, where one chip contains the RF and analog and the other chip, the digital PHY and MAC. While the RF/analog chip might be a III/V device, it is unlikely due to cost, yield and the inability to achieve real combinations of RF, analog and digital on GaAs or InP. We have therefore targeted a silicon-based approach to achieve our aggressive cost goals. One may question whether what we are doing is a commercial development. The fact is that no low-cost 60GHz systems exist. New innovations and inventions are required across the board to achieve our goals. Setting cost as a research goal is somewhat novel in Australia but is required to be able to develop competitive commercial systems in the future. The other purpose of this project is to train people capable of turning research into development.

Another area where cost is significant is packaging. Traditionally III/V MIMICs have been combined to produce mm-wave systems. This results in many relatively expensive (in power and cost) microwave interconnections between components due to the low level of integration. We intend implementing a "System On Chip" (SOC) approach where the only 60GHz connection is the antenna (or antennas). In this paper, we will present some preliminary ideas and simulations that address this area.

B. *Performance*

The desired circuit performance at the desired power is really a function of the transistor transition frequency (f_T) of the process. The higher the f_T, the less power will be needed to achieve given gain and noise parameters at a particular operating frequency (below f_T).

As the cost constraints seem to limit the technology choices to silicon, the feasibility is tied to current silicon processes being able to achieve adequate performance at the frequency of interest. Mm-wave circuits in CMOS processes at 130nm have been demonstrated and at 90nm 60GHz circuits would appear quite feasible. We have chosen to use a SiGe option on a CMOS process. This keeps the prototyping costs low as only 180nm feature masks are required to achieve adequate performance at 60GHz. The f_T of the SiGe npn transistors is around 155GHz.

Apart from noise figure and gain, the most significant performance parameter that impacts feasibility is the phase noise of the (first) local oscillator. As we want a completely monolithic implementation, we desire an on-chip local oscillator. Due to lossy on-chip passives (capacitors, inductors transmission lines), this requires a great deal of attention. Our approach to date is to pay strict attention to the baseband modem design so that it can cope with the phase noise of the oscillators on hand. This supports the technology choice where digital transistors are available in abundance while analog transistors have performance limitations at the highest frequencies of interest.

IV. Work to Date

A. *RF Circuits*

To date we have designed and simulated a number of key building blocks were combined onto a test chip and submitted for fabrication in January 2006. We will summarise our work to date to give indicative performance numbers.

We are targeting a single local oscillator (LO), dual conversion superheterodyne architecture with a first LO frequency of 48GHz and an intermediate frequency (IF) of 12GHz. The IF is the LO frequency divided by four, similar to commercial IEEE 802.11a designs. We will also explore direct conversion designs.

1) *Low Noise Amplifier (LNA)*

We have designed a three stage LNA with an overall gain of 21dB, a noise figure of 8dB and a power dissipation of 15.3mW at 1.8 volts. The input IIP3 is -17.2dBm.

2) *Down-mixer*

A single balanced Gilbert mixer has been designed to convert from 60GHz to 12GHz. It has a simulated conversion gain of 16dB and a noise figure of 17dB. The IIP3 is -1dBm. Combined with the LNA, the overall gain is 40dB and the noise figure 9dB.

3) *Local Oscillator (LO)*

We have designed a variety of oscillators based on a Colpitts architecture for 48GHz and 60GHz[13-15]. They use transmission lines as tuning elements. Simulated phase noise values are in the range of -80dBc/Hz at a 1MHz offset from the carrier. Resistively and inductively loaded oscillators have been designed. These oscillators consume around 36mW for indicated powers of -5 to -10dBm.

4) *Power Amplifier (PA)*

A set of power amplifiers have been designed to deal with a range of usage situations (i.e. high and low power). A representative design has an output power at a 1dB compression limit of 9.1dBm. It dissipates 198mW from a 1.8V supply. It has 8dB gain. A lower power version is also planned for a 0dBm output but at this stage we are over-powering the PA to deal with unmodelled parasitic losses.

5) *Phase Lock Loop (PLL) Dividers*

A regenerative divide by two circuit based on a double balanced Gilbert mixer is used as the first divider. In simulation it operates from 48-60GHz. Subsequent to this (24GHz), ECL dividers reduce the LO to 6GHz where CMOS can take over.

6) *Transceiver Issues*

While individual blocks can be designed with reasonable effort, the combination of these blocks into a low-power

receiver or transmitter requires close attention to the design of each block.

As an example of this, consider the LO in a transceiver. For a half-duplex system, it has to drive the receive down-mixer, the transmit up-mixer and the first divide stage of the synthesizer. Normally, the LO would drive three buffer amplifiers (in our case at 48GHz or 60GHz), which in turn drive the appropriate mixers. This takes space (the amplifiers use transmission lines and hence are fairly large) and power. A tradeoff is to build buffering into the local oscillator say by using a cascode stage[14]. This degrades the phase noise of the oscillator which has to be traded against overall system requirements. By combining antenna/RF/baseband into the one project we hope to have a fluid interchange between achievable RF performance and a baseband that can deal with real radio imperfections.

Another problem is designing for process, voltage and temperature (PVT) to achieve high yields (for instance, current 5GHz CMOS RF circuits have yields in the 80-95% range). One area of particular interest is the LO center frequency. On one hand we desire a low voltage controlled oscillator (VCO) constant (MHz/volt) for good PLL performance and minimal phase noise degradation via noise on the control voltage. On the other, we require a large tuning range to deal with PVT spread.

Indicative Monte-Carlo simulation runs of a 60GHz oscillator indicate a 5GHz spread around the nominal center frequency. We achieve centering in the same way that state-of-the-art 5GHz CMOS chips do, that is, we use bank switched (nMOS switches) capacitors (Metal-Insulator-Metal – MIM) controlled by a serial digital shift register. The PLL varactor (an nMOS transistor), has a tuning range of 500MHz which corresponds to the minimum step of the switched capacitor. This example in its own right shows why CMOS is the technology of choice for any SOC RF project (provided the desired performance can be achieved).

B. Analog Circuits

A key circuit in terms of minimising power dissipation in an integrated transceiver is the Analog to Digital Converter (ADC) used in the receiver. There are normally two, one for the Inphase channel and one for the Quadrature channel. As the ADCs in this project have to operate in the vicinity of 1GHz, every effort has to be made to reduce the number of bits that have to be digitized and the inherent power of the converter. We have been experimenting with very simple flash-converters with around 5-6 bits of precision.

C. Antennas

Two approaches have been considered in relation to the antenna connections. The first is to flip-chip the SiGe chip onto a SOS chip on which the antennas are placed.

The second approach involves trying to use conventional bonding and packaging technology.

1) Flip-chip Approach

By using a substrate (Sapphire) that has excellent RF characteristics (silicon does not), a wide range of antenna structures maybe designed on the SOS substrate. We are using the Peregrine Semiconductor, “Ultra Thin Silicon” process for this option. Work is in progress looking at die attach techniques.

2) Bond Wire Antennas

We advance the idea of using bond wires as antennas at 60GHz. Bond wires have previously used to implement high-Q inductors for monolithic oscillators[18].

There are two basic approaches. The first involves creating a longer than normal looping bond which for sake of discussion loops up from the chip bond pad and then down to a package pad. The bonded chip is then encased in epoxy (as normal), but the package height is extended to encase the longer than normal looping bond wires. The top of the package is then milled down to sever the looping bond wire. This could be further tuned via laser etching of the exposed antenna wire end.

The other approach is to bond laterally from chip antenna pad to a package pad which consists of just a metal pad (i.e. not connected to a pin). Again a laser tuning method in combination with on-chip VSWR circuit could optimize each antenna in the production environment.

We have simulated these structures and look forward to testing our fabricated chip. Issues to be examined, include coupling from the antenna into the substrate and it’s effect on circuits and the effect of a variety of ground-planes and tuning methods. We plan to use on-chip self-test to aid in this tuning.

Antennas, so designed, if feasible, are cheap, manufacturable and have exceptionally high bandwidth comparing with other approaches such as patches. So far, our simulations, indicate maximum gains of the order of 5-6dBi and symmetric radiation patterns normal to the chip surface.

D. Baseband

Our work at baseband has been initially guided by the desire to have a multi-path resistant modulation strategy. This comes about by virtue of the proposed indoor usage models. Whilst we are also investigating other approaches, the work presented here relates to our investigations into the use of an adaptive modulation and coding orthogonal frequency division multiplexing (AMC-OFDM) scheme. Such a scheme aims to exploit the frequency selective nature of the multipath channel by assigning different signal constellations and/or code rates to each subcarrier. Briefly, the signal constellation size and/or code rate on each subcarrier is increased in proportion to signal-to-noise ratio

on that subcarrier. We consider here a system in which 16 subcarriers are used, with a choice of BPSK, QPSK, or 8PSK constellation, and a fixed ½-rate code. More specific details on this system can be found in [19]. It is noted that by using only 16 subcarriers, the degradation in performance due to effects such as phase noise would be less severe than if a large number of subcarriers were used.

V. Simple Arrays

It was felt that some advantage could be gained from using more than one antenna. This section summarises our work which uses a simple two element beam steered antenna for transmitter and receiver.

The performance of the system is investigated for two indoor scenarios that were simulated by way of the 3D ray tracing approach described in [19], based on a room having height 2.7m, width 2.9m, and length 4.9m. The first scenario corresponds to the case where the transmitter (Tx) and receiver (Rx) are both located on a bench of height 0.7m and length 3m, which is assumed to lie along the longest wall. The second scenario considered is that in which the room is empty. For the empty room scenario, the placement of the Tx and Rx is essentially unrestricted; the only restrictions are that the Tx and Rx are separated from the nearest wall or other reflecting surface (ceiling or floor) by at least 5cm, and that the distance between the Tx and Rx, projected onto the longest wall, is at least 5cm. For each scenario, a set of 5000 complex-valued impulse responses have been generated based on a Monte Carlo simulation approach. It is noted that the complex-valued impulse responses encapsulate the phase shifts that occur in reflections, and due to the path length differences. Further details on the assumptions regarding Tx and Rx placements within the aforementioned scenarios, and on the 3D ray tracing approach, can be found in [19].

To allow sufficiently reliable communications at data rates exceeding 1Gb/s whilst using a transmit power on the order of 1mW, we are investigating the use of 2-element phased arrays at both the transmitter and receiver. We assume for each antenna element an idealized version of the bond-wire antennas described in Sec. IV-C-2 (specifically we assume vertically aligned half-wavelength dipoles with 2dBi gain), with half-wavelength element spacing and phase shifts between each antenna element limited to a set of only 4 values as

$$\Psi_0 = [-180^o, -90^o, 0^o, 90^o].$$

The other link budget parameters are broadly in line with those mentioned in Sec. IV-A.

Figs. 1 and 2 respectively show in the bench top and empty room scenarios, the cumulative distribution functions (CDFs) for the achievable throughput assuming the use of the adaptive ½-rate coded phase-shift keying OFDM system described in [19]. Note that the reduction in throughput due to the inclusion of a cyclic prefix has been accounted for in the results. Specifically, this throughput reduction was a factor of 16/18 in both scenarios. It is noteworthy that in both the 60 GHz indoor scenarios considered, the performance with single antennas having transmit power of 6dBm (i.e. 4mW) is similar to the performance with 2 transmit antennas and 2 receiving antennas when the total transmit power was set to 0dBm (i.e. 1mW). In other words, the total transmit power can be reduced by a factor of 4 when using the investigated phased array approach. The reason behind these gains is two-fold. Firstly, the increased directivity achieved at both the transmitter and the receiver can be up to 6dB. As a result, the maximum possible gain achieved by using the considered phased arrays would be 6dB for any individual path between the transmitter and receiver. However, it would not be possible to simultaneously achieve a 6dB gain for each multipath component. Moreover, in many cases, the maximum gain would not be achieved on any of the multipath components since the azimuthal alignments of the antennas in each array were assumed to be uniformly distributed, and the main beam direction would often not correspond to the exact azimuthal path direction. Nonetheless, additional gains occur in some cases since the arrays are capable of reducing the destructive interference that sometimes occurs between the multipath components. Hence, the overall gain with the proposed phased arrays in the scenarios considered was observed to be approximately 6dB, allowing an approximate four-fold reduction in transmit power. It should be noted that such a reduction in transmit power affords significant reductions in the overall power consumption.

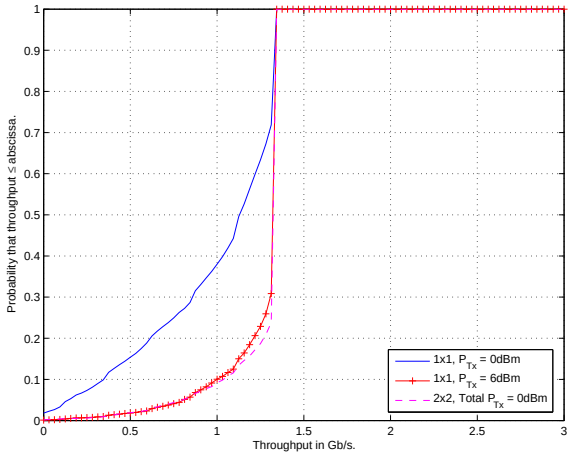

Fig. 1. CDFs of expected throughput with adaptive ½-rate coded OFDM in the bench top scenario.

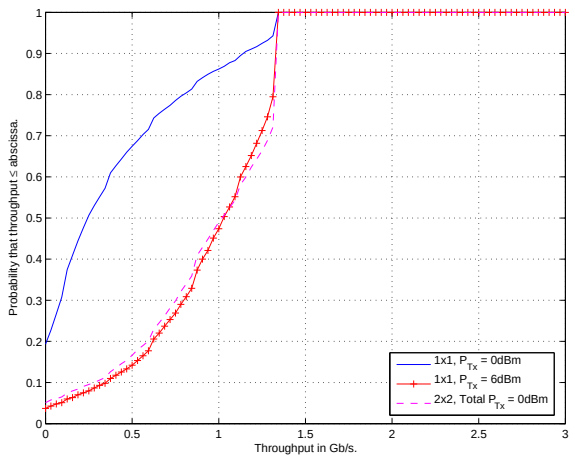

Fig. 2. CDFs of expected throughput with adaptive ½-rate coded OFDM in the empty room scenario.

VI. Summary

The status of a project to design and develop high speed wireless systems at 60GHz for consumer applications has been presented. Simulations for RF, antennas and baseband have indicated the proposed approach seems quite feasible. The use of simple arrays would seem to provide benefit. Measurements on fabricated test chips will likely modify or reinforce our approach.

Acknowledgment

This project is supported by an Australian Government ARC Linkage Grant. The research is carried out by Macquarie University, the University of Adelaide, the University of South Australia and NHEW R&D Pty. Ltd. The commercial sponsors are NHEW R&D, Cadence Design Systems, Jazz Semiconductor, Peregrine Semiconductor, Intel Corporation and AWR. We would like to acknowledge Adam Lauterbach for his preliminary work on SiGe oscillators.

References

[1] P. F. M. Smulders, "60 GHz radio: prospects and future directions," in *Proceedings of IEEE Benelux Chapter Symposium on Communications and Vehicular Technology*, 2003, Eindhoven

[2] D. J. Skellern, T. Percival, N. Weste, C. Lee, P. Ryan, T. McDermott, J. Dalton, J.Graham, T. Wonga and A. Myles, "A mm-wave high speed WLAN for mobile computing - architecture and prototype modem/code implementation," *HotInterconnects Symposium*, Stanford, Aug, 1996.

[3] A. Colquhoun, G. Ebert, J. Selders, B. Adelseck, J.M. Dieudonne, K.E. Schmegner, W. Schwab, **"**A fully monolithic integrated 60 GHz receiver," *Technical Digest 11th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium,* 22-25 Oct. 1989, pp185-188.

[4] C.A Zelley, A.R. Barnes, D.C. Bannister, R.. Ashcroft, **"**A 60 GHz integrated sub-harmonic receiver MMIC," *22nd Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium,* Nov. 5-8, 2000, pp.175-178.

[5] H. Zirath, T. Masuda, R. Kozhuharov and M. Ferndahl, "Development of 60-GHz Front-End Circuits for a High-Data-Rate Communication System," *IEEE IEEE Journal of Solid-State Circuits*, Vol. 39, No. 10, Oct 2004, pp. 1640-1649.

[6] C.H. Doan, S. Emami, A.M. Niknejad, R.W. Brodersen, "Millimeter-ave CMOS design," *IEEE Journal of Solid-State Circuits,* vol. 40 no. 1, Jan. 2005, pp.144-155.

[7] W. Winkler, J. Borngräber, B. Heinemann, F. Herzel, "A Fully Integrated BiCMOS PLL for 60 GHz Wireless Applications," In '*Proceedings of the IEEE International Solid-State Circuits Conference, ISSCC2005*,' San Francisco, Feb. 2005.

[8] W. Winkler, J. Borngräber, H. Gustat, F. Korndörfer, "60 GHz Transceiver Circuits in SiGe:C BiCMOS Technology," In *Proceedings of the 30th European Solid-State Circuits Conference*, Leuven Belgium, 20-25 Sept. 2004.

[9] B.A. Floyd, S.K. Reynolds, U.R. Pfeiffer, T. Zwick, T. Beukema, B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," *IEEE Journal of Solid-State Circuits,* vol. 40. no. 1 Jan. 2005, pp156-167.

[10] S. Reynolds, B. Floyd, U. Pfeiffer, T. Zwick, "60GHz Transceiver Circuits in SiGe Bipolar Technology," *2004 IEEE International Solid-State Circuits Conference*, San Francisco, 2004.

[11] S.K. Reynolds, "A 60-GHz superheterodyne downconversion mixer in silicon-germanium bipolar technology," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, Nov. 2004, pp2065 - 2068

[12] C.H. Doan, S. Emami, D.A.; Sobel, A.M. Niknejad, R.W. Brodersen, "Design considerations for 60 GHz CMOS radios," *IEEE Communications Magazine*, vol. 42, no. 12, Dec. 2004, pp132-140.

[13] W. Winkler, J. Borngräber, B. Heinemann, "60GHz and 76GHz Oscillators in 0.25µm SiGe:C BiCMOS", *IEEE International Solid-State Circuits Conference*, 2003, pp454 -455.

[14] H. Li, H.-M. Rein, "Millimetre-Wave VCOs With Wide Tuning Range and Low Phase Noise, Fully Integrated in a SiGe Bipolar Production Technology," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, Feb. 2003, pp184 -191.

[15] F. Ellinger, T. Morf, G. Büren, C. Kromer, G. Sialm, L. Rodoni, M. Schmatz, H. Jäckel, "60 GHz VCO with Wideband Tuning Range Fabricated on BLSI SOI CMOS Technology," *IEEE Microwave Theory and Techniques Symposium Digest*, vol. 3, Jun. 2003, pp1332 -1329.

[16] S. Kudszus, W. H. Haydl, M. Neumann and M. Schlechtweg, "94/47-GHz Regenerative Frequency Divider MMIC with Low Conversion Loss", *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 9, Sept. 2000, pp. 1312-1317.

[17] A. Rylyakov and T. Zwick, "96-GHz Static Frequency Divider in SiGe Bipolar Technology, *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 10, Oct 2004, pp.1712-1715.

[18] A. Dec and K. Suyama, "A 1.9GHz CMOS VCO with Micromachined Electromachined Tunable Capacitors, *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 8, Aug. 2000, pp. 1231-1237.

[19] I. D. Holland, W. G. Cowley, and C. Burnet, "On the Design of Gigabit Indoor Wireless LANs at 60 GHz", in Proc. *Australian Conference on Wireless Broadband and Ultra Wideband Communications*, Sydney, Australia, Mar. 2006, *to appear*.