EFFICIENT TRANSISTOR COUNT REDUCTION FOR A LOW POWER GaAs A/D CONVERTER.


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Abstract

A three bit A/D converter technique, based on the coupled capacitances to the gate of the inverters, has been successfully simulated with SPICE, using complementary HFET technology (complementary GaAs). Due to the gate leakage current of HFETs, a refreshment circuit is required for a proper behaviour. The input frequency is limited up to 1 MHz due to the time required to charge and discharge the capacitances. The counterpart is a drastic reduction in the number of transistors, so as a lower power consumption (0.69 mW) are reliable with respect to other conventional A/D converters. 

1. INTRODUCTION.

The reduction in the number of transistors, as well as interconnections, is one of the most critical issues when implementing digital VLSI designs. On the other hand, analog to digital converters (A/D converters) with high conversion rates and low power dissipation [1-3] are becoming more important for applications such as video-data processing, hard-disk controllers and, in general, any portable application.

A manufacturable complementary technology [4-7], known as complementary GaAs, can offer minimum static power dissipation (only that one due to the gate leakage current), and high speed due to the carriers properties in GaAs.

The concept of Neuron-inverter [8-10] has been applied successfully by the CMOS designers. It is based on coupling capacitances to the gate of the inverter and evaluating the weighted sum of the inputs.

In this paper we apply the similar concepts to the case of a complementary GaAs A/D converter. The main difference with respect to CMOS technology is that the gate leakage current affects the correct evaluation of the analog input signal. A refreshment circuit is necessary for a proper behaviour.

*With C-HPTec, The University of Adelaide, SA 5000, Australia.

Figure 1: Variable threshold voltage inverter

2. COMPLEMENTARY GaAs PARAMETERS.

Due to the proprietary nature of complementary GaAs data and SPICE parameters, this work is based on a realistic composite parameter set derived from a number of vendors [4-7], for a nominal 0.7µ process. This composite parameters is used to gain an appreciation of the functionality of the new neuron-logic technique, in complementary GaAs technology, and only actual fabrication of the circuit can be relied on for determining ultimate performance data. For comparison, the same circuits were also designed in a standard double-poly silicon CMOS process [9].

3. VARIABLE THRESHOLD VOLTAGE INVERTER.

The inverter is based on HFET transistors and resembles CMOS except that three coupled capacitances, and a voltage reference (Vref) are included to the basic inverter, so that the threshold voltage
can be modified (see Figure 1). The coupled capacitance connected to the transistor gates, reduces the internal capacitances influence on the basic inverter. Thereby the weighted sum of the inputs is better evaluated, and the necessary coupled capacitances can be reduced.

If the coupled capacitances are much higher than the internal capacitances, the internal capacitances can be neglected [8] and the gate voltage \( V_g \) can be approximated as:

\[
V_g = \frac{V_{ref} + xV_i}{1 + x}
\]

In the case of \( V_{ref} \) equal to the voltage supply \( (V_{DD}) \), with \( x = 2 \), and taking into account that the threshold voltage of the basic inverter is \( V_{DD}/2 \), the gate voltage \( V_g \) and the threshold voltage \( V_{th} \) of the structure are:

\[
V_g = V_{DD} + 2V_i
\]

\[
V_{th} = \frac{2V_i}{3}
\]

If \( V_{ref} = 0 \), and \( x = 2 \), then the threshold voltage is:

\[
V_{th} = \frac{2V_i}{3}
\]

4. A/D CONVERTER STRUCTURE.

We started applying the A/D converter structure successfully used for the CMOS version [8], to the complementary GaAs technology. But the behaviour is degraded after a short time, in the order of 8 ns.

As opposed to CMOS technology, the gate leakage current of HFETs can not be neglected. It alters the charge of the coupled capacitances and, therefore, the correct evaluation of the input signals. In order to avoid the degradation of the converter behaviour, a refreshment circuit is required.

The three bits A/D converter under study, with the refreshment circuit, is shown in Figure 2. With the considerations mentioned above, the inverters with threshold voltages \( V_{DD}/4 \), and \( 3V_{DD}/4 \) (inverters 1/4 and 3/4 respectively), are implemented as in Figure 3. The input signals, \( V_{in\ up} \) and \( V_{in\ down} \), are necessary for refreshment (see Figure 4).

Because of the coupled capacitances associated with the inverters, only 52 transistors are enough to implement the A/D converter.

4.1 Design considerations.

The selected voltage supply, \( V_{DD} \), is 1.6 V. With this value, it is unnecessary to scale the transistor widths in order to fix the threshold voltage to \( V_{DD}/2 \).

The low output voltage is set to ground and the high output voltage is set to \( V_{DD} \) ("0" and "1" logic values).

For higher voltage supplies, the inverter 3/4 does not invert properly. On the other hand, with lower voltage supplies, the product power-delay increases...
and it is more difficult to adjust the capacitances for a correct behaviour.

The internal connections (see * in Figure 2) to the capacitances have been avoided, adding two more inverters and the input signal $V^*_{in\,down}$. In this way, there are three independent stages (one for every output), wherein there is no mutual influence when charging or discharging their associated coupled capacitances. A better response is obtained for the outputs and the delay is also reduced.

A simple design is possible when the coupled capacitances are much higher than the internal ones of the inverter. In that way the internal capacitances can be neglected but, on the other hand, high capacitance values increase the delay and area of the circuit. For an input signal frequency of 0.5 MHz, the maximum capacitance in the converter is 5 pF, located in Neuron.0.

4.2 Basic principles of conversion.

Applying the capacitive voltage dividing principle [8], the output signals for the least significative bits, $A_6$ and $A_1$, can be obtained. If the ratio of the capacitances are like in Figure 2, when the input signal is evaluated, the gate voltage for Neuron.0 can be approximated as:

$$V_g = \frac{4V_{in\,down} + V_{1/4} + V_{3/4}}{7}$$

where $V_{1/4}$, $V_{3/4}$, $V_{2\,in\,down}$ are the outputs of the variable threshold voltage inverters respectively.

In the case of Neuron.1, when the input signal is evaluated, the gate voltage is:

$$V_g = \frac{2V_{in\,down} + V_{1/4}}{3}$$

If the input signal varies linearly from zero to the $V_{DD}$ voltage supply, the theoretical gate voltages for Neuron.0 and Neuron.1 are shown in Figure 5. Only one basic inverter, connected to the Neuron.0 and Neuron.1 outputs, is necessary to produce the output logic values $A_6$ and $A_1$ respectively.

The most significative bit, $A_6$, is implemented with only two basic inverters connected to the input signal.

It should be noticed that this technique can be easily extended to a larger bit-number A/D converter.

4.3 Refreshment circuit.

The basic idea to refresh circuit is to discharge the coupled capacitances before the input signal is going to be evaluated. In order to discharge them, when the clock signal is low, the gate and input connections of the coupled capacitances are connected to the same voltage source.

For Neuron.0 and Neuron.1, the voltage source selected is ground. Therefore, when the coupled capacitances are discharged, the outputs $A_6$ or $A_1$ does not change if its previous value was "0".

In the case of the variable threshold voltage inverters, the voltage source of discharging must be the voltage supply. In this way there is no conflict between the outputs of the inverters $1/4$ and $3/4$, and the inputs of Neuron.0. When the clock signal is low, the coupled capacitances of the inverters $1/4$ and $3/4$ are discharged to $V_{DD}$; the outputs of these inverters are low and therefore, the coupled capacitances of Neuron.0 can be discharged to ground.

These two types of refreshment make necessary the use of the two sampled input signals $V_{in\,down}$ and $V_{in\,up}$ (see Figure 4). $V_{in\,down}$ resets the input signal to ground, and it is used to refresh the coupled capacitances of Neuron.0 and Neuron.1. On the other hand, $V_{in\,up}$ resets the input signal to $V_{DD}$, necessary for the capacitances of the inverters $1/4$ and $3/4$.

Due to the refreshment circuit, the degradation is avoided. With the two refreshment sources, when the input signal is evaluated, there are no peak voltages during any transition in the capacitors. Thus, it is not necessary any additional circuit (e.g. flip-flops) to evaluate properly the outputs of the converter.

![Figure 5: Theoretical gate voltage in Neuron.0 and Neuron.1.](image5)

![Figure 6: Switches implementation.](image6)
necessary if two signals are alternatively evaluated. The pass-gate is implemented with two transistors (N and P) connected in parallel. When the coupled capacitances technique is used, this refinement implementation can be easily extended to more complex circuits.

5. RESULTS.

The output signals, when the analog input signal varies linearly at the frequency of 0.5 MHz, are shown in Figure 7. The clock signal frequency is 25 MHz (it could be increased until 40 MHz without degrading the behaviour).

In order to get a better definition, two buffers are located at the outputs of Neuron.0 and Neuron.1.

With respect to the capacitances, if their values decrease, it is more difficult to design properly the neuron structures and the variable threshold voltage inverters. When the capacitances are very low, it is not possible the conversion of the analog input signal.

The circuit response is very sensitive for high frequencies (this is also observed with CMOS-neuron technology). Above 1 MHz the capacitances have not enough time for charging and discharging, hence the behaviour starts degrading.

The power consumption increases with the input signal frequency. It was observed a power consumption as low as the CMOS A/D converter version [8], for an input signal frequency of 0.5 MHz.

The maximum delay in the converter is produced in the A. output. It is also comparable with the delay in the CMOS version. This is because the delay is produced mainly due to the charge and discharge of the capacitors.

Comparison of the power consumption, maximum delay and number of transistors in the A/D converter, with respect to other technologies and techniques, is shown in Table 1.

CMOS-neuron is the CMOS version of the converter under study (complementary GaAs-neuron). Complementary GaAs-flash is a flash A/D converter simulated with the complementary GaAs technology. Finally CMOS-flash is a CMOS flash A/D converter that uses the switched capacitors technique for the comparators (the power dissipation of 7.4 mW in Table 1, is only that one to the comparators).

The delay in the neuron converters is a little higher than the flash ones, mainly due to the charge and discharge processes of the capacitors. High reductions of the number of transistors and the power dissipation for the neuron converters are also observed.

The flash converters are necessary when the input signal frequency is high. A frequency of 7 MHz is reliable with the CMOS-flash converter [1], and for the complementary GaAs-flash converter 10 MHz was successfully simulated. In the converter under study, the complementary GaAs-neuron, for a frequency of 0.5 MHz there is a correct conversion and it starts to fail when the input signal frequency is about 1 MHz.

### Table 1: Results for different technologies.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Power, P(mW)</th>
<th>Delay, d(ps)</th>
<th>Transistors, N</th>
<th>Freq. (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>complementary GaAs-neuron</td>
<td>0.69</td>
<td>7000</td>
<td>52</td>
<td>0.5</td>
</tr>
<tr>
<td>CMOS-neuron [8]</td>
<td>0.51</td>
<td>7050</td>
<td>18</td>
<td>0.5</td>
</tr>
<tr>
<td>complementary GaAs-flash</td>
<td>50</td>
<td>1800</td>
<td>237</td>
<td>10</td>
</tr>
<tr>
<td>CMOS-flash [1]</td>
<td>&gt; 7.4 (25 Msamples/sec)</td>
<td>300</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>

### Table 2: Functionality transistors distribution.

- **A/D converter**: 20
- **Refreshment**: 24
- **Buffers**: 8

Table 2 shows the transistors distribution and their...
respective function in the A/D converter. Only for the refreshment circuit as many transistors as for the conversion function were needed. Furthermore, four inverters were used to implement the buffers. In spite of these requirements, there is still a drastic reduction in the number of transistors with respect to other conventional structures.

6. CONCLUSIONS.

An A/D converter based on coupled capacitances and complementary GaAs technology has been proposed and simulated. A high reduction in the number of transistors is possible with respect to other conventional designs, and similar response to the CMOS version.

When the input signal is not very fast (up to 1 MHz), it is an attractive choice in terms of area (52 transistors and a maximum capacitance of 5 pF), and low power consumption (0.69 mW).

A refreshment circuit has been necessary to avoid the degradation due to the gate leakage current. As the leakage current can be reduced, as the capacitances will be smaller and probably the properties of GaAs carriers will lead to a faster response than the CMOS version.

The use of this technique together with HFET technologies, opens new avenues in the design of high performance VLSI systems, in which delay, power and area must be balanced altogether in order to obtain superior characteristics than their counterparts in Silicon.

References


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