Neu-MOS (νMOS) for Smart Sensors and Extension to a Novel Neu-GaAs (νGaAs) Paradigm (Invited)

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Abstract

The neu-MOS (νMOS) transistor is a new device that enables the design of conventional digital and analog circuits, in standard CMOS, with a factor of 5-10 decrease gate count. Furthermore, νMOS circuit characteristics are insensitive to transistor parameter variations but instead rely on coupling capacitor *ratios*. In this paper, we demonstrate this principle with results from fabricated controlled gain amplifiers. This new technology is ideal for smart sensors where a high functionality per pixel area and good matching between pixels is required. Moreover, we discuss the advantages of smart sensors in GaAs technology and the viability of developing a νGaAs paradigm.

1 Introduction

The neu-MOS (νMOS) transistor, recently discovered by Shibata and Ohmi [1] in 1991, simply uses capacitively coupled inputs onto a floating gate. The resulting output is simply a weighted sum of the inputs, due to the capacitive input network, followed by a thresholding operation. The behaviour of the transistor resembles, very well, that of a biological neuron where the turn-on of the transistor is parallelled by the firing of a neuron. In this respect, the device is called a neuron MOSFET or a neu-MOS (νMOS) for short. The structure, the symbol and the capacitance representation of the νMOS transistor are shown in Fig. 1.a-c. νMOS circuits operate with mixed mode analog/digital functions and can even perform Boolean logical operations that are dynamically reconfigurable. The use of νMOS circuits will greatly increase functionality/area [2] while still maintaining low cost via the use of standard CMOS fabrication. In addition to neural networks the application areas were νMOS will have use are motion detectors [3, 4, 5], monolithic imaging/compression [6], spatial light modulators (SLMs) and optical neural arrays [7].

For instance the same gate can perform the function of *AND*, *OR* and *XOR* depending on the state of an input control signal [8]. This new paradigm of 'soft' hardware is referred to as *flexware*. Consequently, νMOS has been successfully employed in a number of digital architectures with a dramatic saving in silicon area. It has been reported that the area of a νMOS multiplier with full-adders decreases to about 65% of the area of CMOS, and the delay of a νMOS multiplier with (7,3) parallel counters decreases to about 70% of the delay of its CMOS equivalent [2].

An important feature to note is that a νMOS implementation only requires a *conventional* double polysilicon CMOS process and therefore is a readily accessible technology. Consequently, νMOS is a low-cost method for increasing the functionality per unit silicon area. Other schemes to increase functionality/area are generally esoteric and expensive [9].

In the literature, most νMOS circuits have employed digital inputs [10], however a few groups have explored analog νMOS techniques [11, 12]. In this paper new analog circuits built using νMOS transistor are discussed. Section 2 will discuss briefly the key design parameters for the νMOS transistor. Section 3 will discuss the design of controlled gain amplifier circuits in which gain is controlled by capacitor ratio rather than depending on process parameters.

The smart sensor paradigm requires process-

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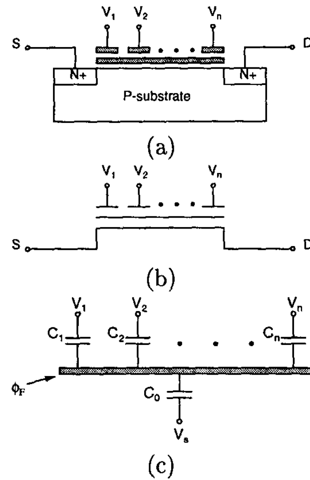


Figure 1: (a) The basic structure of an n-νMOS transistor, (b) its electronic symbol. (c) Capacitance representation of the νMOS, where C_0 is the sum of all the parasitic capacitances from the floating gate to the substrate including the floating gate to source.

ing to take place at every pixel. With increasing demands on at-pixel processing, such as in mobile video communications (eg. the IM^{3}PC paradigm [13]), and with good pixel-to-pixel matching required for minimal fixed-pattern-noise, the νMOS technology offers an ideal solution. With νMOS, greater processing functionality at each pixel becomes possible and better matching is achieved as νMOS relies on controlled capacitor ratios, thus reducing problems due to transistor parameter spreads. Furthermore, we shall discuss the advantages of using GaAs for smart sensors and hence, for the first time, we will comment on the feasibility of a novel νGaAs paradigm.

Due to the greater functionality per unit area, available in νGaAs, interconnect lengths are also greatly reduced as a by-product of this methodology. Hence, νMOS is very promising as a low power technology which is attractive for smart sensors in mobile applications.

2 Key Design Parameters for the νMOS Transistor

This section will identify some of the main key design parameters that can be used in designing analog and digital circuitry using νMOS transistor.

- **Floating-Gate Gain Factor, γ**

  The first design parameter to be considered is the floating-gate gain factor, γ, which is defined as

$$\gamma = \frac{C_1 + C_2 + \ldots + C_n}{C_{TOT}} = \frac{C_{TOT} - C_0}{C_{TOT}} \quad (1)$$

  The product of γ and V_{DD} represents the maximum floating-gate voltage obtained when all input gates are at V_{DD}. In the above equation C_0 can vary depending on the operating condition of the transistor. However, it can be approximated by the gate oxide capacitance when the device is 'ON' and can be regarded as a constant as long as the channel is formed [14]. The value of γ can be maximised by increasing $\sum_{k=1}^{n} C_i$ compared to C_0. However, this would increase the size of the circuit and it should be considered as a trade-off.

- **Threshold Voltage Seen from the Floating Gate, V_{TH}^***

  The second key design parameter is V_{TH}^*, which is the threshold voltage of the transistor seen from the floating gate. V_{TH}^* represents the boundary between the 'ON' and 'OFF' states of the transistor. So, for the transistor to turn 'ON', the following condition should be satisfied

$$\frac{C_1 V_1 + C_2 V_2 + \ldots + C_n V_n}{C_{TOT}} > V_{TH}^*. \quad (2)$$

  Equation 2 states that when the linear weighted sum of all input signals exceeds a certain threshold value V_{TH}^*, the transistor turns 'ON.' V_{TH}^* is one of the main design parameters of the νMOS transistor.

- **Floating Gate Offset Voltage, ϕ_F**

  A shift or an offset on the floating gate voltage can be a result of two separate effects. The first is due to an initial charge on the floating gate that is trapped on the floating gate during the fabrication process. The magnitude of such shift can be as large as ± 200 mV [12]. A number of methods can be used to reduce this effect. The first is to shine UV light on the transistor while all terminals are grounded. This will excite some electrons to energy states above the conduction band of the oxide layer, resulting in an increase in the oxide layer conductance, allowing the discharge of the floating gate until its potential is the same as ground [12]. The second method is to inject some charge carriers to the floating gate. *ie.* programming the floating gate using Fowler-Nordheim tunnelling effect [15]. The third method is to electronically initialise the floating gate charge by connecting the floating gate to a predefined voltage. Such method is actually used in [16, 17, 18] to initialise the floating gate potential.

  The second effect that might cause shift in the floating gate potential is the gate to drain capacitance, C_{gd}, as a result of feedback from the drain to νMOS floating gate. This capacitance will have effect when the νMOS transistor is operating in the linear region of operation [14]. The

effect of such capacitance can be reduced by using minimum size νMOS transistor and maximising the ratio of $\sum_{i=1}^{n} C_i V_i$ to $C_{gd}V_{ds}$. Where V_{ds} is the drain to source voltage of the νMOS transistor.

3 Controlled Gain Amplifiers

This section describes the design of a controlled gain amplifier using νMOS transistor, where the gain of the amplifier is controlled through capacitor ratio instead of transistor size ratio. The amplifier design is based on the linear grounded resistor discussed in [1]. Later in this section, another approach to the amplifier design using a 'neuron-inverter' (νCMOS inverter) will be discussed. It will be shown that both approaches give the same results.

The first approach is to use two grounded resistors, one using n-νMOS, while the other using p-νMOS and connected as shown in Fig. 2.a. The gain of the amplifier circuit can be found analytically by writing the current equations of the n- and p-νMOS transistors as follows

$$I_n = \frac{\beta_n}{2}(W_{in_n} V_{in} + W_{o_n} + V_{gg} - V_{t_n})^2 \tag{3}$$

$$I_p = \frac{\beta_p}{2}(V_{dd} - W_{in_p} V_{in} - W_{o_p} V_o - V_{gg} + V_{t_p})^2 \tag{4}$$

where

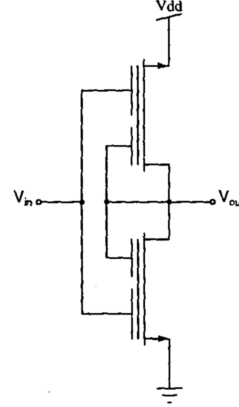
- I_n, I_p are n- and p-MOS drain currents;
- β_n, β_p are n- and p-MOS gain factors;
- W_{in_k} is the ratio of the input coupling capacitance of transistor type k, C_{in_k}, to the total capacitances at that transistor, C_{TOT_k}. *ie.* $W_{in_n} = \frac{C_{in_n}}{C_{TOT_n}}$ and $W_{in_p} = \frac{C_{in_p}}{C_{TOT_p}}$;
- W_{o_k} is ratio of the output to input coupling capacitance of transistor type k, C_{o_k}, to the total capacitance at that transistor, C_{TOT_k}. *ie.* $W_{o_n} = \frac{C_{o_n}}{C_{TOT_n}}$ and $W_{o_p} = \frac{C_{o_p}}{C_{TOT_p}}$;
- V_o is the output voltage on the amplifier;
- V_{gg} is the initial voltage at the floating gate;
- V_{dd} is the supply voltage;
- V_{t_k} is the threshold voltages of transistor type k.

Solving Equations 3 and 4 for V_o results in

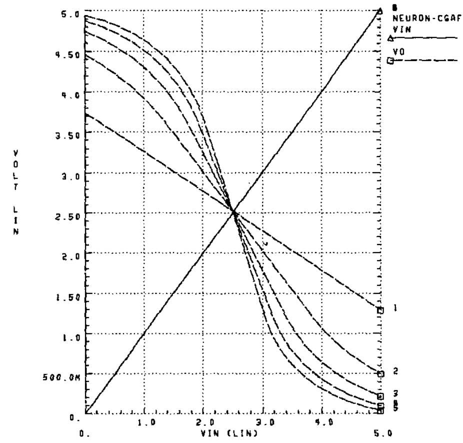
$$V_o = -\frac{\sqrt{\frac{\beta_n}{\beta_p}} W_{in_n} + W_{in_p}}{\sqrt{\frac{\beta_n}{\beta_p}} W_{o_n} + W_{o_p}} V_{in} - \frac{\sqrt{\frac{\beta_n}{\beta_p}} + 1}{\sqrt{\frac{\beta_n}{\beta_p}} W_{o_n} + W_{o_p}} V_{gg} + \frac{V_{dd} + V_{t_n}\sqrt{\frac{\beta_n}{\beta_p}} + V_{t_p}}{\sqrt{\frac{\beta_n}{\beta_p}} W_{o_n} + W_{o_p}} \tag{5}$$

Equation 5 can be simplified by setting $\beta_n = \beta_p$, $V_{t_n} = V_{t_p}$, $W_{in_n} = W_{in_p} = W_{in}/2$, $W_{o_n} = W_{o_p} = W_o/2$ and $V_{gg} = V_{dd}/2$, to

$$V_o = -\frac{C_{in}}{C_o} V_{in} \tag{6}$$



(a)



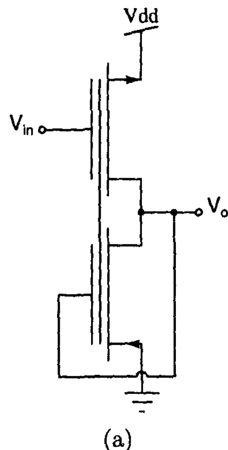
(b)

Figure 2: (a) A controlled gain amplifier circuit designed using linear grounded resistors. (b) The simulated input-output characteristics of the controlled gain amplifier shown in (a).

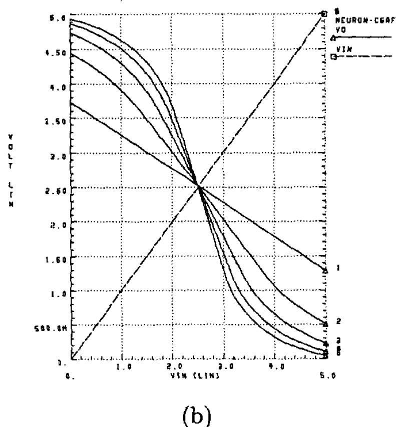
The above equation shows that the amplifier gain is purely a function of the capacitor ratio and it is independent of process parameters and the supply voltage. To confirm Equation 6, the amplifier circuit was simulated with $C_o = 10$ pF while C_{in} was swept from 5 pF to 25 pF in 5 pF steps. The simulation results are shown in Fig. 2.b.

The second approach to the design of a controlled gain amplifier is to use 'νCMOS inverter,' which is simply a normal digital inverter that has N input terminals capacitively coupled to its gate. For the amplifier design a dual input 'neuron inverter' is used with one of the input terminals connected to the output of the inverter, while the other terminal is used as an input terminal, as shown in Fig. 3.a. Once such a connection is made, the functionality of the circuit will be completely different from the 'neuron inverter,' [1]

as in the case the 'neuron inverter' the output signal is a digital state of either '1' or '0.' While using this configuration the circuit will act as an amplifier.



(a)



(b)

Figure 3: (a) A schematic diagram of a controlled gain amplifier using νMOS transistor. (b) The simulation results of relationship between the output voltage, V_o, and the input voltage, V_{in}, of the controlled gain amplifier circuit with input coupling capacitor, C_{in}, swept from 10 pF to 50 pF with 10 pF increment, while C_o was fixed at 20 pF.

The gain of the amplifier can be calculated by writing the current equations of the p-νMOS and n-νMOS transistors using a simple transistor model in the saturation region as follows

$$I_n = \frac{\beta_n}{2}(W_{in}V_{in} + W_oV_o + V_{gg} - V_{t_n})^2 \quad (7)$$

$$I_p = \frac{\beta_n}{2}(V_{dd} - W_{in}V_{in} - W_oV_o - V_{gg} + V_{t_p})^2 \quad (8)$$

where

W_{in} is ratio of i/p coupling cap., C_{in}, to total capacitance, C_{TOT};

W_o is ratio of o/p to i/p coupling cap., C_o, to total capacitance, C_{TOT}.

Solving Equations 7 and 8 for V_o gives

$$V_o = -\frac{W_{in}}{W_o}V_{in} - \frac{V_{gg}}{W_o} + \frac{V_{dd} + V_{t_n}\sqrt{\frac{\beta_n}{\beta_p}} + V_{t_p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad (9)$$

The above equation can be simplified by letting $\beta_n = \beta_p$, $V_{t_n} = V_{t_p}$ and $V_{gg} = V_{dd}/2$, resulting in

$$V_o = -\frac{C_{in}}{C_o}V_{in} \quad (10)$$

From the above first order analysis, it can be seen that the gain is also function of the of the ratio of C_{in}/C_o and independent of the process parameters and the supply voltage. The simulation results of the amplifier with C_{in} swept from 5 pF to 25 pF in 5 pF steps, while assuming that $\beta_n = \beta_p$ and $V_{t_n} = V_{t_p}$, are shown in Fig. 3.b.

An interesting feature of the above circuits can be obtained by taking the special case when $C_{in} = C_o$, this will result in an inverting analog buffer circuit with linearity completely independent of the transistor parameters and purely function of the capacitor ratios.

Measurements results for a 6 dB neuron-MOS-amplifier circuit designed based on the above analysis will be presented in the conference. The amplifier is implemented in a 1.2 μm double poly, double metal CMOS process.

4 GaAs for Smart Sensors

A number of physical and optoelectronic properties of GaAs make it a highly suitable medium for optical smart sensors. In this section, these properties are discussed with a view to smart image sensors (a) in a stand-alone context and (b) in the context of spatial light modulators (SLMs). After establishing that GaAs is indeed advantageous for smart sensors, we then go onto discuss the possibility of a new neu-GaAs (νGaAs) paradigm and discuss the most suitable GaAs technology to achieve this.

The motivation to explore smart sensors in GaAs technology arises from the fact that (a) the optical absorption coefficients in GaAs are such that light is absorbed 10 times closer to the surface, than in silicon, resulting in more efficient photocollection and tighter control over optical overload (blooming) [19] (b) the diffusion lengths in SI GaAs are over an order of magnitude shorter than in silicon, resulting in improved spatial resolution, showing promise for HDTV applications [20] (c) GaAs has superior dark current characteristics, as evidenced by the successful realisation room temperature GaAs X-ray detectors [21] and (d) there is promise of integration of high-speed processing (eg. image compression) on the same chip as the sensor.

This section demonstrates the superiority of GaAs in all areas over silicon, but reveals that shot noise degradation is the main area of weakness for MESFET technology. However, newly emerging GaAs technologies such as HIGFETs [22], anisotype FETs [23] and

MOS-GaAs [24] are discussed, showing promising results.

4.1 GaAs Smart Image Sensors

In this context, the 'smart sensor' paradigm implies the integration of processing circuitry (eg. for image compression) with the image sensor. The superior power-delay product of GaAs becomes ideal for such high-speed processing in real-time. Such integration rules out the possibility of using a CCD process – CCD technology cannot support conventional digital circuits. Therefore, such a GaAs image sensor must use a standard or near-standard VLSI GaAs technology. The type of imager in this technology uses an XY addressable array of transistors as shown in Fig. 4.

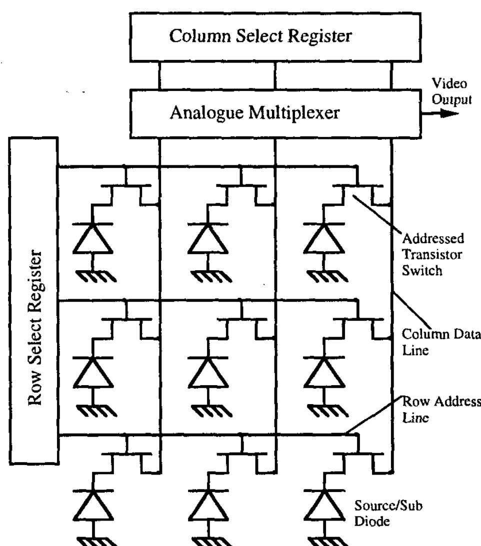


Figure 4: XY Array imager architecture – charge sensing approach.

There are two methods of readout: (a) charge sensing and (b) voltage sensing. In a voltage sensing approach, signal charge is converted to a voltage at each pixel node. As the conversion capacitance at each pixel is small, this results in reduced kTC noise and hence improved dynamic range. However, the downside is that capacitor and source follower mismatching between pixels lead to high fixed pattern noise (fpn).

In the charge sensing approach, this source of fpn is eliminated by dumping the charge from each pixel on to the output node. In this way, charge-to-voltage conversion occurs at the final output – thus only one source follower is required at the output. Due to the architecture of the array a large output node capacitance is unavoidable, leading to increased kTC noise and reduced dynamic range.

However, due to the semi-insulating (SI) substrate, capacitances are reduced making the *charge sensing* XY array, in Fig. 4, the best choice in GaAs.

Further advantages with the shift to GaAs, as outlined in Sec. 5, include shallow optical absorption lengths and small carrier diffusion lengths. The superiority of the GaAs over silicon, in terms of absorption length, is illustrated in Fig. 5. As can be seen, light is absorbed about ten times closer to the surface in GaAs than in silicon. This implies tighter control over blooming, increased photocollection efficiency and greater spatial resolution.

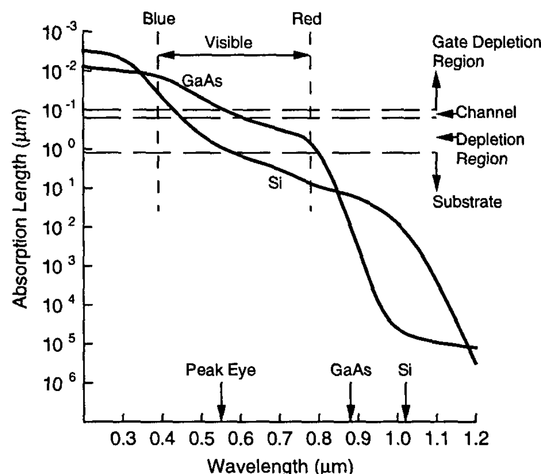


Figure 5: GaAs v. silicon absorption length

It can be estimated [20] that the carrier diffusion length is $<10\mu m$. This is much smaller than in CMOS where minority carrier diffusion lengths are in the 200-$400\mu m$ range. The implication of short diffusion length together with shallow absorption length is excellent spatial resolution for HDTV applications [25]. However, in practice, for silicon imagers, good spatial resolution is obtained at the expense of responsivity, by use of a thin epi layer. Therefore in practice, with GaAs, improved spatial resolution translates into improved responsivity over silicon, as the epitaxial approach can be dispensed with. This improved responsivity impacts not only on GaAs HDTV sensors, but on the GaAs smart sensors discussed herein.

4.2 GaAs Spatial Light Modulators (SLMs)

SLMs are basically 2-D arrays that output image patterns reflectively (eg. via Ferroelectric Liquid Crystal or FLC) or directly (eg. a micro-array of LEDs or a VCSEL). These light patterns can be modulated either electrically (ie. an electrically addressable SLM or EASLM) or optically (ie. an optically addressable SLM or OASLM). Thus these devices essentially perform smart optical spatial filtering functions.

The EASLM can consist of an array of smart pixels sandwiched to either a LED or FLC display device. Further to this, the OASLM utilises a smart image sensor for optical addressing.

GaAs offers two significant possibilities: an LED/-GaAs, Fig. 6, or an FLC/GaAs, Fig. 7, architecture. The advantages of GaAs are numerous. Firstly the

larger absorption coefficient in GaAs leads to improved optical addressing characteristics [19]. Secondly, FLC technology is sensitive to surface planarity and wafer warp as little as 1 μm – GaAs offers excellent planarity due to the absence of field oxide steps and a warp of less than 0.5 μm has been achieved. In silicon, for typical devices, the warp is greater than 1 μm leading to critical non-uniformities in the FLC layer. GaAs also offers the potential to move away from LC technology altogether as LED arrays can be monolithically integrated [26]. With the emergence of low-power complementary GaAs, already available with VLSI maturity, the traditional problems with power dissipation are no longer of concern. Other advantages of GaAs include no latchup, fewer masking layers (simpler) and existing techniques for through-substrate-vias (this has implications for future 3-D mounted SLMs).

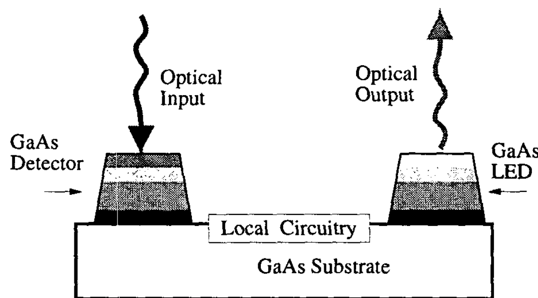


Figure 6: A LED/GaAs smart pixel

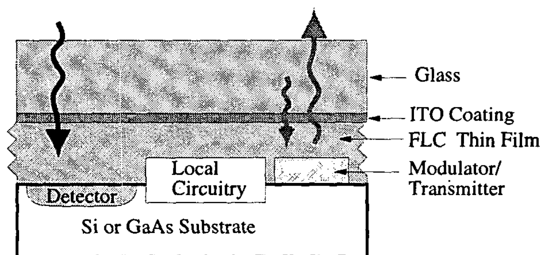


Figure 7: A FLC/Si or FLC/GaAs smart pixel

GaAs has a number of advantages with respect to the smart pixel concept. Firstly in order to enable optical input, a 2D image sensor must be vertically stacked with parallel connections to the display device using, for example, flip-chip techniques. Fortunately, the GaAs crystal has excellent crystal properties enabling etching of through-substrate-vias with relative ease and this is a known technique in GaAs MMICs that use vertical connections to a backside groundplane. Smart pixel functions can be embedded either in the sensor or display device or both.

Another feature of GaAs is that wafer warp across a chip is superior to silicon and <1 μm. Silicon has the disadvantage that a warp >1 μm degrades the performance of the FLC display, creating a deleterious dispersion in phase across the area of the device. The digital GaAs process is also intrinsically more planar than CMOS (eg. no field oxide) and therefore variations in FLC thickness are further reduced.

Due to the improved power-delay product of GaAs over silicon, either throughput rate can be increased or, for the same speed, power dissipation is reduced. This becomes important for stacked devices as greater care over thermal management is required.

5 Choice of GaAs Technology

We have shown [27] that shot noise dominates the noise of the output circuit of a smart sensor array based on GaAs MESFET technology. Unfortunately it is impossible to remove shot noise by correlated double sampling. This means that the circuit cannot be optimised for this MESFET technology. The source of this shot noise is the high gate leakage current in MESFETs, which also makes the realisation of νGaAs circuits impossible due to the consequent rapid discharging of the various coupling capacitors.

In the longer term, two emerging GaAs technologies are promising: the HIGFET and the anisotype FET. The HIGFET [23] uses a semi-insulating AlGaAs layer in the gate to reduce leakage currents. The anisotype FET [22] uses a graded semiconductor InGaAs/GaAs layer in the gate, producing yet a further improvement in gate leakage.

Recently Lucent have announced a true MOS-GaAs [24], using a mixture of gallium oxide and gadolinium oxide $Ga_2O_3(Gd_2O_3)$. If oxide stability and high integration levels are eventually proven, this will be the ideal medium for the GaAs smart sensors based on νGaAs.

However, in the immediate short term, complementary GaAs based on HIGFET transistors appears to be the most viable option for νGaAs smart sensors in terms of maturity, low power performance and tolerable gate leakage levels. We have performed some initial complementary HIGFET simulations based on a realistic composite parameter set derived from a number of complementary GaAs processes. These include Honeywell [28], Sandia [29], Univ. Lille [30], Fujitsu [31] and MIT [32]. Although this parameter set is contrived, our approach be to adjust the parameters (esp. gate leakage) to produce the optimum νGaAs performance. In this way we 'reverse engineer' the expected complementary HIGFET parameter set for best νGaAs performance. Then this information will help to select the best HIGFET vendor for νGaAs. At this stage νGaAs simulations are somewhat hypothetical, as convenient capacitors do not exist – whereas in MOS the coupling capacitors are conveniently provided by the poly1 to poly2 overlap. However, in principle, it would be relatively simple to add a special high capacitance MIM layer to existing HIGFET processes. Justification of this would not be solely based on νGaAs, but would also be for RF circuits in instances where complementary GaAs is used in mixed RF/digital applications. This would be particularly pertinent in mobile multimedia systems that use both smart sensors and

RF wireless communications. Preliminary simulations demonstrate functional νGaAs 3-bit A/D converters with a factor of 4 reduction in gate count and power dissipation reduction over a factor of 50 over conventional complementary GaAs layouts.

6 Conclusion

The Neuron MOS transistor has been used extensively in the design of digital circuitry, however, the use of such a transistor in analog design has not been fully investigated. In this paper a number of key design parameters for analog and digital circuits have been identified. The analog examples designed and discussed in this paper and based on these key design parameters are meant to demonstrate that the νMOS transistor can be used to design useful analog circuitry. This was demonstrated through the design of controlled gain amplifiers. These circuits have gain that is independent of the process parameters and also independent of the supply voltage. The designed circuits represent good candidates for basic building blocks in analog signal processing and in the smart pixel environment. Moreover, we have discussed a number of advantages of the GaAs technology for smart sensors and have indicated that the complementary GaAs technology based on HIGFETs is the most promising approach for future νGaAs circuits.

In conclusion, νMOS transistor can be used successfully in designing useful analog building blocks and has the potential to provide low power circuitry because the input signals are capacitively coupled to the floating gates which are of small area. Moreover, as the functionality per unit area increases, this would enable the design of systems with complex functions with smaller silicon area compared to traditional MOS circuitry, and hence provide a step forward toward pseudo ULSI integration density.

7 Acknowledgement

The authors would like to thank The Computer Vision Group in the The Centre for High Performance Integrated Technologies & Systems (CHiPTec) for including test module fabrications as part of their system. Funding from the Australian Research Council (ARC) is greatfully acknowledged.

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