Pairing Frequency Experiments in Visual Cortex Reproduced in a Neuromorphic STDP Circuit

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***Abstract*— Previous studies show that the conventional pair-based form of STDP (PSTDP), is not able to account for many biological experiments including frequency-dependent pairing experiments performed in the visual cortex region of the brain. However, new improved synaptic plasticity rules, such as Triplet-based Spike Timing Dependent Plasticity (TSTDP), are capable of replicating many biological experiments outcomes including the results of the experiments carried out in the visual cortex. This paper proposes a programmable analog neuromorphic circuit, which is capable of reproducing pairing frequency experiments in the visual cortex. The circuit utilizes transistors working in their subthreshold region of operation. In addition, it implements a minimal model TSTDP learning rule, which needs a low number of transistors compared to its PSTDP circuit counterparts. These features result in low-power compact circuits that are suitable for large-scale VLSI implementations of Spiking Neural Networks (SNNs) with improved synaptic plasticity and learning capabilities.**

I. Introduction

Spike Timing Dependent Plasticity (STDP) is the most recognized learning algorithm in VLSI studies of Spiking Neural Networks (SNN). The conventional form of STDP, which alters the synaptic weights according to the timing differences between pairs of pre- and post-synaptic spikes, has been extensively investigated in many VLSI studies [1]–[3]. In its pair-based form, STDP is able to reproduce the fundamental weight change window that has been experimentally verified [4], [5]. However, the main shortcoming of the PSTDP rule, is its inability to account for a range of STDP behavior. For this reason, other implementations of synaptic plasticity rules are proposed to provide a more accurate representation of the relevant biological behavior [3].

In order to better reproduce the outcomes of multiple biological experiments, in addition to spike timings, recent synaptic plasticity rules considered other synaptic and neural variables such as membrane potential, post-synaptic spiking frequency, and calcium ion concentration, in their plasticity mechanisms [3], [6]. The VLSI implementation of these new rules becomes challenging, due to the inclusion of these additional variables in silicon. A synaptic plasticity model, which alters the synaptic weight based only on the timing of spikes, with the ability to reproduce a diverse range of biological behaviors relies on the triplet-based STDP (TSTDP) rule proposed by Pfister and Gerstner in 2006 [7]. This rule can be easily implemented in VLSI and does not require complex circuitry to deal with complex ionic dynamics present in more complex synaptic plasticity rules, while possessing almost similar capabilities to these rules [7]. This paper proposes a simple yet compact analog circuit for a minimal version of TSTDP rule. Simulation results of the circuit demonstrate its ability in reproducing complex biological behaviors, where PSTDP circuits fail.

The remainder of the paper is organized as follows. Section II gives an introduction on the PSTDP model and discusses a previous PSTDP VLSI implementation. Section III reviews the TSTDP model and introduces the proposed circuit for a minimal version of TSTDP. Simulation results of both PSTDP and TSTDP circuits are presented in Section IV and the results were compared to experimental data. Section V gives the concluding remarks of this paper.

II. Pair-based STDP

A mathematical representation of the pair-based STDP (PSTDP) rule [5] is expressed as

$$\Delta w = \begin{cases} \Delta w^+ = A^+ \exp\left(\frac{-\Delta t}{\tau_+}\right) & \text{if } \Delta t > 0 \\ \Delta w^- = -A^- \exp\left(\frac{\Delta t}{\tau_-}\right) & \text{if } \Delta t \leq 0, \end{cases} \quad (1)$$

where $\Delta t = t_{\text{post}} - t_{\text{pre}}$ is the timing difference between a single pair of pre- and post-synaptic spikes. According to this model, the synaptic weight will be potentiated if a pre-synaptic spike arrives in a specified time window (τ_+) before the occurrence of a post-synaptic spike. Analogously, depression will occur if a pre-synaptic spike occurs within a time window (τ_-) after the post-synaptic spike. The amount of potentiation/depression will be determined as a function of the timing difference between pre- and post-synaptic spikes, their temporal order, and their relevant amplitude parameters (A^+ and A^-).

Due to its simplicity, the PSTDP rule has been implemented by many neuromorphic researchers [1]–[3]. One of the simple implementations for the PSTDP rule is the subthreshold VLSI circuit proposed by Indiveri *et al.* [2]. This symmetric circuit has two potentiation and depression transistor branches as shown in Fig. 1. The upper branch results in charging the weight capacitor, if a pre-synaptic spike precedes a post-synaptic one in a determined time, and the bottom branch is for discharging the capacitor if the reverse spike order occurs. The potentiation and depression timings in this design are set by two leaky integrators, in which their decays are set by two bias voltages, V_{tp} and V_{td}, for potentiation and depression time

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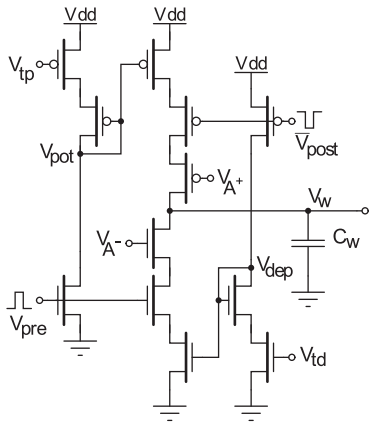

Fig. 1. Pair-based STDP circuit presented in [2].

constants respectively. In addition, the amplitude of the potentiation and depression are set by V_{A^+} and V_{A^-}, respectively. Therefore, a simple design strategy has been used, in order to design the PSTDP circuit according to the rule given in Eq. 1. A similar design methodology has been utilized to implement the proposed TSTDP rule described in the following Section.

III. Triplet-based STDP

In this model of synaptic plasticity, changes to synaptic weight are based on the timing differences among a triplet combination of spikes [7], [8]. This rule uses higher order temporal patterns of spikes to modify the weights of synapses. Triplet STDP (TSTDP) is described by

$$\Delta w = \begin{cases} \Delta w^+ = \exp\left(\frac{-\Delta t_1}{\tau_+}\right)\left(A_2^+ + A_3^+ \exp\left(\frac{-\Delta t_2}{\tau_y}\right)\right) \\ \Delta w^- = -\exp\left(\frac{\Delta t_1}{\tau_-}\right)\left(A_2^- + A_3^- \exp\left(\frac{-\Delta t_3}{\tau_x}\right)\right), \end{cases} \quad (2)$$

where the synaptic weight is potentiated at times when a post-synaptic spike occurs and is depressed at the time when a pre-synaptic spike occurs. The potentiation and depression amplitude parameters are A_2^+, A_2^-, A_3^+ and A_3^-, while, $\Delta t_1 = t_{\text{post(n)}} - t_{\text{pre(n)}}$, $\Delta t_2 = t_{\text{post(n)}} - t_{\text{post(n-1)}} - \varepsilon$ and $\Delta t_3 = t_{\text{pre(n)}} - t_{\text{pre(n-1)}} - \varepsilon$, are the time differences between combinations of pre- and post-synaptic spikes. Here, ε is a small positive constant, which ensures that the weight update uses the correct values occurring just before the pre or post-synaptic spike of interest, and finally τ_-, τ_+, τ_x and τ_y are time constants [7].

The TSTDP rule was proposed, in theory, to overcome deficiencies in the traditional PSTDP rule in being unable to reproduce the outcomes of various physiological experiments such as the data generated by frequency-dependent pairing experiments performed in the visual cortex [9], or triplet, and quadruplet spike experiments performed in [10]. The main advantage of synaptic plasticity rules based upon higher order spike patterns over pair-based rules is the fact that contributions to the overall change in efficacy of traditional additive pair-based rules is essentially linear, while for higher order rules, the underlying potentiation and depression contributions do not sum linearly. It is this underlying non-linearity that is captured in such higher order spike-based STDP rules—but is clearly lacking in pair-based STDP—and has been shown to reproduce nonlinear interactions between spikes as those observed in experiments [3], [11].

Comparing the PSTDP rule shown in Eq. 1, and the TSTDP rule presented in Eq. 2, a similar design approach to the circuit shown in Fig. 1, can be employed to design the various parts of the TSTDP rule. In order to generate the potentials for plasticity, there is a need for leaky integrators. As shown in Fig. 1, these integrators are built using a RC network, where the resistor is implemented using the transistor's channel resistance, which is a function of the gate to source voltage of the transistor. The potentiation and depression potentials for plasticity in Fig. 1 are marked with V_{pot} and V_{dep}, respectively. If the amplitudes of these voltages are kept below the threshold of the transistors, to which these potentials are connected, the transistors will operate in the subthreshold regime, where the required exponential behaviour is approximately reproduced.

In addition, the timing differences between spikes, Δts, can be measured by controlling the arrival times of these spikes at the gates of those transistors, which act as switches. Furthermore, the amplitude of the synaptic voltage changes, which are represented by the amount of current that sources into or sinks from the weight capacitor, can be controlled by transistors in series with the main potential transistors. This will implement an approximation of the required multiplications in Eq. 1.

Considering this design methodology, a VLSI circuit for a minimal version of the TSTDP rule, which is capable of reproducing the visual cortex experiments was proposed [7]. This minimal form of TSTDP rule is demonstrated in Eq. 3,

$$\Delta w = \begin{cases} \Delta w^+ = A_3^+ \exp\left(\frac{-\Delta t_1}{\tau_+}\right)\exp\left(\frac{-\Delta t_2}{\tau_y}\right) \\ \Delta w^- = -A_2^- \exp\left(\frac{\Delta t_1}{\tau_-}\right). \end{cases} \quad (3)$$

The circuit for this minimal rule is shown in Fig. 2. This circuit is a major improvement over previous TSTDP circuits presented in [3], [8], [12]. The circuit operates as follows: When a pre-synaptic spike, $V_{\text{pre(n)}}$, is received at the gate of M2, V_{pot1} reaches ground resulting in switching on M5, and then starts to increase linearly toward V_{dd} with a rate determined by V_{tp1} that is applied to the gate of M1. In fact, V_{pot1} that controls the existence of the potentiation in the first place and allows the current to flow through the triplet potentiation branch (M3-M6) at the time of arrival of a post-synaptic spike at M6, represents one of the exponential term in the potentiation part in the first line of Eq. 2 shown as $\exp\left(\frac{-\Delta t_1}{\tau_+}\right)$, where τ_+ is controlled by V_{tp1} and Δt_1 shows the timing difference between the pre-synaptic spikes arrived at M2 and the post-synaptic spike received at M6.

Furthermore, the amount of current passing through the potentiation branch (M3-M6) is controlled by $V_{A_3^+}$, and the second potentiation exponential dynamic, V_{pot2} that controls the gate voltage of M4. This voltage depends on the arrival time of the previous post-synaptic spike, $V_{\text{post(n-1)}}$. When a post-synaptic spike arrives at M13, V_{pot2} reaches ground and

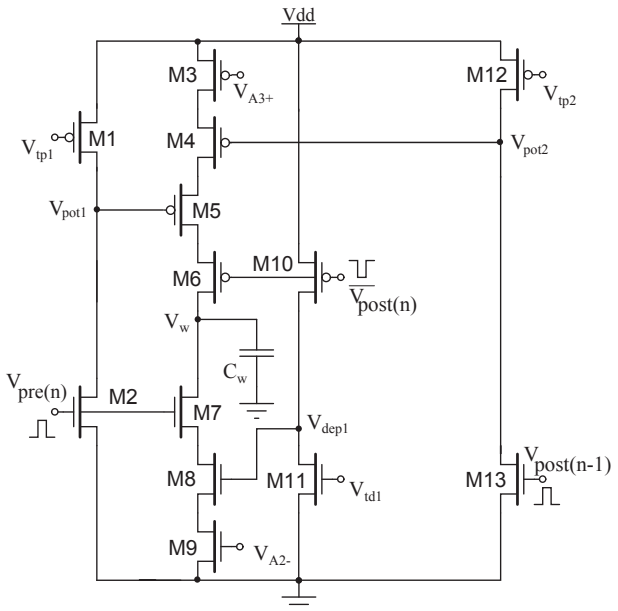

Fig. 2. Circuit for the minimal TSTDP rule. This minimal circuit is capable of reproducing the outcomes of visual cortex experiments [7].

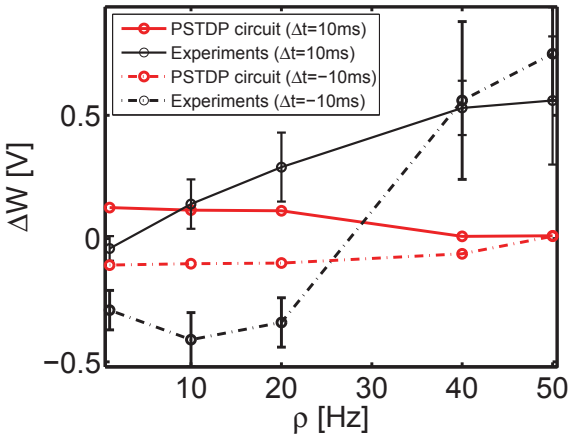

Fig. 3. The PSTDP circuit fails to reproduce pairing frequency experiments performed in the visual cortex. Note that, there is no data available at 30 Hz [7], [9].

after the post-synaptic pulse duration is finished, it starts to increase linearly toward V_{dd} with a rate determined by V_{tp2} that is applied to the gate of M12. Therefore, the current flowing through M3-M4 approximates $A_3^+ \exp(\frac{-\Delta t_2}{\tau_y})$.

The depression part of the proposed circuit, in which current flows away from the weight capacitor, C_w, implements only the pairing depression in a similar way to the circuit proposed in [2]. In this part, current will flow through M7-M9 if there has been a post-synaptic action potential in a specified time window defined by V_{td1} (which corresponds to τ_-), before a pre-synaptic spike. If a post-synaptic spike arrives at M10, then V_{dep1} reaches V_{dd}, resulting in M8 switches on. It starts decreasing linearly over time, with a rate determined by V_{td1}, applied to the gate of M11, which corresponds to τ_- in Eq. 3. If a pre-synaptic spike arrives at the gate of M7, before V_{dep1} reaches ground and therefore M8 switches off, the depression branch will conduct currents out of the weight capacitor, with an amplitude controlled by the gate voltage of M9, which corresponds to A_2^- in Eq. 3.

IV. Experimental Results

In order to verify the performance of both mentioned circuits in reproducing the behavior experimentally found in the visual cortex, they are simulated under similar protocols, data fitting techniques and experimental conditions. Below is a brief explanation of experimental conditions, under which the circuits are examined.

A. Experimental Setup

The proposed minimal TSTDP circuit, as well as Indiveri's PSTDP circuit were simulated in HSpice using the 0.35 μm C35 CMOS process by AMS. All transistors in both designs (shown in Figures 1and 2) are set to 1.05 μm wide and 0.7 μm long. The weight capacitor values are set to 1 pF. It should be noted that the circuits simulated on an accelerated time scale of 1000 times the real time. However, for the sake of simplicity when comparing the results to the experiments, all displayed results are scaled back to real time. In addition, a nearest-spike interaction model has been implemented in both circuits that corresponds to STDP nearest-spike model presented in [7].

B. Experimental Protocol

In the applied protocol in the visual cortex experiments, performed by Sjostrom *et al.* [9], 60 pairs of pre- and post-synaptic spikes with a delay of $\Delta t = t_{post} - t_{pre}$ were conducted with a repetition frequency of ρ Hz. It has been previously illustrated in [9] that altering the pairing repetition frequency affects the total change in weight of the synapse. The visual cortex experimental data under this protocol, are shown in black in Figs. 3 and 4. When simulating both mentioned circuits, the same spiking protocol was employed and the resulting weight changes were measured from the circuit weight capacitors.

C. Error Measurement and Data Fitting Approach

In an identical manner to [7] that examines their proposed triplet model simulation results against the experimental data using a Normalized Mean Square Error (NMSE), both circuits are verified by comparing their simulation results with the experimental data and ensuring a small NMSE value. The NMSE is calculated using the following equation:

$$\mathrm{NMSE} = \frac{1}{p}\sum_{i=1}^{p}\left(\frac{\Delta w_{\mathrm{exp}}^i - \Delta w_{\mathrm{cir}}^i}{\sigma_i}\right)^2, \tag{4}$$

where $\Delta w_{\mathrm{exp}}^i$, $\Delta w_{\mathrm{cir}}^i$ and σ_i are the mean weight change obtained from biological experiments, the weight change obtained from the circuit under consideration, and the standard

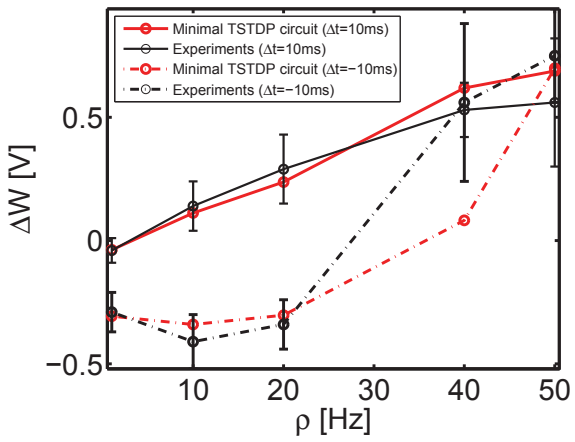

Fig. 4. The minimal TSTDP circuit is able to reproduce frequency-dependent pairing experiments performed in the visual cortex. Note that, there is no data available at 30 Hz [7], [9].

error mean of Δw^i_{exp} for a given data point i, respectively; p represents the number of data points in the data set, here is 10 points that are extracted from [9].

In order to minimize the resulting NMSEs for both circuits and fit the circuit outputs to the experimental data, there is a need to adjust the circuits bias parameters and time constants.

D. Simulation Results

The first circuit that we examine is the PSTDP circuit shown in Fig. 1. After optimizing the circuit's four bias parameters, i.e. V_{tp}, V_{td}, $V_{\text{A}+}$ and $V_{\text{A}-}$, the best obtained NMSE is 7.74, which is very close to the PSTDP model error, reported in Fig. 6A of [7]. In addition, circuit simulation results illustrated in Fig. 3 are similar to the reported results in [7], which shows that the PSTDP rule fails to reproduce the outcomes of visual cortex experiments.

In the second simulation, the proposed minimal TSTDP circuit is simulated with the same protocol and its five biases, namely V_{tp1}, V_{td1}, V_{tp2}, $V_{\text{A3}+}$ and $V_{\text{A2}-}$, are optimized so that the NMSE was minimized. Simulation results for this circuit along with the experimental data, are depicted in Fig 4. This figure shows how well the proposed TSTDP circuit performs, in comparison to the PSTDP circuit, and reaches a good NMSE=0.39, which is very close to the reported NMSE=0.34, obtained using Matlab simulations of the minimal nearest-neighbour TSTDP model, as shown in Table 3 of [7].

Given the ability of the proposed minimal TSTDP circuit to mimic visual cortex experimental data, a slightly modified version of our TSTDP circuit, is also capable of reproducing conventional STDP learning window, Triplet, Quadruplet, and BCM experiments [13]. The proposed TSTDP circuit consists of 13 transistors, which is only one transistor more than the simple PSTDP circuit, shown in Fig. 1. It has a lower number of transistors than almost all other previous PSTDP circuits available in the literature [1], [3]. Furthermore, the circuit is significantly simpler, and smaller than the previously proposed TSTDP designs available in the literature [3], [8], [12].This feature makes the proposed circuit consume less power and occupies a smaller area, which are the main goals always being sought by the neuromorphic VLSI designer.

V. Conclusion

A compact VLSI implementation of triplet-based STDP (TSTDP) rule is proposed. The synaptic weight modifications performed by the proposed circuit closely recovers the behavior found in complex biological experiments in the visual cortex, while all previous PSTDP circuits fail to reproduce those experiments. Furthermore, compared to previous VLSI designs for both pair-based and triplet-based STDP, the proposed circuit has significant advantages in terms of power and area consumption. This feature, along with an improved synaptic weight modification capability, makes the proposed design an interesting synaptic plasticity component for implementing large-scale Spiking Neural Networks (SNNs).

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