Novel AESA Architecture for Earth Observation and Planetary Sciences

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Abstract-In this paper we present a description and evaluation of Gallium Nitride (GaN) Transceivers within frontends for space-based Synthetic-aperture radar (SAR). The GaN power switches are evaluated in a voltage mode Class-D (VMCD) RF amplifier and as a DC-DC converter. The efficiency of the circuit when evaluated as a Class D power amplifier (PA) is 73% at 250 MHz and delivers an output power of 37.3 dBm. The measured DC-DC converter circuit has an efficiency of over 89.7% at 100 MHz, delivering 38.6 dBm. These are the highest reported efficiencies for the RF PA and the switching modulator performance is comparable to state of the art at its respective operating frequencies. A flat panel metasurface antenna topology that can be integrated into the RF front end to facilitate a variety of SAR modalities. This antenna structure can substantially simplify the deployment mechanism of airborne and spaceborne SAR instruments.

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1. INTRODUCTION

Synthetic Aperture Radar (SAR) has become an indispensable tool in the observation of Earth and Planetary physical properties as shown in the NASA Goddard Space Flight Center (GSFC) SAR concept in Fig. 1. There is intense interest in developing ultra-compact, lightweight, high performance SARs in order to make spaceborne missions feasible and affordable. Such a concept would be applicable to a number of science, commercial, and military areas ranging from ecosystem structure, surface and sub-surface topography, soil freeze-thaw, ice sheet

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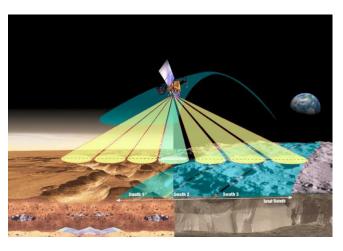


Fig 1. NASA SESAR Concept [1]

composition, glacier depth, and surface water, among many others [1,2].

The size, weight and performance parameters required for such missions calls for the development of integrated multifunctional system-on-chips (SoCs) [3] within Active Electronically Scanned Array (AESA) antenna architectures [2].

Gallium nitride (GaN) technology offers several remarkable advantages as compared to its GaAs counterpart, such as higher breakdown electric field and power density, improved radiation hardness and thermal properties, as well as comparable noise performance in comparison to CMOS and GaAs technologies. Gallium Nitride RF HEMTs technology which offer low onresistance, low capacitances and high breakdown voltage are ideal candidates for RF and power conversion applications. The GaN technology represents a general-purpose technological platform that can be exploited to realize integrated

transceivers with power conversion and signal amplification functionalities with smaller footprint, higher efficiencies, and increased power density.

P-Band SARs are currently being considered for planetary exploration [4]. However, solid-state power amplifier technologies were not mature enough to be deployed in AESA topologies [5]. This work investigates advanced RF GaN transceivers for P-Band operation along with next antenna designs generation that enable revolutionary performance eliminating by complex switching circuity using metamaterial surfaces.

This paper is organized as follows. The GaN process technology is given in Section II. RF sensor architecture is described in Section III. The simulation and layout are given in Section IV. The measured results are given in Section V. Finally, metasurface antennas structure is given in Section VI, followed by summary and conclusion in section VII.

2. PROCESS TECHNOLOGY

The AlGaN/GaN HEMTs investigated in this study were fabricated on a commercial foundry 3-inch GaN-on-SiC process. The epitaxial structure has a Si GaN buffer with Fe doping for improved isolation. An AlN spacer was inserted between the buffer and the AlGaN Schottky barrier layer, and the surface is covered by a GaN cap layer for reduced leakage. The active device layers are isolated by performing a mesa etch down to the GaN buffer. The ohmic contacts were formed by

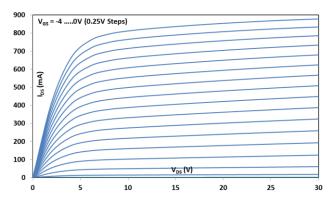


Fig. 2. IV Curves for 1 mm GaN HEMT

Table. 1. Characteristics of GaN HEMT

Size	Ron	Cin	Соит	V _{BD}	V _{DS}
(µm)	(Ω)	(pF)	(pF)	(V)	(V)
12 x 200	0.9	4.08	0.98	100	30

alloying Ti/Al/Mo/Ti/Au. The ohmic source-drain spacing is 4 μm with nominal contact resistance of 0.5 ohm-mm. The gate length is defined by patterning and etching a 0.25 μm opening in the Silicon Nitride (SiNx). A second patterning and subsequent metallization over the etched SiNx opening completes the gate process and forms an integrated field plate.

Also, a source-connected second field plate (2FP) was implemented to reduce the electric field in the device channel under high voltage operation. The 2FP geometry was designed to optimize the efficiency and gain of the device. For backside via formation the wafers are ground and polished to a thickness of $100 \ \mu m$.

The DC I-V characteristics for a 1 mm HEMT device up to $V_{DS} = 30 \text{ V}$ and for $V_{GS} = -5...0 \text{ V}$, is given in Figure 2. The breakdown voltage is above 100 V, which is about four times as high as for GaAs devices having similar cut-off frequencies. The characteristics of the power transistor are given in Table 1.

The device also exhibits excellent transconductance characteristics. A maximum gm of 340 mS/mm was measured at a drain bias voltage of 10 V with $V_{GS} = -1.5$ V, and 310 mS/mm at $V_{DS} = 30$ V with $V_{GS} = -1.5$ V. The complete channel pinch-off is at about -3.9 V independent of the drain bias voltage. An extrinsic transit frequency of $f_T = 32$ GHz and an extrinsic maximum frequency of oscillation of $f_{MAX} = 42$ GHz were obtained at $V_{DS} = 30$ V.

3. RF SENSOR ARCHITECTURE

The proposed SAR sensor architecture is a transceiver topology consisting of high efficiency high-power amplifiers, single pole double throw (SPDT) switches, low noise amplifiers (LNAs) and power conversion blocks all integrated onto a

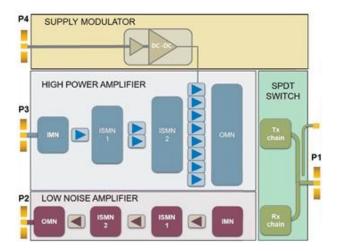


Fig. 3. Modulator incorporated GaN Transceiver, where IMN, ISMN and OMN are input matching network, interstage matching network and output matching network, respectively.

single GaN die to form a Single Chip Front End (SCFE) as shown in Figure. 3 [6].

The cost, performance, and volume trade off leads to the utilization of efficient off-chip SMD filters in contrast to fabricating on-chip integrated filters using various metallization available within the foundry process. The major objective is to optimize the Size, Weight and Performance (SWaP) of the sensor element for flight qualification. Descriptions of these modules are provided in the following subsections.

a) Switching-mode Power Amplifier Circuit: Voltage Mode Class D and Half bridge DC-DC Converter

The power transistors within power amplifiers approaches 100% efficiency when used as switches, hence are called switch mode power amplifiers (SMPAs). This non-linear mode of operation enables cooler operation of transistors. Here a high efficiency Class D P-Band power amplifier topology was investigated. There are two types of Class-D amplifiers: voltage mode (VMCD) and current mode (CMCD). The voltage mode is illustrated in Figure 4 [7]. The output node is switched alternatively between the supply voltage and ground. Figure 5 shows the square output voltage waveform from a VMCD [7]. The dual of VMCD circuit, the Current Mode Class D steers a DC current between the two switches.

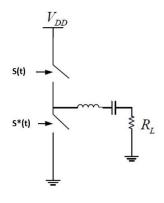


Fig. 4. Simplified Schematic of VMCD

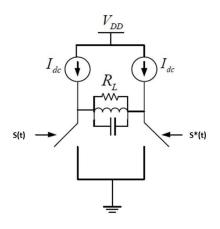


Fig. 5. Simplified Schematic of CMCD

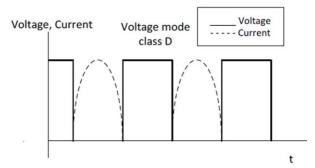


Fig. 6. VMCD Voltage and Current Waveforms

The output voltage and current waveforms for an ideal operation is shown in Figure. 6 and 7 [7]. In VMCD the voltage waveform is a square pulse and alternatively in its dual circuit, the current is a pulse. The current is a half wave rectified sine wave in VMCD, while CMCD delivers a half wave rectified output voltage. In practice the parasitics cause the waveforms to deviate from this ideal shape.

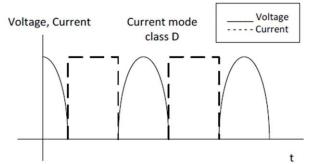


Fig. 7. CMCD Voltage and Current Waveforms

The LC filters in the circuits provide the optimum load impedance at the fundamental frequency. In VMCD the higher order harmonics of the output square wave should terminate to open circuit, while in CMCD the higher order harmonics of the output current square wave must have short circuit termination to maximize the power efficiency. The major loss mechanisms include the capacitance and inductance losses, along with the resistance loss (Ron) in the power transistor.

The timing of switching transistors is crucial as there could be instances in which both are in the "ON" state in the VMCD allowing a large current to flow through and destroying the switching elements or in the "OPEN" state in the case of a CMCD, causing voltage pikes at the output.

A Voltage Mode Class D HPA was chosen due to ease of design, integration and testing requirements. In order to simplify the design process reusable circuit blocks were considered for the power amplifier and the switching power converter for integration into a single chip front end die. As a result, the HPA and the DC-DC converter share the same topology.

The switching circuit consists of a totem pole configured output stage with high and low-side gate drivers driven in anti-phase by an external PWM signal as shown in Fig. 8. This enables the high-side switch to be turned on while the low-side switch is off. Since no complementary GaN HEMTs are available, different voltage swings need to be generated at the input of the output-stage transistors.

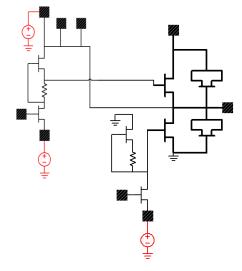


Fig. 8. Schematic of switching circuit combined with the driver circuit.

Particularly, a high voltage swing between -5 V to V_{DD} (max. 30 V) is needed at the gate of the high side transistor whereas a comparatively small voltage swing from -5 V to 0 V is required at the input of low side power transistor.

In this work, a modified bootstrap topology was adopted for the high side driver. The gate drivers are optimized for high efficiency by optimizing the sizes of the switching transistors, which is driven by an external pulse and load transistors which supply the required voltage to turn on and pinch off the depletion mode power stage transistors. The switching and load transistor sizes were $4 \times 50~\mu m$. The power stage transistor was $10 \times 300~\mu m$ and the size of the used diodeconnected transistor was $10 \times 150~\mu m$.

The simulated transient waveforms show clean switching and no significant overshoot or waveform distortion at the switch node. It must be noted that the simulations did not consider intrinsic and extrinsic parasitics and hence the switching waveform is that of the ideal scenario.

4. SIMULATION AND LAYOUT

The simulated output voltage of the circuit at the switch node for a duty cycle of 50% with an input voltage set to 30 V and a frequency of 100 MHz is shown in Figure 9. One of the major issues that

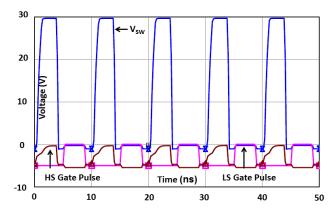


Fig. 9. Simulation of switch node voltage waveform.

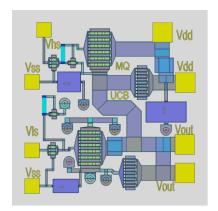


Fig. 10. Layout of the integrated power switch

needs to be addressed when simulating switching topologies is the lack of switching models within the process design kit, which can lead to convergence problem for certain bias conditions. The layout of the integrated power switch was done using a commercial foundry 0.25 µm GaN processes technology is shown in Fig. 10. Figures 11 and 12 show photographs of fabricated MMIC and protype PCB, respectively.

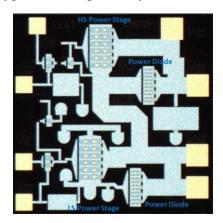


Fig. 11. Photograph of fabricated MMIC (2 mm × 2 mm)



Fig. 12. Photograph of the prototype PCB.

The fabricated chip was soldered onto the gold-plated base using silver epoxy. This provided good thermal conductivity and mechanical stability. The interface to the PCB was created using 25 µm thick gold wire bonds. SMA adapters were screwed onto the test jig for the PWM gate driver signals to interface to the chip. The test jig acts as the ground node since the back side of the MMIC is in contact with it and the test jig is connected to the power supply ground.

As mentioned previously, the cost, volume and current density offered by external SMD components were superior to what was available using integrated filters aimed by the 3 metals utilized in the process. High Q, low ESR chip capacitors and inductors from Coilcraft Midi spring series were used for the 4th order filter implementation.

External decupling capacitors were soldered onto the PCB to minimize instability issues that can arise due to the very high gain of GaN transistors at low frequency, and also to eliminate any feedback loops that may occur during the testing regime in a noisy lab environment. The band pass filter response with a center frequency of 250 MHz is shown in Figure. 13, and had approximate component values of $L_1 = 30 \, nH$, $L_2 = 25 \, nH$, $L_3 = 50 \, nH$, $L_4 = 50 \, nH$, $C_1 = 15 \, pF$, $C_2 = 20 \, pF$, $C_3 = 10 \, and \, C_4 = 10 \, pF$.

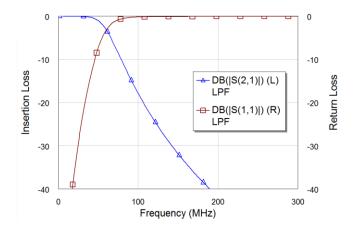


Fig. 14. Filter Analysis – Low Pass Filter

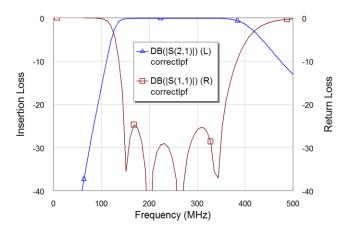


Fig. 13. Filter Analysis - High Pass Filter

The LPF response is given in Figure. 14 and its component values are $L_1 = 100$ and $L_2 = 250$ nH, while the capacitor values are $C_1 = 100$ pF and $C_2 = 40$ pF.

Figure 15 shows the time domain measurement setup with. off-chip SMD low pass filter (*LPF*) and band pass filter (*BPF*) structures are clearly shown. High frequency, high fidelity PWM control signals were generated using Agilent M8190A AWG, which is fed to a Hittie pulse driver amplifier. These signals are level shifted using an external low frequency bias tee to the appropriate HS and LS PWM gate drive signals. The output switch node voltage was measured using Agilent DSOX3104T oscilloscope. Figure 16 shows the test bench with the prototype PCB under test mounted on a temperature-controlled surface.

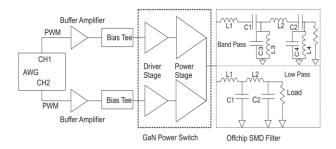


Fig. 15. Time domain measurement setup



Fig. 16. Photograph of DUT

5. MEASURED RESULTS

a) 250 MHz Class D PA

The switching circuit was characterized as a VMCD with an external bandpass filter implemented using SMD components and with a center frequency of 250 MHz. The input signal was driven by 50% duty cycle PWM signal, while the output from the switch node was terminated with a 50 Ω load. Figure 17 shows the measured drain efficiency (DE), power added efficiency (PAE) and output powers. The VMCD MMIC circuit delivered a maximum output power of 37.3 dBm with a PAE of 73 %. The drain efficiency measured over various drain voltages remained over 90%.

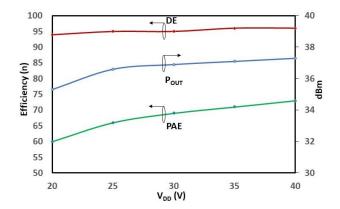


Fig. 17. Efficiency, Pout v V_{DD} of VMCD (Fc = 250 MHz)

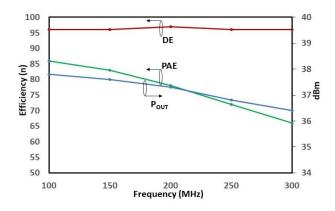


Fig. 18. Efficiency (%), POUT (dBm) v Frequency (MHz)

Next, the frequency response of the PA was analyzed by varying the switching frequency from 100 to 300 MHz. PAE of 86% was achieved at 100 MHz while delivering 37.9 dBm. With increase in frequency, the PAE decreased due to switching losses and misalignment of drive signals. The PAE of 66% measured at 300 MHz. It was extremely challenging to get the deadtime in the driver pulses to align without damaging the power transistors at high switching frequencies. As a result, the V_{DD} was reduced to 30 V for the DC-DC converter's measurement, this allowed for a higher current to be drawn by from the supply as the load value was varied

b) 100 MHz DC-DC Converter

A low pass SMD filter with cutoff frequency below 100 MHz was chosen as earlier. The switching circuit was driven by an external PWM signal for varying load conditions and duty cycles.

Figure 19 shows the switch node voltage of the DC-DC Converter.

Figure 20 shows the efficiency curves for the dc-dc converter at duty cycles (DC) of 25%, 50% and 75% at 100 MHz. Power stage efficiency peaks at 96.8%, while the total efficiency is 89.7% with a maximum output power of 38.6 dBm.

It must be stated that normal RFPA measurement setup is not catered for time domain signals hence, the experimental setup for this work was extremely difficult due to low frequency electrical noise within the lab and instability issues due to long cables forming feedback loop.

The use of commercially available GaN semiconductor process, innovative circuit design techniques incorporating efficiency enhancement techniques and a modular approach to transceiver functional blocks enables the development of new Tx/Rx modules for space based AESA radars.

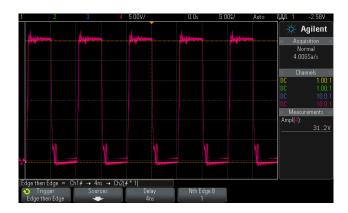


Fig. 19. VMCD Switch Node Voltage

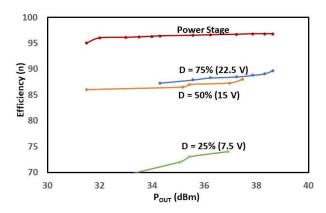


Fig. 20. P_{OUT} v Efficiency of DC-DC converter for various duty cycles.

6. METASURFACE ANTENNA ARCHITECTURE FRONT END

Developing lightweight, compact, and power efficient RF frontends for SAR systems require that innovative antenna structures be developed as part of the RF frontend. Conventionally, SAR modalities are realized using high gain antennas. Because the length of the observation path is rather large for orbital SAR applications, such as Earth observation and interplanetary science, having a high gain antenna in the front end is crucial to satisfy the key link budget metrics. However, high gain antennas typically require large apertures, such as parabolic reflector antennas, patch arrays and reflect arrays to name a few [8].

This selection brings several challenges when it comes to deploying instruments with such antennas. Parabolic reflector antennas have a volumetric structure and typically exhibit aperture sizes above the payload allowance of airborne and spaceborne instruments. As a result, launching instruments with parabolic reflector antennas requires a special deployment mechanism to fold the reflector before launch and unfold them after the instrument is deployed [9, 10]. Such a deployment mechanism further increases the overall weight of the antenna structure and becomes challenging given the limited weight requirements of instruments for SAR missions.

Besides, the parabolic reflector antenna is a passive architecture and requires mechanical scanning to steer its radiation pattern, further complicating the deployment architecture. As an alternative, flat-panel reflectarrays can be used to replace the volumetric parabolic antennas. This advantage can simplify deployment process and also reduce the weight requirements substantially. and cost The application of the reflectarray architecture for CubeSat platforms recently has been demonstrated as part of NASA's MarCO mission [11]. Despite the planar geometry of the antenna aperture, reflectarrays require a secondary feed to illuminate the reflectarray aperture. Therefore, reflectarrays can still be considered as volumetric structures requiring the launch of multiple parts

once the instrument is deployed. A truly flat-panel architecture can be realized in the context of patch array antennas, such as the topology used in NASA's soil-moisture remote-sensing applications at L-band frequencies [12].

However, microstrip patch array antennas rely on a phased array principle, suggesting that, to be able to reconfigure the radiation pattern of these antennas, they either need to be mechanically rotated, such as in [13], or a phase shifting technology is required to be adopted [14, 15]. Whereas mechanical scanning is undesirable, allelectronic operation in the context of phased arrays requires that each antenna element within the array aperture be connected to a dedicated shifting circuit. This requirement phased substantially complicates the hardware architecture of phased arrays, especially for electrically large array antennas where the number of individual antennas forming the array aperture can be large. Moreover, phase shifting circuits typically exhibit large losses and to compensate for these losses, dedicated power amplifiers are needed. As a result, the phased array topology can be power hungry and expensive.

To address these challenges, metasurface antennas can be used. A metasurface antenna can synthesize an arbitrary waveform of interest in an all-electronic manner without the need for phase shifting circuits. This is achieved in a holographic manner, similar to an optical hologram. In this technique, a guided-mode (or reference-wave) is launched into the metasurface to excite the metasurface layer. The goal of the metasurface in this design process is to modulate the launched reference-wave into the desired aperture wavefront distribution, which produces the radiation pattern of interest in the far-field of the antenna. Once the metasurface layer is calculated. exciting the metasurface layer with the referencewave is guaranteed to produce the radiation pattern of interest [16-17].

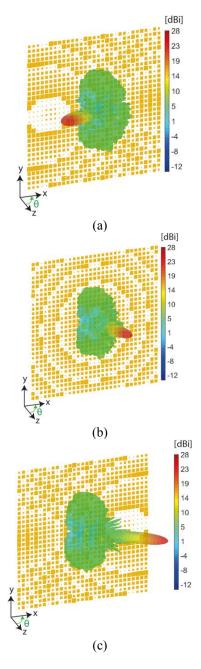


Fig. 20. Flat-panel metasurface antenna for beam-scanning (a) θ =-45°, (b) θ =0°, (c) θ =45°

A significant advantage of the holographic beamforming metasurface antennas is that different from the reflectarray topology, the secondary source feeding the metasurface can be integrated into the metasurface architecture, resulting in a truly flat-panel aperture layout [16]. As an example, in Figures. 20 and 21, we show the numerical simulations of a flat-panel metasurface architecture that can scan its radiation pattern along the azimuth plane (xz-plane) by using the holographic beam-forming principle.

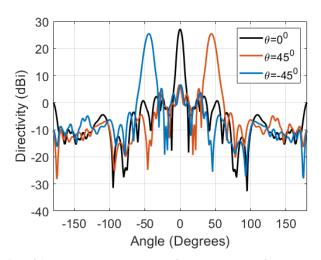


Fig. 21. Flat-panel metasurface antenna for beam-scanning - Comparison of the directivity patterns along the azimuth scanning axis.

The simulations of the metasurface antenna are carried out using a full-wave electromagnetic simulation software, CST Microwave Studio.

As can be seen in Figure. 20, using the same aperture layout, a stripmap SAR modality can be realized in an all-electronic manner. Although shown in scanning mode, the metasurface concept can be used to create an arbitrary aperture waveform of interest that would radiate tailored radiation patterns in the far-field of the antenna. example, presented For the metasurface architecture can also be modulated to produce a spotlight SAR modality, focusing the radiation pattern of interest over a certain field-of-view during the SAR scan to improve the imaging resolution.

7. SUMMARY

The design and realization of MMIC power switch with its associated drivers demonstrated in a high frequency switching circuit as a voltage mode class D power amplifier and as a DC-DC converter. The VMCD delivered 39.5 dB of output power with an associated PAE of 74.5% at a switching frequency of 250 MHz with bandpass filter circuit. The power converter with a low pass SMD filter circuit exhibited efficiencies above 80% for a wide range of load conditions, delivering a maximum output power of 40.8 dBm and a peak efficiency of 92%. The high side driver turns out to be a critical element in the overall efficiency as well as output waveform integrity. The drain efficiencies for both circuits were above 90%.

Various GaN switching circuits [19-25] — both PAs and power converters in literature, VMCD has the highest PAE of reported Class D GaN PAs in the VHF band, the efficiency of the integrated power switch as a power converter is comparable to those available in literature while delivering the output power.

GaN based transceiver architectures in the P-band will lead to the development of compact, lightweight, high power phased array radars with individual control of each radiating element. This will give an extra degree of freedom for system architects in the design of advanced SAR concepts for earth observation and interplanetary missions.

We have also shown a flat-panel metasurface antenna topology that can be integrated into the RF frontend to facilitate a variety of SAR modalities. The use of metasurface allows for complete elimination of complex switching circuity within the AESA front end. This antenna substantially structure can simplify the deployment mechanism airborne and spaceborne SAR instruments.

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BIOGRAPHY



Aaron Pereira received his BE in Microelectronic Engineering from Griffith University, Australia in 2003. From 2003 to 2010, he worked various roles as RF design engineer, systems engineer and project management positions in Australian space and defence industry. He is a recipient of Endeavor Australia Research and

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Neil Weste received the B.Sc., B.E. (Elec.), and Ph.D. degrees from the University of Adelaide, Australia. In 1977, he commenced working at Bell Labs, Holmdel, NJ, USA, in the area of IC design. Subsequently, he spent a year in North Carolina primarily at Duke University, UNC

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He later worked at Cisco Systems after the acquisition of Radiata Communications in 2000. He then became and angel investor, and after developing an interest in flying, he cofounded Oz Runways Pty. Ltd. where he co-wrote the software now used by the majority of pilots in Australia in their Electronic Flight Books. He is a Fellow of ATSE, was awarded a D.E. (honoris causa) from the University of Adelaide in 2004 and received the 2010 Clunies Ross Medal for his contributions to the development of Wi-Fi. He is currently an adjunct Professor in the School of Electrical and Electronic Engineering, at the University of Adelaide.



Derek Abbott was born in South Kensington, London, U.K., in 1960. He received the B.Sc. (Hons.) degree in physics from Loughborough University, Leicestershire, U.K., in 1982, and the Ph.D. degree in electrical and electronic engineering from The University of Adelaide, Adelaide, SA, Australia, in 1995,

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