An Accurate Analytical Spur Model for an Integer-N Phase-Locked Loop

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***Abstract*—Reference spur is a limiting performance factor in an integer-N phase-locked loop (PLL). In this paper, we investigate the effect of VCO gain, ripple magnitude in VCO tuning voltage and reference frequency with reference spur magnitude. Normally, VCO gain and reference frequency are chosen according to needed system requirement, leaving only the ripple voltage on the VCO control signal to be minimised in order to minimize the reference spur. The ripple voltage is mainly contributed by current mismatch, current leakage, switching delay and discrepancies between the rise and fall times in charge pump circuit. In addition, loop filter is also affecting the ripple voltage. In this paper, we consider these effects analytically to predict ripple voltage in the VCO tuning voltage and hence calculate the reference spur magnitude of the PLL device.**

***Index Terms*—reference spur, tuning voltage, charge pump, phase/frequency detector (PFD), voltage controlled oscillator (VCO), current mismatch, loop filter.**

I. Introduction

PLL is a commonly used module in the frequency synthesizer of an RF transceiver to result in a high quality data transmission. PLL noise consists of random noise and periodic noise. Random noise is known as phase noise in frequency domain or jitter in time domain. Meanwhile, periodic noise is known as spur. In integer-N PLL architecture, the spur is called reference spur since the spur exists at a reference frequency offset from the carrier frequency.

Many works have been conducted on PLL phase noise modelling [1]–[3], however, the reference spur aspect of PLL modelling attracted much less attention. Reference spur is modelled by a narrow-band frequency modulation theory [4], [5]. Based on the published models, spur magnitude is predicted and used in several published works [6]–[8]. However, none of the work models ripple voltage in the VCO tuning voltage, which is the main source to the spur magnitude.

In the published spur analysis, ripple on the VCO tuning voltage is assumed to be a sinusoidal signal, resulting an inaccurate spur magnitude estimation. In this paper, we accurately model the ripple on tuning voltage, hence an accurate spur magnitude could be estimated. In addition, the magnitude of the ripple voltage is also analysed. The ripple voltage is caused by circuit-non-idealities in charge pump and phase/frequency detector (PFD). Three non-idealities, namely current leakage, current mismatch and switching delay, have been modelled in phase domain [8]. The relationship between phase error due to these three non-idealities and ripple magnitude were discussed in [4]. However, the non-idealities effect were discussed seperately, hence the resulting reference spur magnitude estimation was only considered for that particular non-ideality. In this paper, time domain analysis will be considered to model the effect of current leakage, current mismatch, rise and fall times characteristic and switching delay on the reference spur. In addition, this work proves that VCO tuning port leakage affects the reference spur magnitude for PLL when second order loop filter is used. Then, combinations of all these non-idealities are considered together for reference spur magnitude estimation.

Reference spur estimation using simulation requires a huge amount of time. A long time transient analysis is required to make sure the PLL is locked. The VCO output signal after the PLL is locked is sampled and FFT is performed to the sampled data. The FFT magnitude at the first reference frequency offset is divided by FFT magnitude at the VCO frequency in order to get the reference spur magnitude. The proposed analysis is able to estimate reference spur magnitude without performing the time consuming simulation.

In Section II a reference spur analysis for an integer-N PLL is presented. In Section III, ripple in VCO tuning voltage is modelled. The spur magnitude predicted using the proposed model is then compared with transistor level simulation in Section IV. Finally, this work is summarized in Section V, followed by an acknowledgement.

II. Reference Spur Analysis

The tuning voltage, $V_{\rm t}$ tunes the VCO output frequency. Ideally, $V_{\rm t}$ is a straight line without any ripple, however in physicall implementations, $V_{\rm t}$ is a periodic signal with pulse repetition rate equal to reference frequency, as shown in Figure 1. This periodic signal is caused by non-idealities in charge pump and PFD circuits.

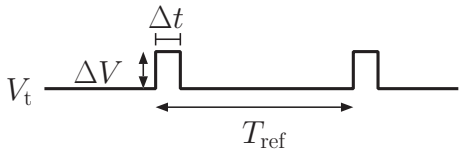

Fig. 1. Due to circuit non-idealities, VCO tuning voltage becomes a periodic signal instead of a solid line.

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$$V_{\rm vco}(t) = V_{\rm o}\cos\left(\omega_{\rm vco}t\right) - \frac{V_{\rm o}K_{\rm v}\Delta V}{T_{\rm ref}\omega_{\rm ref}^2}\sin(\omega_{\rm vco}t)\left(\cos(\omega_{\rm ref}(\Delta t - t)) - \cos(\omega_{\rm ref}(\Delta t + t))\right) . \quad (9)$$

In locked state, ΔV is very small, hence a narrow-band frequency modulation theory can be used to model the VCO output. The VCO output signal could be presented by Equation 1, where $V_{\rm o}$ is the amplitude of VCO output, $V_{\rm t}$ is the VCO tuning voltage, $\omega_{\rm o}$ is the VCO output frequency when tuning voltage is zero and $K_{\rm v}$ is VCO gain in rad/sV.

$$V_{\rm vco}(t) = V_{\rm o}\cos\left(\omega_{\rm o}t + K_{\rm v}\int V_{\rm t}\ dt\right) . \quad (1)$$

Using a Fourier Series, $V_{\rm t}$ could be presented as

$$V_{\rm t}' = V_{\rm t} + \frac{\Delta V\Delta t}{T_{\rm ref}} + \frac{2\Delta V}{T_{\rm ref}\omega_{\rm ref}}\sum_{n\neq 0}\frac{\cos(n\omega_{\rm ref}t)\ \sin(n\omega_{\rm ref}\Delta t)}{n} . \quad (2)$$

Where $\omega_{\rm ref}$ is the reference signal phase and n is integer. Let the periodic component in the Fourier Series be represented as $A(t)$ and VCO output frequency is represented as $\omega_{\rm vco}$, yields:

$$A(t) = \frac{2\Delta V}{T_{\rm ref}\omega_{\rm ref}}\sum_{n\neq 0}\frac{\sin(n\omega_{\rm ref}(\Delta t - t))}{n} . \quad (3)$$

and

$$\omega_{\rm vco} = \omega_{\rm o} + K_{\rm v}V_{\rm t} + K_{\rm v}\frac{\Delta V\Delta t}{T_{\rm ref}} . \quad (4)$$

Substituting $V_{\rm t}$ in Equation 1 with Equations 2, 3 and 4 yields:

$$\begin{aligned} V_{\rm vco}(t) &= V_{\rm o}\cos\left(\omega_{\rm vco}t + K_{\rm v}\int A(t)\ dt\right) , \\ &= V_{\rm o}\cos\left(\omega_{\rm vco}t\right)\cos\left(K_{\rm v}\int A(t)\ dt\right) \\ &\quad -V_{\rm o}\sin\left(\omega_{\rm vco}t\right)\sin\left(K_{\rm v}\int A(t)dt\right) . \end{aligned} \quad (5)$$

Let the phase deviation due to circuit non-idelaities, ϕ be represented as:

$$\phi = K_{\rm v}\int A(t)\ dt . \quad (6)$$

The value of ϕ is very small, therefore Equation 5 can be simplified as:

$$V_{\rm vco}(t) = V_{\rm o}\cos\left(\omega_{\rm vco}t\right) - V_{\rm o}\phi\ \sin\left(\omega_{\rm vco}t\right) . \quad (7)$$

Expand the phase deviation, ϕ in Equation 6, yields:

$$\phi = \frac{K_{\rm v}\Delta V}{T_{\rm ref}\omega_{\rm ref}^2}\sum_{n=0}^{\infty}\frac{\cos(n\omega_{\rm ref}(\Delta t - t)) - \cos(n\omega_{\rm ref}(\Delta t + t))}{n^2} . \quad (8)$$

Substituting Equation 8 into Equation 7 with only the first spur order is considered, where $n = 1$, the VCO output is given by Equation 9.

According to the FM theory, the modulation index, β, is

$$\beta = \frac{K_{\rm v}\Delta V}{T_{\rm ref}\omega_{\rm ref}^2} . \quad (10)$$

Replace the VCO gain $K_{\rm v}$ (in rad/sV) with $2\pi K_{\rm v}$ (in $\rm Hz/sV$) and simplify Equation 10, yields

$$\beta = \frac{K_{\rm v}\Delta V}{\omega_{\rm ref}} . \quad (11)$$

A frequency modulated signal can be expressed by the Bessel function series, as given in Equation 12.

$$J_n(\beta) = \sum_{k=0}^{\infty}\frac{-1^k}{k!\ \Gamma(k+n+1)}\left(\frac{\beta}{2}\right)^{2k+n} . \quad (12)$$

For a small modulation index, $\beta \ll 1$, carrier amplitude is approximately 1, $J_0(\beta) \cong 1$ and the first spur amplitude is approximately half of the modulation index, $J_1(\beta) \cong \beta/2$, while the rest of series is approximately zero. Therefore, the reference spur magnitude, P_r in dBc is given by

$$P_r = 20\log\left(\frac{K_{\rm v}\Delta V}{2\omega_{\rm ref}}\right) . \quad (13)$$

Equation 13 is similar to [4], [5], except for the VCO gain in the published work is in rad/sV, while this work proves that the VCO gain should be in $\rm Hz/sV$, which means reference spur magnitude calculated from the proposed analysis is 2π lower compared to the published work. This difference is because the published work assumed the tuning voltage signal as a sinusoidal, while the proposed analysis accurately models the tuning voltage using the Fourier Series.

III. VCO Tuning Voltage

As shown in Equation 13, ripple in VCO tuning voltage, ΔV is proportional to reference spur level. In this section, the amplitude of ΔV is modelled, hence reference spur could be calculated.

The presented analysis only concentrates on the reference spur, therefore PLL is assumed to be in locked condition. For analysis simplification, charge sharing and clock feedthrough are not taken into account. In locked condition, charge transfer to the loop filter is zero, $Q = 0$. The charge transfer to the loop filter is given by

$$\begin{aligned} Q &= I_{\rm cp}\ t_{\rm PFD} \\ &= \left(I_{\rm up} - I_{\rm dn}\right)t_{\rm PFD} . \end{aligned} \quad (14)$$

$$V_{t_{I_{up}}}(t) = \begin{cases} -\frac{1}{C}\int I_{dn} dt & \text{if } 0 < t < t_{diff} \\ -\frac{I_{dn} t_{diff}}{C} + \frac{1}{C}\int (I_{up} - I_{dn})\, dt & \text{if } t_{diff} \le t \le (t_{diff} + t_{PFD})\ . \end{cases} \quad (17)$$

$$V_{t_{I_{dn}}}(t) = \begin{cases} \frac{1}{C}\int I_{up} dt & \text{if } 0 < t < t_{diff} \\ \frac{I_{up} t_{diff}}{C} + \frac{1}{C}\int (I_{up} - I_{dn})\, dt & \text{if } t_{diff} \le t \le (t_{diff} + t_{PFD})\ . \end{cases} \quad (19)$$

where t_{PFD} is PFD delay and I_{cp} is net charge pump current goes to loop filter, with I_{up} is the current enter the loop filter and I_{dn} is the current exits the loop filter.

At the beginning, consider the loop filter as a single capacitor C. Detailed analysis on second and third order loop filters are discussed later in Section III-E. The VCO tuning voltage, V_t is given by

$$V_t(t) = \frac{1}{C}\int I_{cp}\ dt\ . \quad (15)$$

Ideally charge pump current I_{up} and I_{dn} are equal, PFD delay for UP signal (t_{up}) is equal to delay in DOWN signal (t_{dn}). Therefore, no disturbance exist on the VCO tuning voltage ($\Delta V = 0$).

Non-idealities in the charge pump and PFD affect the tuning voltage. This section discusses the effect of charge pump current mismatch and PFD delay, charge pump current leakage, switching delay, rise and fall times characteristic and loop filter order to the ΔV.

A. Charge pump current mismatch and PFD delay

Due to channel length modulation and variation of parameters between the NMOS and PMOS transistors, I_{up} is not equal to I_{dn} [9]. Since the total charge transfer to the loop filter must be zero, the amount of PFD delay either UP or DOWN signal has to be adjusted to compensate the current difference as shown in Figure 2. If I_{up} is larger than I_{dn}, t_{dn} should be slightly larger than t_{up}, and vice versa.

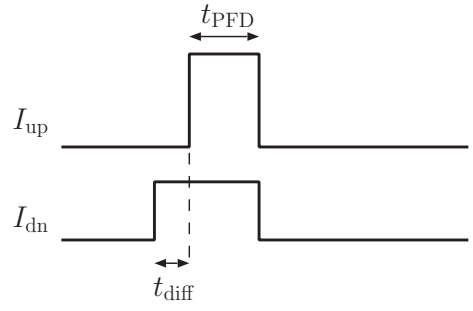

Fig. 2. I_{up} is larger than I_{dn} resulting longer t_{dn} to compensate for the current mismatch, hence produces a small ripple in the VCO tuning voltage.

Assuming the I_{up} is larger than I_{dn}, $t_{dn} = t_{PFD} + t_{diff}$, where t_{diff} is the PFD delay difference between UP and DOWN signals and $t_{up} = t_{PFD}$ as shown in Figure 2. Since charge transfer is zero when PLL is in locked, Equation 14 can be rewritten as

$$\begin{aligned} I_{up}\, t_{up} - I_{dn}\, t_{dn} &= 0\ , \\ I_{up}\, t_{PFD} &= I_{dn}\ (t_{PFD} + t_{diff})\ , \\ t_{diff} &= t_{PFD}\left(\frac{I_{up}}{I_{dn}} - 1\right)\ . \end{aligned} \quad (16)$$

and the VCO tuning voltage is given by Equation 17. If the I_{dn} is larger than I_{up}, $t_{up} = t_{PFD} + t_{diff}$, and $t_{dn} = t_{PFD}$. Equations 16 and 17 are rewritten to Equations 18 and 19, respectively.

$$t_{diff} = t_{PFD}\left(\frac{I_{dn}}{I_{up}} - 1\right)\ . \quad (18)$$

As shown in Equations 16 and 18, t_{diff} has a linear relation with both the charge pump current mismatch and PFD delay. As a result, ΔV is proportional to t_{diff}. A higher t_{diff} results in a higher ΔV in the tuning voltage, hence result in increase the level of reference spur. As shown by Equations 17 and 19, if I_{up} is larger than I_{dn}, the ripple voltage falls slightly lower than the tuning voltage, meanwhile if I_{dn} is larger than I_{up}, the ripple voltage rise slightly higher than the tuning voltage. However, the ripple voltage direction is not important in the reference spur calculation, rather the magnitude of difference is required.

B. Switching delay

Another main cause for the reference spur is the charge pump switching mismatch between UP and DOWN switches. Since UP switch uses a PMOS transistor, an inverter is required to invert signal from PFD. This inverter introduces a delay to the UP signal, hence delays the I_{up} switching. The analysis on how this delay affects ΔV is divided into two categories, depending on the charge pump current.

The first category is when I_{up} is larger than I_{dn}, where t_{dn} = $t_{PFD} + t_{diff}$ and t_{up} = t_{PFD} as shown in Figure 3(a). In this category, the delay caused by the inverter increases ΔV, hence increases the spur level. The second category is when I_{dn} is larger than I_{up}, where t_{up} = $t_{PFD} + t_{diff}$ and t_{dn} = t_{PFD} as shown in Figure 3(b). The delays in UP signal helps to reduce the ΔV amplitude, hence decreases the reference spur level.

The amplitude of ripple voltage affected by the switching delay is given by

$$\Delta V_{t_{delay}}(t) = \frac{1}{C}\int_0^{t_{inv}} I_{cp}\ dt\ . \quad (20)$$

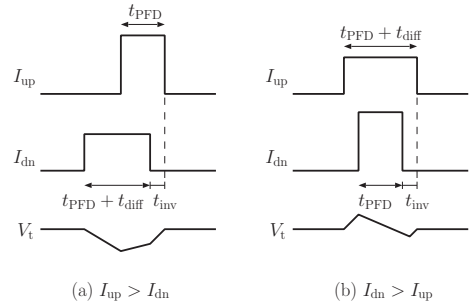

Fig. 3. (a) I_{up} ia larger than I_{dn}: switching delay increases ΔV. (b) I_{dn} ia larger than I_{up}: switching delay compensates the current mismatch and reduces the ΔV.

C. Charge pump rise and fall times characteristic

Charge pump current response also affects the level of reference spur. The size of PMOS and NMOS transistors in the charge pump circuit affect the rise and fall times of the I_{up} and I_{dn}. Also, the different types and sizes of transistors can result in more differences in the rise and fall times. In addition, different loop filter gives a different load to the charge pump, hence affects the rise and fall times characteristic.

Considering the rise and fall times, the charge pump current, I_{up} and I_{dn} can be modelled as i_{up} and i_{dn}, respectively [10]:

$$i_{\mathrm{up}} = \begin{cases} I_{\mathrm{up}} \left(1 - \exp^{\left(\frac{-t}{\tau_{\mathrm{rup}}}\right)}\right). & \text{if } 0 < t \leq t_{\mathrm{up}} \\ K_{\mathrm{up}} \exp^{\left(\frac{-t}{\tau_{\mathrm{fup}}}\right)}. & \text{if } t_{\mathrm{up}} < t \leq t_{\mathrm{ref}} \end{cases} \tag{21}$$

$$i_{\mathrm{dn}} = \begin{cases} I_{\mathrm{dn}} \left(1 - \exp^{\left(\frac{-t}{\tau_{\mathrm{rdn}}}\right)}\right). & \text{if } 0 < t \leq t_{\mathrm{dn}} \\ K_{\mathrm{dn}} \exp^{\left(\frac{-t}{\tau_{\mathrm{fdn}}}\right)}. & \text{if } t_{\mathrm{dn}} < t \leq t_{\mathrm{ref}} \end{cases} \tag{22}$$

where τ_{rup} and τ_{rdn} are rise time for i_{up} and i_{dn}, respectively, while τ_{fup} and τ_{fdn} are fall time for i_{up} and i_{dn}, respectively. t_{ref} is reference clock period and K_{up} and K_{dn} is given by

$$K_{\mathrm{up}} = I_{\mathrm{up}} \left(1 - \exp^{\left(\frac{-t_{\mathrm{up}}}{\tau_{\mathrm{rup}}}\right)}\right). \tag{23}$$

$$K_{\mathrm{dn}} = I_{\mathrm{dn}} \left(1 - \exp^{\left(\frac{-t_{\mathrm{up}}}{\tau_{\mathrm{rdn}}}\right)}\right). \tag{24}$$

The net current flow that goes into the loop filter is given by $i_{\mathrm{up}} - i_{\mathrm{dn}}$. Different rise and fall times between i_{up} and i_{dn} produce ΔV in the VCO tuning voltage.

D. Charge pump current leakage

When both UP and DOWN switches are OFF, a small amount of current leaks to and from the loop filter. The leakage current is due to sub-threshold leakage in the switches and current mirror transistors in the charge pump [11]. The amount of leakage current is also affected by VCO tuning port leakage. Since VCO input impedance is very large, the current leaks to the loop filter [12].

For second order filter, the tuning port shares the same node with charge pump output. Therefore, the current leakage from the VCO tuning port modulates the charge pump current, hence increase the net current goes to the loop filter. As for third order loop filter, the VCO tuning port is only connected to the third capacitor in the loop filter (as shown in Figure 4b). Therefore, the leakage current from the VCO tuning port does not modulates the charge pump current, and does not effect the tuning voltage. Effect of VCO tuning port leakage current can be seen by performing transient analysis to the PLL while replacing the charge pump circuit with a Verilog-A behavioural model. In the charge pump behavioural model, only current mismatch effect is included. The results from the simulation shows that the tuning voltage slightly increase even when both UP and DOWN switches are OFF. Since the behavioural charge pump does not inject any leakage current into the loop filter, so the tuning voltage is only affected by VCO tuning port leakage current that will charge the capacitor in the loop filter.

Current leakage gives a huge effect to the ripple voltage magnitude for the second order loop filter, while only gives a minimum effect to the third order loop filter and can be neglected. Detail discussion on effect of loop filter is presented in the next section.

E. Loop filter

Early in this section, the loop filter is considered as a capacitor. In reality, a second order and third order passive low pass filter are commonly used. Detailed analysis on how these two types of filters affect the VCO tuning voltage is presented in the following paragraphs.

1) Second order low pass filter: Transfer function of a second order low pass filter shown in Figure 4(a), is given by

$$F_2(s) = \frac{R_2 C_2 s + 1}{R_2 C_2 C_1 s^2 + C_1 s + C_2 s}. \tag{25}$$

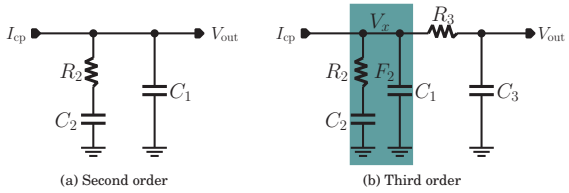

Fig. 4. (a) Second order low pass filter (b) Third order low pass filter

Using Kirchhoff's current law, the current that goes through C_1 branch and R_2C_2 branch can be written as

$$I_{C_1}(s) = \frac{I_{\mathrm{cp}}}{s} \frac{R_2 C_2 C_1 s + C_1}{R_2 C_2 C_1 s + C_1 + C_2}. \tag{26}$$

$$I_{R_2C_2}(s) = \frac{I_{\mathrm{cp}}}{s} \frac{C_2 s}{R_2 C_2 C_1 s + C_1 + C_2}. \tag{27}$$

With $R_2C_2C_1s + C_1 \gg C_2s$, we assume that all current goes to C_1. Therefore, the tuning voltage for PLL with second order loop filter could be presented as:

$$F_3(s) = \frac{R_2C_2s+1}{(R_2C_2C_1s^2+C_1s+C_2s)(R_3C_3s+1)+C_3s(R_2C_2s+1)} . \quad (29)$$

$$I_{F_2}(s) = \frac{I_{\rm cp}}{s}\frac{(R_2C_2C_1s^2+C_1s+C_2s)(R_3C_3s+1)}{(R_2C_2s+1)C_3s+(R_3C_3s+1)(R_2C_2C_1s^2+C_1s+C_2s)} . \quad (30)$$

$$I_{R_3C_3}(s) = \frac{I_{\rm cp}}{s}\frac{C_3s(R_2C_2s+1)}{(R_2C_2s+1)C_3s+(R_3C_3s+1)(R_2C_2C_1s^2+C_1s+C_2s)} . \quad (31)$$

$$V_{\rm tfs2}(t) = \frac{1}{C_1}\int I_{\rm cp}\ dt\ . \quad (28)$$

2) Third order low pass filter: The transfer function of a third order filter shown in Figure 4(b) is given by Equation 29. Using Kirchhoff's current law, the current that goes through F_2 branch and R_3C_3 branch can be written as given by Equations 30 and 31, as shown on the next page.

Since $(R_2C_2C_1s^2 + C_1s + C_2s)(R_3C_3s + 1) \gg C_3s(R_2C_2s+1)$, we assumed all current goes to F_2 branch. As explained earlier, in F_2 branch, all current is assumed to go through C_1 branch. Therefore, node V_x in Figure 4(b) can be calculated using Equation 28. The current through capacitor C_3 is calculated by

$$I_3 = \frac{V_x - V_{\rm out}}{R_3}\ . \quad (32)$$

VCO tuning voltage for third order loop filter can be calculated by:

$$V_{\rm tfs3}(t) = \frac{1}{C_3}\int I_3\ dt\ . \quad (33)$$

F. Tuning Voltage Ripple Magnitude

Tuning voltage ripple magnitude could be calculated by considering all the circuit non-idealities as explained earlier. Firstly, calculate $t_{\rm diff}$ by either Equation 16 or 18, caused by charge pump current mismatch. Then, switching delay with amount of $t_{\rm inv}$ is added to the $I_{\rm up}$. Apply Equations 21 and 22 in order to get the net charge pump current that goes into loop filter. Finally, the tuning voltage ripple can be calculated using Equation 28 for the second order loop filter or Equation 33 for third order loop filter. Effect of charge pump current leakage is added to the ΔV for second order loop filter. As explained in Section III-D, current leakage does not effect on ΔV for third order loop filter.

IV. Analysis Verification

For verification, the results from presented analysis are compared with simulation results using Cadence Spectre tools. Two verifications are conducted, which are reference spur magnitude based on the analysis in the Section II and ripple voltage magnitude as discussed in Section III. For the reference spur magnitude verification, ΔV is obtained from simulation and reference spur is calculated using Equation 13. Meanwhile for ripple voltage verification, ΔV is obtained based on Section III-F.

For the Cadence Spectre simulation, a transistor level transient analysis was performed. To get reference spur magnitude, FFT with length of 2^{19} points was applied to the VCO output and the difference power level at the VCO output frequency and the first reference spur were calculated and converted into decibels.

For spur magnitude verification, ΔV and $K_{\rm vco}$ in the Equation 13 are obtained from transistor level simulation. For ΔV value, the VCO tuning voltage from the transistor level transient analysis is plotted. Meanwhile, $K_{\rm vco}$ is attained by plotting tuning voltage versus VCO output frequency using Periodic Steady State (PSS) analysis in Cadence SpectreRF. Gradient of the graph at each tuning voltage is the $K_{\rm vco}$ for that particular tuning voltage. These values are then applied to Equation 13 and the results are plotted on Figures 5 and 6, for second and third order loop filters, respectively.

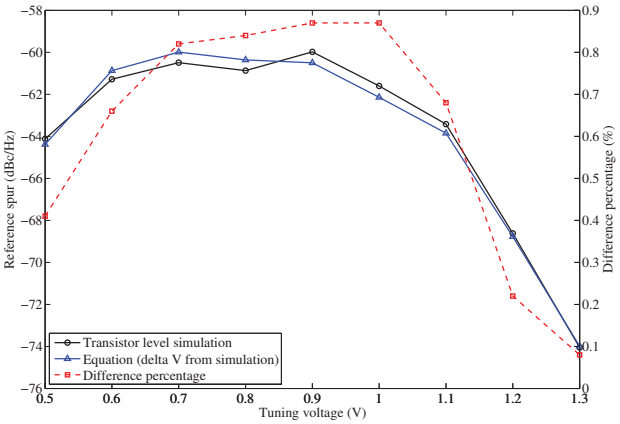

Fig. 5. Comparison reference spur level from simulation and presented model for PLL with second order loop filter.

Figures 5 and 6 show that the proposed analysis accurately calculate the reference spur magnitude, with difference percentage of less than 1%. Comparing between these two figures show that with the same loop bandwidth and phase margin, third order loop filter gives a lower reference spur magnitude.

For ripple voltage verification, ΔV is obtained based on procedure as discussed in Section III-F. The $K_{\rm vco}$ is attained by the same means as discussed in previous paragraph. Both ΔV and $K_{\rm vco}$ values are then inserted into Equation 13 and the results are plotted in Figures 7 and 8, for second and third order loop filter, respectively.

As shown in Figures 7 and 8, comparison between spur

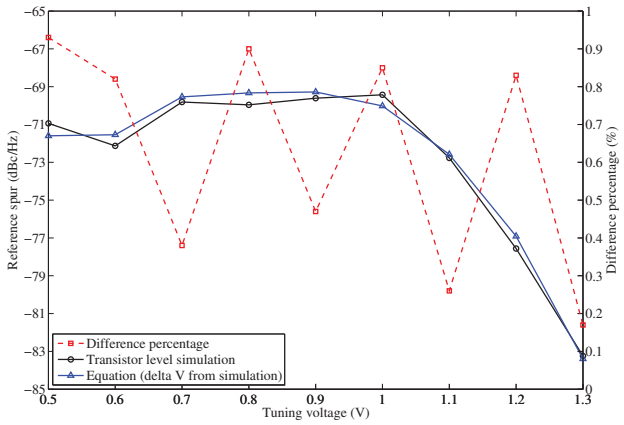

Fig. 6. Comparison reference spur level from simulation and presented model for PLL with third order loop filter.

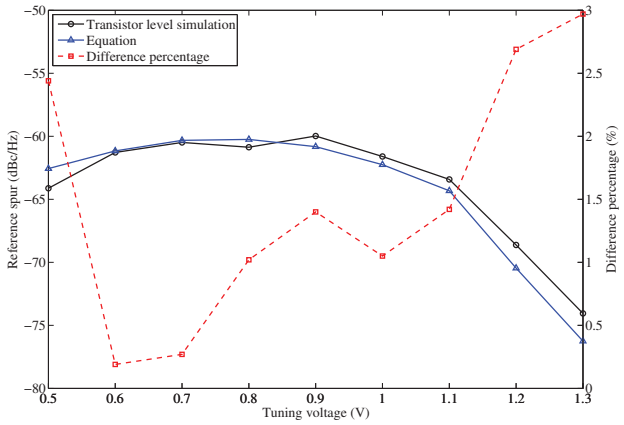

Fig. 7. ΔV model verification for second order loop filter.

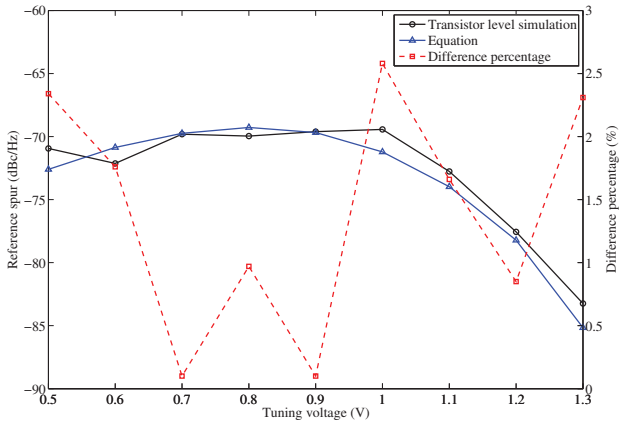

Fig. 8. ΔV model verification for third order loop filter.

magnitude using the proposed analysis for ΔV estimation and FFT from transistor level transient analysis gives less than 3% difference.

V. Conclusion

A reference spur analysis for an integer-N PLL is presented. The analysis accurately predicts reference spur level in the PLL output. In addition, ripple in VCO tuning voltage (ΔV) is also modelled. The reference spur magnitude and ΔV analysis are verified by comparing the results with transistor level simulation. For the spur magnitude verification, the difference between analysis and transistor level simulation is less than 1%, while for ΔV verification the difference is less than 3%.

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