On-chip Current Sensing Circuit for Current-limited Minimum Off-time PFM Boost Converter

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Abstract—**An on-chip current sensing circuit for current-limited minimum off-time pulse frequency modulation (PFM) boost converter is designed and verified by SPICE simulations. The current mirror pair, power and sensing MOSFETs with size ratio of *K*, is used in our on-chip current sensing circuit. Very low drain voltages of the current mirror pair should be matched to give accurate current sensing, so a folded-cascode opamp with a PMOS input pair is used in our design. Simulation results show that current sensing is accurate with properly frequency compensated opamp; over-compensation results in inaccuracies in current sensing.**

Keywords-Boost converter, pulse frequency modulation, current-sensing circuit, minimum off-time, current-limited.

I. INTRODUCTION

There are two control topologies for DC-DC converters: the pulse width modulation (PWM) control and pulse frequency modulation (PFM) control [1]. For moderate to heavy loads, PWM controlled converters are usually used due to its higher efficiency. Also, PWM converters have less output ripple voltage and smaller external components (*L* and *C*) by choosing higher switching frequency. But, PWM converters require more than 2 external components for compensating the closed-loop feedback system. For example, 6 external components are required for type III frequency compensation of voltage-mode buck converter [2]. For light loads such as the application with power saving mode, the efficiency of PWM converters decreases due to switching and gate drive loss. In this case of light loads, the PFM controllers have higher efficiency compared to PWM converters because PFM converters use low switching frequency for light loads, therefore the switching loss can be minimized. Also PFM converters do not need explicit frequency compensation because compensation is done through changing the switching frequency. Therefore for the application such as portable equipment operating in the power saving mode, PFM converter is more suitable than PWM converter.

The current-limited minimum-off-time PFM [3] as shown in Fig. 1 is one of widely used PFM schemes because of its simpler topology and merits mentioned in the previous paragraph. In this PFM controller, the peak output current sensing is very important for reliable system operation and there are lots of techniques to sense the peak MOSFET current. In this paper an on-chip current sensing circuit for the current-limited minimum-off-time PFM boost converter is designed and verified by SPICE simulations.

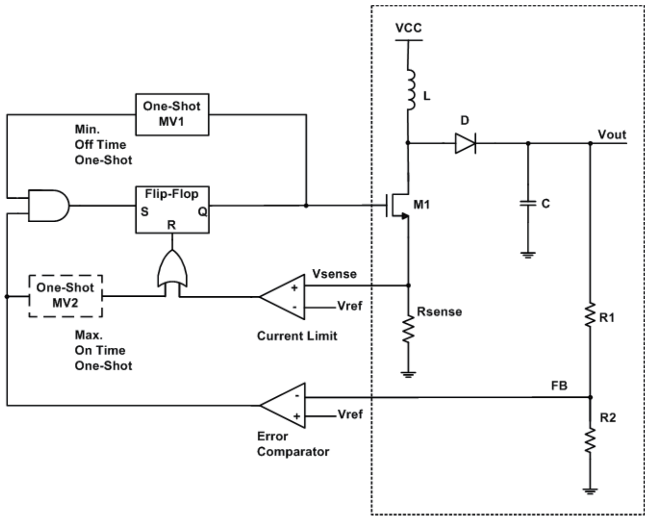

Fig. 1. Current-limited minimum off-time PFM.

II. CURRENT-LIMITED MINIMUM OFF-TIME PFM BOOST CONVERTER

The current-limited minimum-off-time PFM converter as shown in Fig. 1 has a simple topology compared to the PWM converters requiring the frequency compensation network. The output voltage is divided by resistors R1 and R2 and the voltage across R2 (the voltage at FB node) is applied to the error comparator of the PFM controller. If the voltage at FB node drops below the bandgap reference voltage, the output of error comparator goes high and sets the SR flip-flop to turn on the power MOSFET. The SR flip-flop can be reset to turn-off the power MOSFET by two conditions: the peak MOSFET current I_{max} reaching the critical point – maximum allowable current through the power MOSFET and the triggering of maximum on-time one-shot multivibrator. The maximum on-time one-shot multivibrator MV2 may not be necessary due to its dependence on maximum peak current by

$t_{\max-on-time} = L \bullet I_{\max} / V_{CC}$, i. e., limiting maximum peak current also setting the maximum on-time. When one or both conditions are met, the SR flip-flop is reset and the power MOSFET is turned-off. The turn-off of the power MOSFET then triggers the minimum off-time one-shot multivibrator MV1. After the minimum off-time, one input to AND logic is high and thus the SR flip-flop is ready to accept a set signal from the output of error comparator. When the voltage at FB node is lower than the bandgap reference voltage, the SR flip-flop is set and the power MOSFET is again turned on, otherwise the power MOSFET remains OFF until the FB voltage drops below the bandgap reference voltage. This cycle repeats itself.

III. ON-CHIP CURRENT SENSING CIRCUIT

There are many current-sensing techniques for DC-DC converters [4], [5]. A small sensing resistor can be inserted into the source of the power MOSFET as shown in Fig. 1. This method is very simple, but a power loss in R_{sense} is unavoidable and therefore reduces the efficiency of the DC-DC converter. Another method of current sensing is measuring the drain-source voltage of the power MOSFET, provided that the drain-source resistance RDS ($= \dfrac{L}{W \mu C_{ox}(V_{GS} - V_{TH})}$) of M1 in the triode region during the on-period is known. This technique is not accurate; the RDS has significant process variations due to process-sensitive parameters, μ, C_{ox}, V_{TH} . Even though these problems can not be solved, commercial products usually use this technique due to its lossless property. There are other methods such as filtering the voltage across the inductor, measuring the inductor voltage to sense the current, average current-sensing technique, or using current-sensing transformers in high power systems. The current transformer is neither cost- nor size-effective and can not be integrated into the controller. Another method is using a current sensing transistor in parallel with the power MOSFET [6]-[8]. This method is lossless and can be easily integrated into the controller chip.

In this paper a current sensing transistor is used to monitor the peak current flowing through the power MOSFET. The on-chip current sensing circuit for the current-limited minimum off-time PFM boost converter is shown in Fig. 2. The power MOSFET M1 and the current sensing transistor M2, whose size ratio is K : 1 (in our design, K = 5000), are the current mirror pair during the on-period of the power MOSFET. To get an accurate current sensing, the drain voltages of M1 and M2 should be matched. For this purpose a feedback network using an operational amplifier and the load transistor M3 is used in our current sensing circuit. A general purpose op-amp can not be used in this application because drain voltages of M1 and M2, connected to the inputs of op-amp, are very low values near zero during the on-period. In our design a folded-cascode structure with a PMOS differential input pair is used. Input common-mode voltages of this op-amp can be as low as zero due to the PMOS input pair and current source load of the folded-cascode structure. During the off-period (Qb in Fig. 2 is high), transistor M5 is turned on to set input voltages of op-amp to zero, therefore the sensed current is set to zero and transistor M6 is used to disconnect the negative input node of the op-amp from the high drain voltage of M1. During the on-period period (Q in Fig. 2 is high), M6 is turned on to connect the negative input node of op-amp to the drain of M1. Bias current I_0 is chosen to be very small to make the drain-source voltage of M6 small, so that the drain voltage of M1 is approximately equal to the negative input voltage of op-amp during the on-period. The sensed peak MOSFET current is flowing through M2, M3, then M4 and R_{sense}. The sensed current is converted to a voltage across R_{sense} (= 12.5 kΩ) and then compared to the bandgap reference voltage. If the sensed current is larger than I_{max}/K, the output of current limiter comparator in Fig. 1 is high to generate a reset signal for the RS flip-flop.

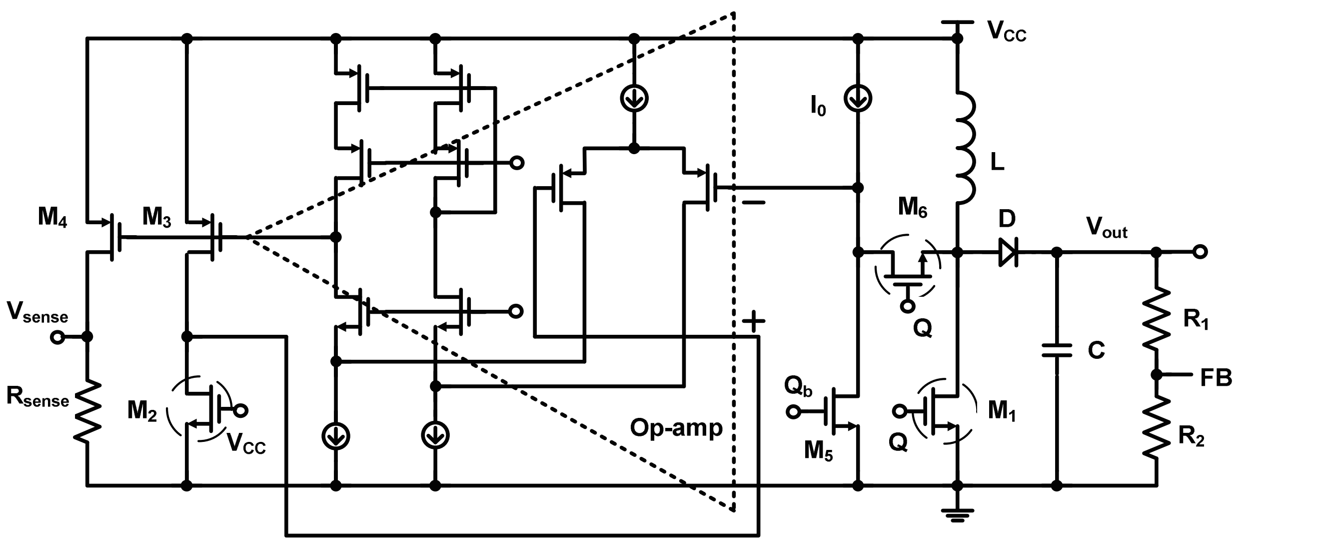

Fig. 2. On-chip current sensing circuit for current-limited minimum off-time PFM boost converter. This figure represents dotted box in Fig. 1. ◌ is high voltage MOSFET.

IV. Verifications Using SPICE Simulations

The on-chip current sensing circuit for the current-limited minimum off-time PFM boost converter was verified by SPICE simulations using the high-voltage 0.5 µm CMOS process. Design specifications of the boost converter are V_{CC} = 5.0 V, V_{out} = 20 V, and I_{out} = 20 mA. SPICE simulation results are shown in Figs. 3-7. Fig. 3 shows power MOSFET gate and boosted output voltages for the current-limited minimum off-time PFM boost converter with the on-chip current-sensing circuit. During initial pumping to the specified output voltage, the frequency of the MOSFET gate voltage is high and once the output voltage is reached to the target voltage, then its frequency becomes low, which enables to achieve enhanced efficiency at light loads. Note that the output voltage ripple is large due to the hysteresis window of the error comparator. This ripple can be reduced by decreasing the hysteresis window of the error comparator, but cannot be eliminated.

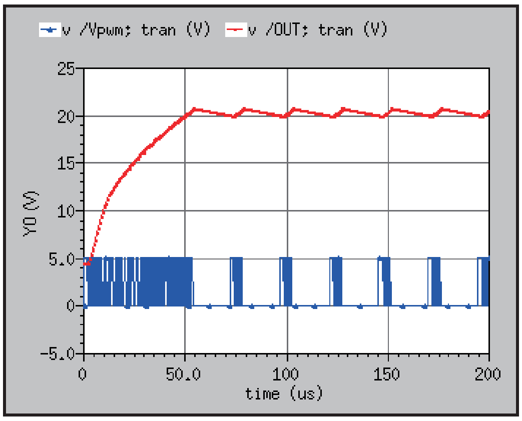

Fig. 3. MOSFET gate and output voltages for current-limited minimum off-time PFM boost converter with the on-chip current-sensing circuit.

Fig. 4 shows set and reset signals of the RS flip-flop, power MOSFET gate and output voltages during voltage boosting operation of the PFM boost converter. The maximum on-time is about 5 µs set by the $v=L*di/dt$ at maximum peak current of 0.5 A. The minimum off-time is about 0.3 µs set by the internal delay element using the capacitor and current source.

Fig. 5 shows the drain voltages of the power MOSFET M1 and current-sensing transistor M2. These voltages are exactly matched by the folded-cascode op-amp for accurate current-sensing. During the off-period the drain of M6 is shorted to ground by transistor M5. But due to the limited size of M5 the drain-source voltage of M5 is about several mV. Note that the maximum drain voltages of M1 and M2 are about 175 mV. This is why we should be careful when designing the op-amp. Parasitic bipolar transistors are used in [5], but in our design a simple PMOS differential input folded-cascode opamp is used.

Fig. 6 shows power MOSFET drain current and sensed current multiplied by the size factor K. This result verifies the operation of current sensing circuit for PFM boost converter. The op-amp needs frequency compensation for stable voltage-follower operation, but adequate compensation load capacitor needs to be used to avoid any current-sensing inaccuracies (in our design, C_L = 0.5 pF), in case of over-compensation the current-sensing is not accurate. For example, in case of C_L = 5 pF (it is good enough for compensation purpose), but Fig. 7

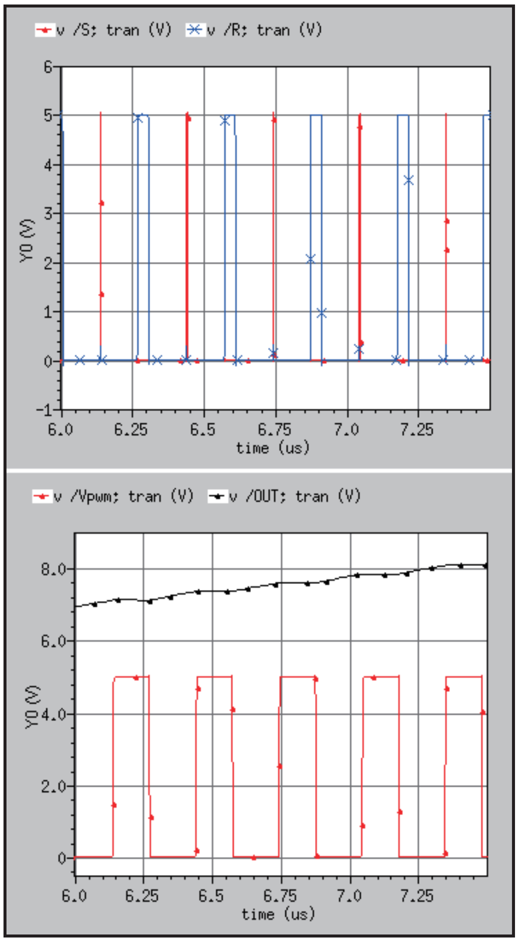

Fig. 4. Set and reset signals of the RS flip-flop, MOSFET gate and output voltages.

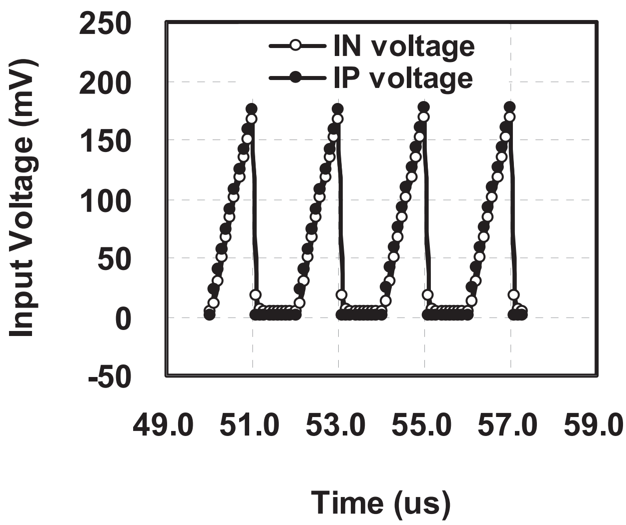

Fig. 5. Input voltages of opamp.

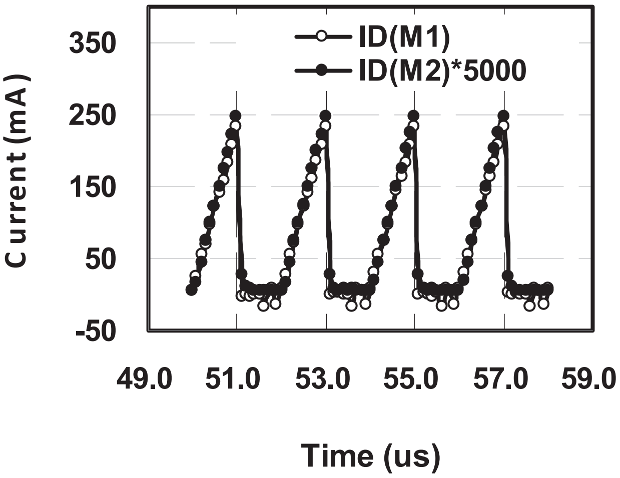

Fig. 6. Power MOSFET drain current and sensed current multiplied by the size factor K for $C_L = 0.5$ pF.

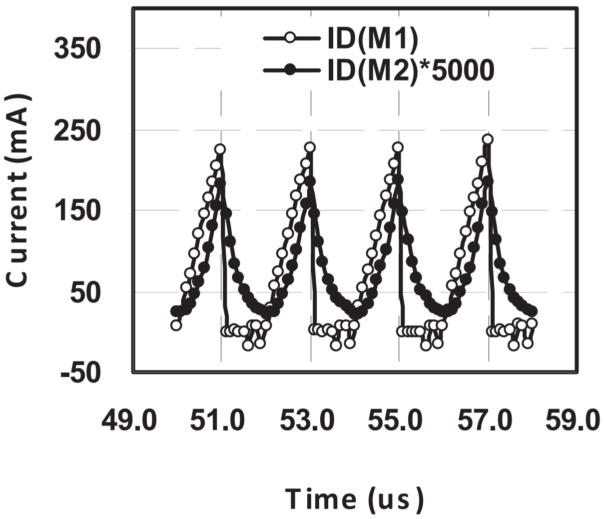

Fig. 7. Power MOSFET drain current and sensed current multiplied by the size factor K for $C_L = 5$ pF.

shows the current sensing circuit is not accurate.

V. SUMMARY

An on-chip current sensing circuit for current-limited minimum off-time PFM boost converter is designed and verified by SPICE simulations. SPICE simulations show that drain voltages of power and current-sensing MOSFETs are matched by the folded-cascode opamp and therefore sensed current multiplied by the size ratio is exactly equal to drain current of power MOSFET. It is also shown that too much frequency compensation of opamp in the current-sensing circuit gives inaccurate current-sensing. This current-sensing circuit for current-limited minimum off-time PFM boost converter can be used for the power supply with power saving mode.

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