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Triplet-based spike-timing dependent plasticity in silicon

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Abstract— In this paper, we present a new triplet based STDP VLSI implementation, based on a previous published pair-based STDP circuit [1]. Simulation results illustrate that the proposed VLSI circuit can reproduce similar results to those observed in various physiological STDP experiments [2–4], while the traditional pair-based VLSI implementation fails to do so [2].

Keywords— Synaptic Plasticity, Spike Timing Dependent Plasticity, Spike Triplet, VLSI Implementation

1 Introduction

Implementation of STDP into VLSI has drawn the attention of many researchers during the past decade. STDP alters the synaptic weight depending on the timing difference between spikes. This can be the timing difference between pre- and postsynaptic spikes (pair-based STDP or pSTDP) or the timing differences between spikes of higher order patterns, e.g. triplet and quadruplet patterns [2]. Previous studies have reported the failure of pSTDP to reproduce the experimental outcomes when stimulation is provided by patterns consisting of triplet or quadruplet of spikes or the effect of increasing repetition frequency of pairs of spikes [2–4]. In 2006, Pfister and Gerstner introduced a new spike triplet-based STDP (tSTDP) rule [2] which succeeded in reproducing observed experimental measurments.

This paper proposes the first VLSI implementation of the tSTDP rule presented in [2] and demonstrates how the proposed implementation is capable of reproducing the physiological experiments reported in [2–4]. The proposed tSTDP circuit is based upon an extension to the STDP circuit presented by Indiveri *et al.* [1]. Although there are several VLSI implementation of pSTDP in the literature [1, 5], we selected this circuit due to its low-power and small area features.

2 Spike-Timing Dependent Plasticity

In pSTDP, potentiation occurs when a pre-synaptic spike precedes a post-synaptic spike; otherwise depression occurs, where weight changes can be governed by a temporal learning window. In tSTDP, however, synaptic weight change is the result of interaction between triplet of spikes (pre-post-pre or post-pre-post). The pre-post-pre combination of spikes can result in depression, while the other combination (e.g. post-pre-post) can lead to potentiation. Next section gives more explanation on tSTDP rule while describing how the proposed circuit acts to mimic tSTDP behaviour. For further details on the learning rule and its eight various parameters, the reader is referred to [2].

3 VLSI Implementation of tSTDP

In the triplet model, a pre-synaptic (post-synaptic) spike have an effect on its successive post-synaptic (pre-synaptic) spike and can also have an effect on its consecutive pre-synaptic (post-synaptic) spike(s). In order to have these new effects in the proposed triplet circuit, two more pulses, $V_{\text{post}(n-1)}$ and $\overline{V}_{\text{pre}(n-1)}$, were added which show the extra post/pre required spike in addition to $\overline{V}_{\text{post}(n)}$ and $V_{\text{pre}(n)}$ (Fig. 1). These extra pulses are for implementing same-type spike interaction (e.g. pre-pre or post-post) which leads to producing the nonlinearity in the triplet-based model [2].

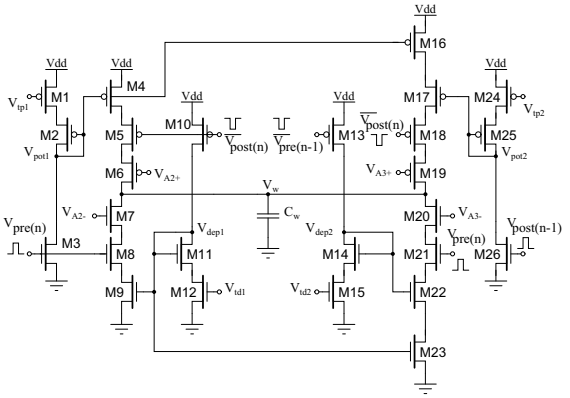

Figure 1: Proposed VLSI implementation of triplet-based STDP.

The circuit works as follows: upon the arrival of a post-synaptic pulse, $\overline{V}_{\text{post}(n)}$, the M5, M10 and M18 transistor switches turn on. Then M10 sets a depotentiating voltage V_{dep1} to V_{dd}. This voltage then starts decaying linearly in time which can result in depression, if a pre-synaptic pulse, $V_{\text{pre}(n)}$ arrives during the time V_{dep1} is decaying to zero (τ_- time constant). In this situation, C_w will be discharged through M7-M9 by a current that is limited by the M7 bias voltage ($V_{\text{A}_2^-}$). In contrast to M10, M5 and M18 can lead to two different potentiations. The first one can occur if M5 turns on during time constant of V_{pot1} (τ_+). This potentiation will be through M4-M6 and is proportional to the bias voltage at M6 ($V_{\text{A}_2^+}$). The second potentiation term can charge C_w through M16-M19 and is proportional to $V_{\text{A}_3^+}$ if M18 is on at the required time, i.e. when V_{pot1} and V_{pot2} keep M16 and M17 on. This is the term that distinguishes triplet from pair-based STDP. Similarly, upon the arrival of a pre-synaptic pulse, $V_{\text{pre}(n)}$, a potentiating voltage V_{pot} is set to zero and starts to increase linearly in time which can result in potentiation when a $\overline{V}_{\text{post}(n)}$ pulse arrives within the τ_+ time constant. In addition,

two possible depressions proportional to A_2^- and A_3^- can take place, if this pre-synaptic pulse is in the interval area of effect of V_{dep1} and V_{dep2}, i.e. in τ_- and τ_x time constants. It is worth mentioning that the required time constants in the proposed circuit, τ_-, τ_+, τ_x and τ_y, can be easily adjusted by altering their corresponding bias voltages, V_{td1}, V_{tp1}, V_{td2} and V_{tp2}.

4 Experimental Setup

In order to have consistent circuit experiments with the physiological experiments reported in [2–4], the experimental protocols and experimental data sets that were used in [2] were also adopted in the present study. Identical to [2], two data sets were selected for carrying out the experiments. The first data set originates from experiments on the visual cortex [3] that investigated how altering the repetition frequency of spike pairings affects the overall synaptic weight change. This data set is presented in Table 1 of [2], consists of 5 different frequencies for two different Δt values and under pairing protocol in the visual cortex (See five distinguished points with error bars in Fig. 2(a)). The other experimental data set that was utilized, originates from hippocampal culture experiments from [4] which examined pairing, triplet and quadruplet protocols effects on synaptic weight change. This data set is manifested in Table 2 of [2]. In addition, similar experimental protocols to those employed in [2] were used while simulating the proposed circuit.

5 Circuit Simulation Results

The tSTDP circuit uses eight different bias voltages to control the parameters associated with the spike-triplet learning rule. These voltages were adjusted in order to obtain weight changes akin to those seen in experiments [2–4]. Parameter adjustments were conducted to achieve the smallest Normalized Mean Square Error (NMSE), like Eq. 5 in [2].

Simulation results shown in Fig. 2(a)-(d) demonstrate that the proposed VLSI triplet-based circuit has a good capability in mimicking biological experiments. In contrast, our simulation results (not presented here) for a pSTDP circuit show that it fails to mimic biological behaviours as it is the case for the pSTDP model [2]. The NMSE achieved for tSTDP circuit and using the first data set (Fig. 2(a)), was $E = 0.82$, which is fairly close to the analytical calculation of the triplet-based model given in [2] ($E = 0.22$, data obtained from Table 3 in [2]). In addition, results for the triplet-based circuit, stimulated using the second data set (quadruplet and the triplet protocols), are shown in Fig. 2(b)-(d). The minimal NMSE for the second data set using the proposed triplet circuit was $E = 3.46$ which is consistent with the full-triplet model presented in [2] using analytical calculations ($E = 2.9$, data obtained from Table 3 of [2]).

6 Conclusion

The proposed STDP circuit demonstrates its ability in mimicking some complicated biological experiments while the pair-based circuit is unable to reproduce observed results. Since the proposed circuit leads to better synaptic weight modification capability in comparison to its classical counterpart (pSTDP circuit), it would lead to more realistic physical implementation of synaptic modification rules. These rules in turn can be used to train networks of VLSI spiking neurons to perform various tasks including pattern classification and learning cross-modal spatial transformations, an important task involved in the multisensory integration [6].

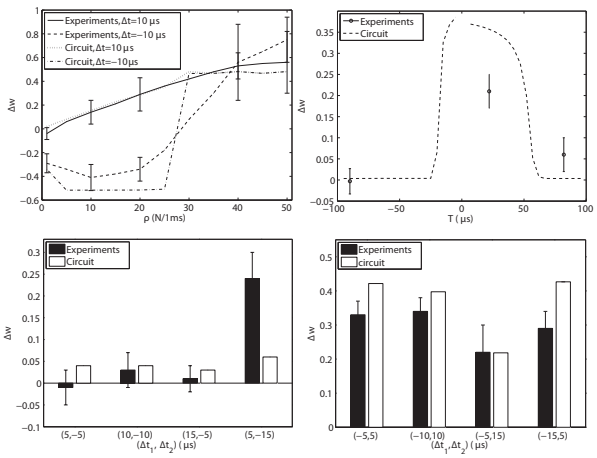

Figure 2: Triplet-based STDP circuit experiments. (a) Pairing protocol applied to the circuit for various spike-pair frequencies. (b) Quadruplet protocol applied to the circuit for various Ts. (c) and (d) Triplet protocols applied to the circuit for various delays. The values of ρ, T and Δt are used as described in [2].

References

[1] Indiveri, G., Chicca, E., & Douglas, R. (2006). A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity. *IEEE Transactions on Neural Networks*, vol. 17, no. 1, pp. 211-221.

[2] Pfister, J.P., & Gerstner, W. (2006). Triplets of spikes in a model of spike timing-dependent plasticity. *The Journal of Neuroscience*, vol. 26, no. 38, pp. 9673–9682.

[3] Sjöström, P.J. & Turrigiano, G.G. and Nelson, S.B. (2001). Rate, timing, and cooperativity jointly determine cortical synaptic plasticity. *Neuron*, vol. 32, no. 6, pp. 61149–1164.

[4] Wang, H.X. and Gerkin, R.C. and Nauen, D.W. and Bi, G.Q. (2005). Coactivation and timing-dependent integration of synaptic potentiation and depression. *Nature Neuroscience*, vol. 8, no. 2, pp. 61149–1164.

[5] Tanaka, H. and Morie, T. and Aihara, K. (2009). A CMOS spiking neural network circuit with symmetric/asymmetric STDP function. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E92-A, no. 7, pp. 1690–1698.

[6] Davison, A.P. and Frégnac, Y. (2006). Learning cross-modal spatial transformations through spike timing-dependent plasticity. *The Journal of Neuroscience*, vol. 26, no. 21, pp. 5604–5615.