# Towards the Realisation of an Interactive Mobile Multimedia Personal Communicator (IM$^3$PC)

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**Mobile phone handsets of the future will be able to communicate with multiple service networks. The handset will become a portable terminal for not only voice, but for video, banking and various other information services. This will be the new IM$^3$PC paradigm. In this paper we discuss the issue involved towards the hardware realisation of such systems.**

## 1 Introduction

Personal communication systems of the future will augment the mobile phone concept to include multimedia services such as: digitised speech, data, e-mail, paging, fax, GPS, still image compression, compressed/slow scan video and eventually real-time video. The many potential applications for this technology include use of mobile telecommunications in areas of telepresence such as telemedicine, teleworking, telebanking, teleshopping, teleconferencing, personal communication/navigation, and tele-education. This range of services will lead to the development of interactive mobile multimedia personal communicators (IM$^3$PCs) that require the integration of many sub-systems including real-time image and signal processors, computer vision, RF communications links, and high-speed networks. These systems demand very high speed processing, small physical size and low power consumption and in the next five years demand for such a combination of processor attributes will increase.

We have a further vision driving this concept: ideally future IM$^3$PCs will embrace further paradigms including:

- *Interactive Telebanking (ITB):* the IM$^3$PC will have an option to replace plastic cards. On entering a PIN into the phone, shopping transactions can automatically take place and the user's final bank balance can be checked on the phone's display.
- *Interactive Time Keeping (ITK):* the time will be displayed on the screen of the IM$^3$PC. The displayed time will automatically change for daylight saving and during interstate travel through different time zones. For international travel, the displayed time will interactively speed up or even go backwards!
- *Interactive Personal Navigation (IPN):* when a 'locate' button is depressed on the phone, the nearest street name that you are located to will be displayed. This essentially becomes a smart hand-held global positioning system (GPS).
- *Interactive Personal Video (IPV):* via an image sensor installed on the IM$^3$PC, the user can transmit any real-time image.

To enable a full public access system, the IM$^3$PC handset will require a BISDN microcell network infrastructure to be put into place. Therefore a possible shorter term commercialisation strategy is to choose

a subset of these functions for operation within a wireless local area network (LAN) office environment with a localised degree of mobility – for mobile teleworking and teleconferencing applications. Given this first step, an enormous opportunity exists for companies that can exploit the underlying microelectronics technology to provide IM$^3$PCs at a price acceptable to the business community. In particular, the following sub-systems must form part of any IM$^3$PC and their integration represents the major hurdle to realisation of IM$^3$PC technology:

- high-speed high-density RAM;
- very high-speed video compressor;
- very high-speed modulo multiplier encoder/decoder circuit;
- solid-state imager ('camera-on-a-chip');
- integrated RF/digital circuitry for wireless communication.

To facilitate hardware realisation and integration of these system elements, advances in both technology and implementation are required. This paper will review the above subsystems. Also, we have developed a software 'demonstrator' of the IM$^3$PC, where transmission occurs over a standard computer network.

## 2 Integrated Circuit Technology

IM$^3$PCs impose enormous demands on the system designer for both compactness and low power performance. To this end the best strategy is to integrate all sub-systems into one common IC technology.

Consequently, we have identified the complementary gallium arsenide integrated circuit process as the most advanced production-ready technology that can provide the integration of both RF and high-speed digital functions. Complementary GaAs incorporates both n-type and p-type pseudomorphic high electron mobility transistors (P-HEMTs). Furthermore, a semi-insulating layer is inserted under the gate to reduce gate leakage and this type of transistor is referred to as the HIGFET. Hole mobility in these transistors has been found to be very much higher than in MESFETs [1], enabling CMOS-like gates to be built from dual networks of n-type and p-type transistors that have power dissipations two orders of magnitude lower than gates built from MESFETs. Consequently, Complementary GaAs overcomes the major difficulty associated with using gallium arsenide to fabricate integrated circuits – namely, its much higher power dissipation than silicon CMOS – permitting the integration of millions of very high-speed P-HEMTs onto one chip, offering system performances equivalent to CMOS for lower power dissipation or superior system performances for the same power dissipation.

## 3 State-of-the-Art

Internationally, many researchers have proposed and realised desk top multimedia applications; such as in [2, 3, 4]. Mobile or wireless multimedia has been considered, such as in [5] and [6], proposing various algorithms for efficiently processing the data. However, there is little work specifically addressing the hardware issue of a compact and low power hand-held IM$^3$PC device – this is due to speed-power limitations in the current VLSI technology.

## 4 High-Density High-Speed RAM

Sophisticated memory structures are required to implement data compression algorithms – eg. transpose memory. Also, cryptographic processing requires scratch-pad memory for partial results storage, and each frame captured by the imager will require a frame buffer. GaAs VLSI has long suffered from the high gate leakage current exhibited by MESFETs, so that GaAs RAM cells have been typically static in design. We have developed a 3-transistor dynamic RAM cell design, suitable for MESFET technology, that is smaller and less power-hungry than the static RAM cell [7].

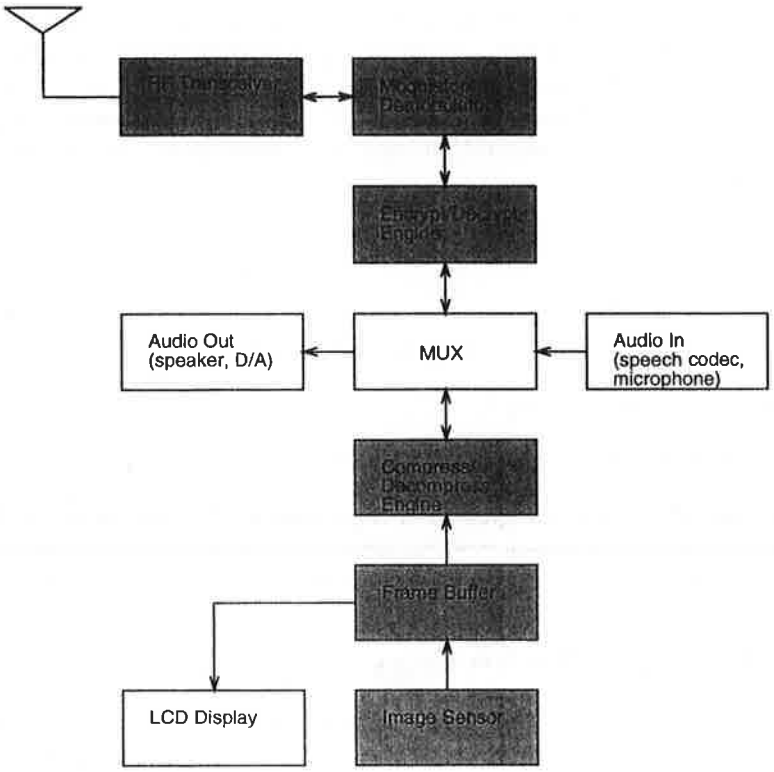


Figure 1: System block diagram for basic mobile video device. Unshaded areas are standard tasks. Shaded areas need to be particularly addressed by C-GaAs solutions.

# 5 Image compression

Compressed video is critical to the development of multimedia applications, because the storage requirements and associated transmission times for uncompressed images (still or video) are prohibitive. Image compression methods reduce the amount of data that needs to be transmitted and stored and in recent years, there has been significant progress towards the development of image compression standards:

- CCITT H.261 for tele-conferencing
- ISO JPEG for high quality still image storage and retrieval
- ISO MPEG I for interactive video playback
- ISO MPEG II for entertainment quality video distribution

All of these standards employ transform coding based on the Discrete Cosine Transform (DCT) to remove spatial redundancy in the image data. The DCT is the most demanding part of the video encoding/decoding process in terms of the number of arithmetic operations required citeackland94. Our strategy has been to not consider Motion Compensation or Interpolation techniques because in the applications intended, there will be little variation between succeeding frames, so that only Frame Differencing need be employed to further reduce the amount of transmitted data. Our preliminary experiments show that using frame differencing only (and dispensing with interpolation and motion estimation) greatly reduces the complexity of video compression circuits for only a 3% increase in the compressed image data size.

# 6 Modulo Multiplier for Encryption

Global digital communications networks are growing at an exponential rate to facilitate the electronic transfer of data in areas as diverse as entertainment, business, law, government, personal communication,

and banking, to name but a few. Data transmitted over these networks will often be of a sensitive nature and hence security of transmitted data is becoming increasingly important. Data coding is employed to provide security and authentication of data: transmitted data must not be intercepted and deciphered by anyone unauthorised to do so; data to be transmitted must be 'signed' so that fake received messages may not be invented by a receiver nor real sent messages disowned by a sender. Since its invention in 1978, RSA coding has been widely accepted as the best means of implementing public-key coding systems. For example, the Australian Standard for Electronic Data Transfer, AS28095.5.3 specifies RSA. It will be more widely used still in virtually all forms of secure data transmission now that the U.S. Government has accepted that RSA provides a means for electronically 'signing' a document for electronic transmission.

Specifically, the existing work has shown that radix-64 ('6 bits at a time') modulo exponentiation minimises the number of multiplications to perform an exponentiation of any length. The existing work has also found that use of Montgomery's modulo multiplication algorithm [9] enables long word length (512 bit) modulo multiplication rates in excess of 10 MHz to be achieved. (We are currently investigating a modification of Montgomery's algorithm to facilitate modulo squaring of long word length numbers, which is also needed in RSA processing.) We show that a combination of these two techniques leads to 512-bit processing on C-GaAs in excess of 1 Mb/s, in comparison with a silicon-based processing rate of 64 kb/s [10].

# 7 Solid-State Imager

The key reason for developing the sensor using a digital GaAs IC process is the facility to integrate this sensor with a digital GaAs preprocessor for low-level vision tasks such as thresholding, contrast enhancement, edge detection, etc. and/or data compression for remote communication. The advantage of a GaAs preprocessor is to meet the demands for ever increasing speed-power performance. Improved speed-power together with the increased compactness, from the circuit integration, suits advanced mobile applications well with their demand for minimal power consumption.

Our work on GaAs solid-state imagers to date includes extensive laser-based optical characterisation of both GaAs and C-GaAs detectors, extensive design and simulation studies of imager read-out circuitry, theoretical modelling of photo-detector characteristics and full noise analysis of imager output amplifier circuitry. This work uncovered the superiority of GaAs over Si especially with regard to spatial resolution [11], photo-collection efficiency, and anti-blooming capability [12]. However, conventional GaAs MESFETs displayed disappointing levels of shot noise in the imager output circuit. This problem is totally solved by the move to C-GaAs that uses a semi-insulating gate that dramatically reduces the gate leakage current and hence shot noise levels. We estimate that CGaAs' is ultimately expected to produce an overall factor of 10 improvement in noise performance over Si [13]

The results of our research on imagers in GaAs apply equally to C-GaAs because all the anticipated benefits still hold for C-GaAs. However C-GaAs has the added advantage that proper pass gates are realisable, thus solving the problem of threshold voltage drops within the imager. The semi-insulating gate also permits use of capacitive bootstrapped circuit techniques in the address circuitry, if desired, to provide variable pulse height control (this may be useful in the early stages of optimising the imager's performance). Finally it should be noted that the C-GaAs process is truly planar, with no gate recess etching, thus providing the perfect medium for imager design work.

# 8 RF/digital interface

C-GaAs also offers the prospect of integrating RF and digital circuit onto one chip – a degree of integration not readily achieved in silicon technology. This would represent a major step forward in IM$^3$PC technology because the number of chips needed in a communicator would be reduced if some RF and digital functions can be placed on the same chip. Most power consumption in a chip is due to the i/o pads, which house relatively high power pad drivers. If there are fewer chips in a system, there will be fewer pads and consequently a lower power demand. Such a reduction in power requirements is vital to IM$^3$PC technology because it leads to longer battery life, as well as increased reliability and a reduction in size and weight.

Direct digital down conversion using under-sampled analog-to-digital converters removes all the IF circuitry found in a conventional superheterodyne receiver. None have been realised in silicon to date because sample-and-hold circuits with a sufficiently quick switching rate may not be realised in CMOS owing to the inadequate $f_t$ of currently available MOSFETs (silicon MOSFETs would need a channel length of <0.25 $\mu$m to be acceptable [14]). The HIGFETs found in 0.7 $\mu$m C-GaAs circuits have an $f_t$ of 20 GHz, comfortably exceeding that required for direct RF down conversion using an under sampled ADC.

# 9 Conclusion

We have highlighted our vision and have defined a number of paradigms for future IM$^3$PC systems.

In conclusion, we have outlined the main hardware requirements for future IM$^3$PC and have identified a number of solutions based on complementary GaAs technology.

# 10 Acknowledgements

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