Improved Image Sensor for HDTV

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Silicon image sensors suffer from minority carrier diffusion lengths as high as 200-400 μm. In contrast, SI GaAs substrates have short carrier diffusion lengths below 10 μm. This is attractive for HDTV sensors with small pixel sizes in the order of 10 μm. Unfortunately, GaAs MESFETs show disappointing levels of shot noise. A number of solutions are proposed, including a shift towards GaAs HIGFET technology.

1   Introduction

Presently HDTV sensors are exclusively fabricated in silicon based technology. There are of the order of 1000 by 1000 pixels in such sensors, thus the pixel pitch tends to be of the order of a few microns — whereas, the minority carrier diffusion length, in silicon, can be as much as 200-400 μm for typical substrates. This large figure, in comparison to the pixel pitch, leads to crosstalk and degradation of spatial resolution – this is valid for conventional image sensors and worsens with the move to HDTV. Traditionally, this problem is controlled by the use of epitaxial substrates, but this is at the expense of reduced responsivity. Currently silicon epitaxial layers can be in the order of 20 μm · but any further decrease in this thickness would overly degrade the responsivity.

This has lead to the investigation of alternative substrates such as GaAs. The motivation to explore XY arrays in GaAs technology arises from the fact that (a) the optical absorption coefficients in GaAs are such that light is absorbed 10 times closer to the surface, than in silicon, (see Fig. 1) resulting in more efficient photocollection and tighter control over optical overload (blooming) [1] (b) the diffusion lengths in SI GaAs are over an order of magnitude shorter than in silicon, resulting in improved spatial resolution, showing promise for HDTV applications [2] (c) GaAs has superior dark current characteristics, as evidenced by the successful realisation room temperature GaAs X-ray detectors [3] and (d) there is promise of integration of high-speed processing (eg. image compression) on the same chip as the sensor. This is the reason for our focus on XY arrays rather than CCD technology.

The main drawback with GaAs, for the realisation of an XY array imager, is in the design of a low noise output circuit. This will become apparent in the analysis to be presented in this paper.

2   Noise Analysis of Imager Output Circuit

The output circuit of most standard solid-state imagers usually consists of the output node capacitance, a reset transistor and a source follower. For best noise performance, the traditional solution is to choose a source follower with an input capacitance equal to that of the output node (or video line) capacitance [4, 5, 6, 7, 8]. In practice, we have shown that this 'capacitance matching' approach results in
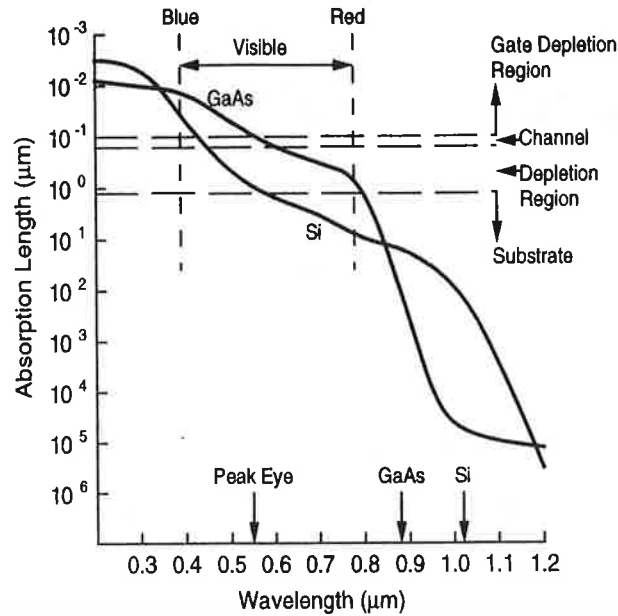
Figure 1: GaAs v. silicon absorption length comparison

an unnecessarily large estimate of transistor size [9] for silicon. We compare results between silicon and gallium arsenide, and show that capacitance matching is even less appropriate for GaAs. A noise model, for the GaAs case is fully presented.

Using the equivalent circuit, in Fig. 3, for the GaAs case, we find that the output noise is given by

$$\langle v_s^2 \rangle = \frac{kT}{C_v} + \frac{\alpha_c V_p^2 B}{2aN_dWL} \frac{1}{f} + \frac{2eI_g}{\omega^2 C_v^2} + \frac{4kTBg_o}{g_m}[(\frac{1}{2g_o} - \frac{1}{g_m}) + \frac{1}{g_m}(1 + \frac{C_{gs}}{C_v})^2] \qquad (1)$$

where Graffeuil's model [10] has been used for the flicker noise term and Pospieszalski's model [11] has been used for the thermal noise terms: $\langle v_n^2 \rangle = \frac{4kTB}{g_m}(\frac{1}{2} - \frac{g_o}{g_m})$, $\langle i_n^2 \rangle = 4kTBg_o$ and $\langle v_n^* i_n \rangle = 0$. For a first order analysis the shot noise, due to gate leakage, is modelled by one source [12]. Although the kTC noise is strictly a sequence of random dc voltage samples [13], we add it in quadrature in the usual way.

3   Discussion and Conclusion.

In practice, flicker and kTC noise are removed by correlated double sampling (CDS) [14] or delayed double sampling (DDS) [15], for example, and thus we concentrate on the thermal and shot noise curves.

We see from Fig. 4, that shot noise dominates the noise of the GaAs output circuit. Unfortunately it is impossible to remove shot noise by correlated double sampling. This means that the circuit cannot be optimised for this MESFET technology. Hence to realise a proof-of-concept imager, in the short term, two options are available: (a) use off-chip output circuitry or (b) use ammonium sulphide, $(NH_4)_2S$, annealed MESFETs — which is is reported as reducing gate leakage currents by 3 orders of magnitude [16].

Option (a) would add 1-2 pF of parasitic capacitance to the output node, but this total capacitance would still be less than in the case of silicon. With option (b) there is a question over the stability of sulphide treatments in GaAs. In the short term, (a) provides the simplest solution for producing a proof-of-concept demonstrator.

In the longer term, two emerging GaAs technologies are promising: the HIGFET and the anisotype FET. The HIGFET [17] uses a semi-insulating AlGaAs layer in the gate to reduce leakage currents — the middle shot noise curve in Fig. 4 represents this case. The anisotype FET [18] uses a graded semiconductor
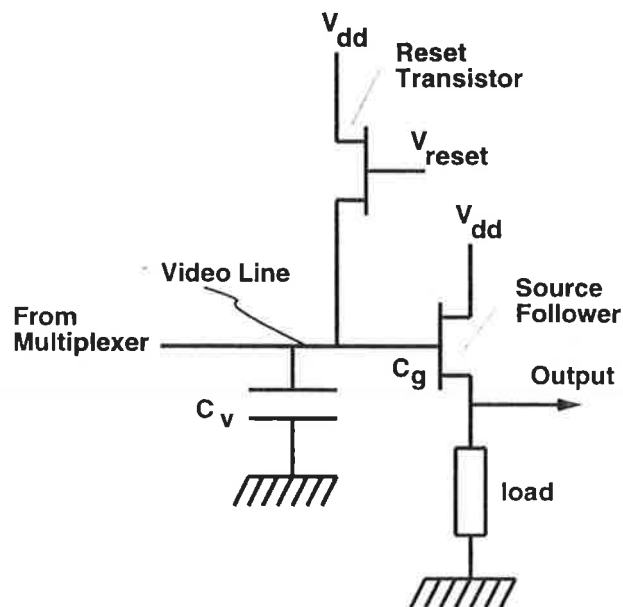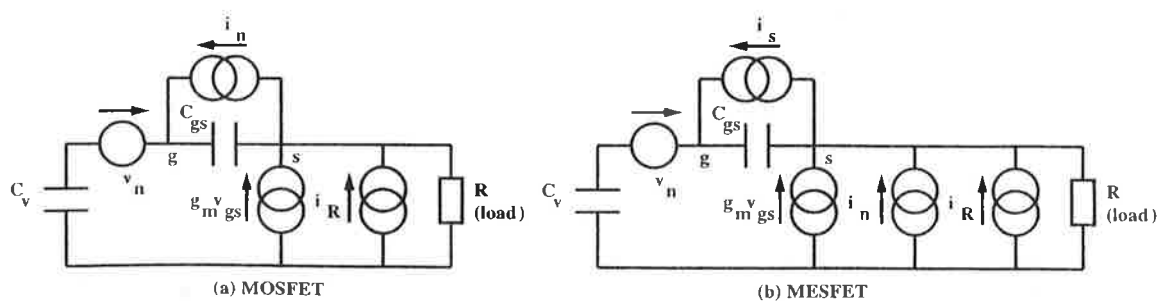
Figure 2: Imager output circuit configuration.

Figure 3: Equivalent circuit of the output stage. (a) *Si MOSFET case:* The voltage v_n and current i_n noise sources are referred to the input. (b) *GaAs MESFET case:* The voltage noise source v_n is referred to the input and the thermal current noise source i_n is at the output, in accordance with Pospieszalski's model. The shot noise due to gate-channel leakage is modelled, to first-order, by the single current source, i_s. In both cases R_{gs} has been ignored, as it is assumed that $\omega R_{gs} C_{gs} \ll 1$.
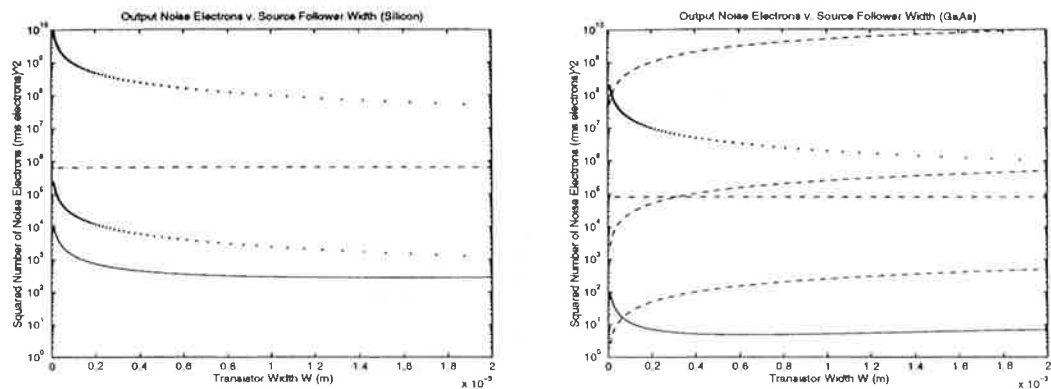
Figure 4: Imager output circuit noise sources. (a) *Silicon*. Solid line: thermal noise. Chained line: kTC noise. Dotted lines: maximum & minimum flicker noise (frequency dependent). (b) *GaAs*. Solid line: thermal noise. Chained line: kTC noise. Dotted line: maximum flicker noise. Dashed lines: shot noise (upper curve, MESFET, $I_g = 2 \times 10^{-8}$A/m; middle curve, HIGFET, $I_g = 10^{-12}$A/m; lower curve, anisotype FET, $I_g = 2 \times 10^{-15}$A/m.)

InGaAs/GaAs layer in the gate, producing yet a further improvement in gate leakage — the shot noise for this case is the lowest dashed curve in Fig. 4.

Recently Lucent have announced a true MOS-GaAs [19], using a mixture of gallium oxide and gadolinium oxide $Ga_2O_3(Gd_2O_3)$. If oxide stability and high integration levels are eventually proven, this will be the ideal medium for the proposed sensor.

4   Acknowledgement

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