3D Packaging Technology for Portable Systems

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This paper reviews the state-of-the-art in VLSI 3D packaging technology with a view to compact portable electronic systems. A number of bare dice and MCM stacking technologies are now emerging to meet the ever increasing demands for low power consumption, low weight and compact portable systems. Technical issues such as silicon efficiency, complexity, thermal management, interconnection capacity, speed and power are shown to be critical in the choice of 3D stacking technology, depending on the target application.

1 Introduction

As the complexity of portable electronic systems increases, such as in the shift from the mobile phone towards the Interactive Mobile Multimedia Personal Communicator (IM^3PC) paradigm, greater demands are being placed on the production of low power, low weight and compact packaging technologies for VLSI integrated circuits. Likewise many aerospace and military applications are following this trend. In order to meet this demand, many new 3D packaging technologies are now emerging where either bare dice or MCMs are stacked along the z-axis, resulting in dramatic improvement in compactness. As this z-plane technology results in a much lower overall interconnection length, parasitic capacitance and thereby system power consumption can be reduced by as much as 30% [1].

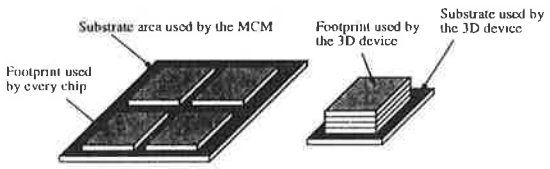

Figure 1: A graphical illustration of the silicon efficiency between MCMs and 3D technology.

2 The 3D Paradigm

Fig. 1 clearly demonstrates the appeal of stacking technology, showing how several chips can use a small substrate 'footprint' area. The ratio of the total chip area to the footprint area is called the *silicon efficiency*. Consequently, the bar chart in Fig. 2 illustrates the fact that the 3D stacking paradigm breaks the 100% barrier for silicon efficiency. A further advantage of the 3D approach is that interconnect lengths can be greatly reduced, leading to reduced propagation delays and reduced CV^2f power consumption. Fig. 3 illustrates, for example, a possible factor of 20 reduction in interconnect length by utilising the 3D paradigm.

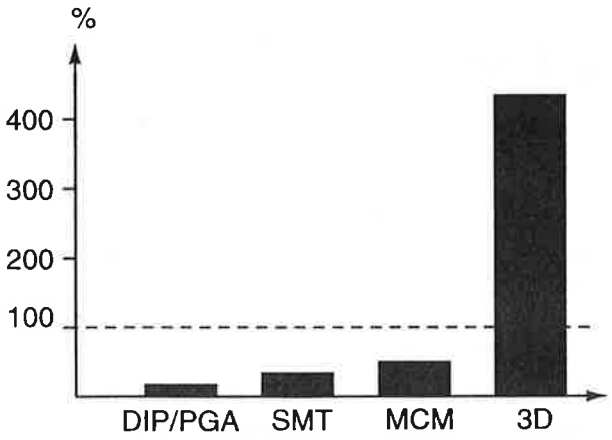

Figure 2: Silicon efficiency comparison between 3D packaging technology and other conventional packaging technologies [2].

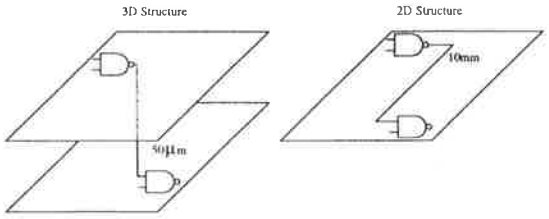

Figure 3: A comparison between the wiring lengths in 2D and 3D structures [3].

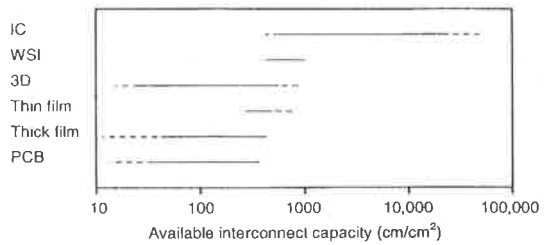

Figure 4: Available interconnect capacity for different technologies (cm/cm^2) [4, 5].

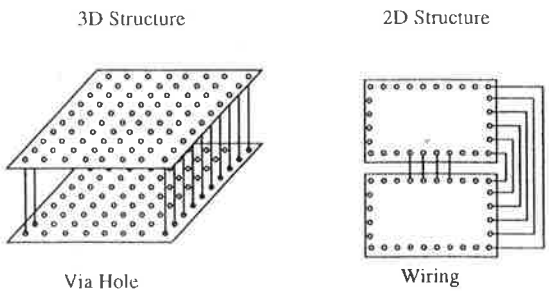

Figure 5: A comparison between 3D and 2D structures in terms of the possible number of interconnections assuming one routing layer for the 2D structure [3].

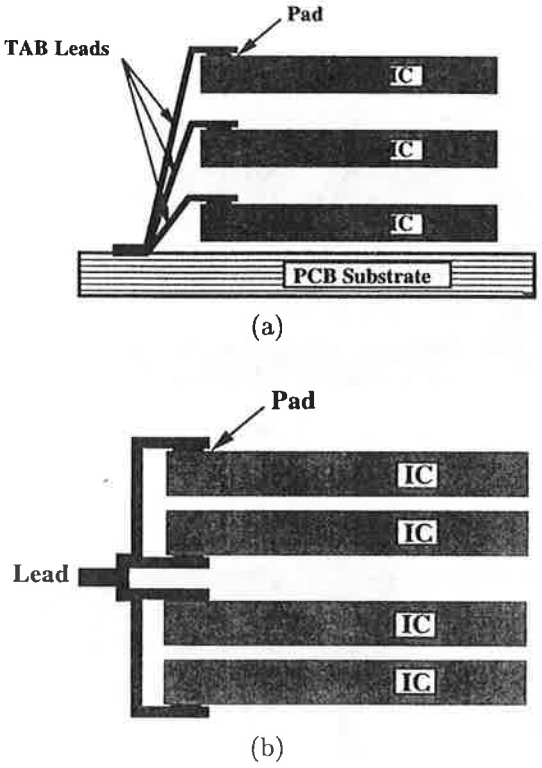

Figure 6: Two variants of the stacked tape carrier vertical interconnect. (a) Stacked TAB on PCB. (b) Stacked TAB on Leadframe.

The available interconnect length per unit area of each layer is referred to as the *interconnect capacity* (or connectivity) and is illustrated for different technologies in Fig. 4. Moreover, Fig. 5 illustrates the greater degree of freedom in forming interconnects in a 3D structure.

3 Stacking Techniques

There are many ways to stack devices. Packaged devices, PCBs, MCMs, wafer scale devices etc. can all be stacked. This can done by a number of proprietry processing techniques (at some expense!) or more cheaply by purchasing specialised connector systems (at the expense of increased volume). Perhaps the most popular approach, when using mounted die, is MCM stacking by use of 'fuzz button' connectors. Fuzz buttons are like small mounds of steel floss that make a surprisingly good connection and can be repeatedly used.

However the above stacking methods are still rather bulky for portable systems such as mobile handsets, and we shall concentrate now on bare die stacking. Bare die stacking can be split into two main categories: *loaf* stacking and *pancake* stacking. Loaf stacking is the best approach for an *area* connection to an array of points across the surface of a chip. In this case, several chips are stacked horizontally (with the appearance of a loaf of sliced bread - hence the term 'loaf') and then the top set of edges is connected to the whole *area* of another chip laid horizontally across the top of the loaf. This exercise is extremely expensive and has only been used, to date, for very high performance military imaging systems. Hence, we shall focuss on *peripheral* connections to a vertical *pancake* stack of bare die.

The main *peripheral* bare die stacking techniques are illustrated in Figs. 6 and 7. In Fig. 6 two variants of the tape carrier method are illustrated. In Fig. 7, three variants of soldered edge conductors are shown. Fig. 8 shows a bare die 'cube' with metallisation directly deposited on the cube faces – tracks can then be defined by direct laser writing. Figs. 9 and 10 show two schemes for stacking bare die of differing size the disadvantage is that the stack height is fairly limited.

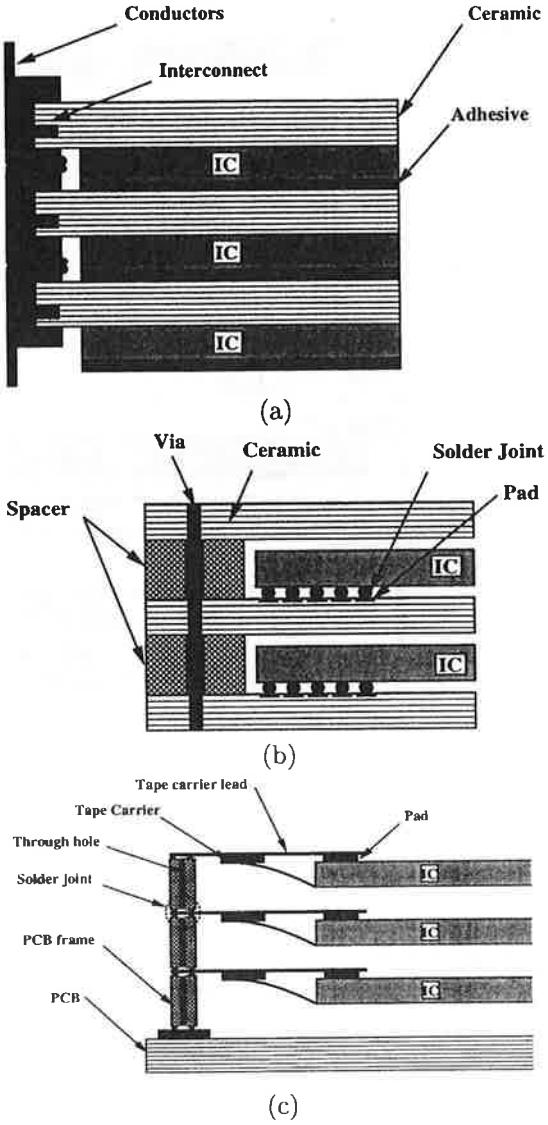

Figure 7: Three variants of the solder edge conductors vertical interconnections. (a) Solder edge contacts. (b) Solder filled via. (c) Stacked PCB leadframes.

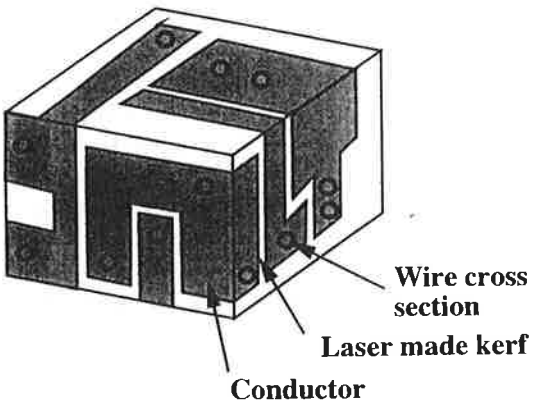

Figure 8: Direct laser writing process for vertical interconnections.

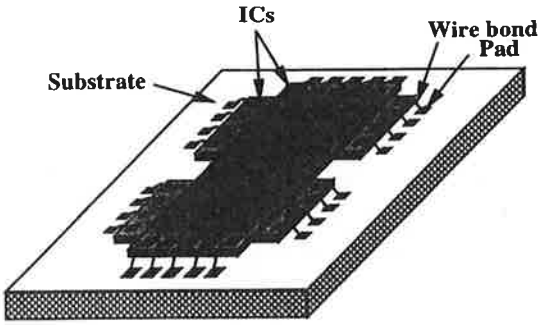

Figure 9: A vertical interconnection approach using wire bonding techniques.

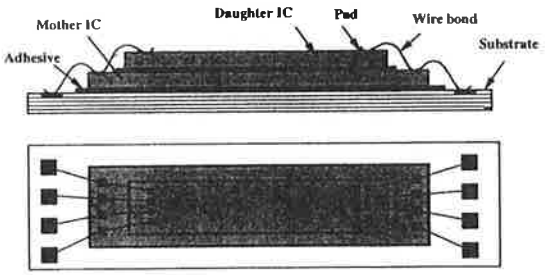

Figure 10: (upper) A schematic diagram of two chips stacked and interconnected using wire bonding. (lower) A top view of the upper schematic diagram.

Bare die 3D techniques are fairly complex, expensive and require matched die sizes for large stacks. On the other hand, stacked ceramic MCMs tend to be bulky, for portable systems. Perhaps the best compromise beteween the two approaches is a technique that mounts the bare die on thin 200 μm MCM 'flex' boards, which are then stacked and potted in epoxy. This results in an extremely compact and light stack (compared to ceramic MCMs) and allows the use of chips of differing die size.

4 Discussion and Conclusion

Significant savings in power consumption, weight and physical volume can be achieved by adopting the 3D packaging approach. A number of emergent bare dice and MCM stacking approaches have been reviewed. The choice of 3D technology depends largely on the application. For stacking memory ICs, where the power dissipation is low and all the ICs are of matched size, 'pancake' bare die stacking produces the most efficient results.

For the special case of *area* rather than *peripheral* connections (ie. a regular array connected to a processor on a pixel-by-pixel basis), 'loaf' rather than 'pancake' bare dice stacking is preferrable. The reason for this is that loaf stacking avoids the need for through-substrate-vias and hence saves silicon space and cost.

Bare dice stacking techniques that require little or no silicon post processing and have the fewest number of fabrication process steps are the most attractive. The number of steps required for bare die stacking varies dramatically from vendor to vendor from the order of 5 to 50 steps!

In summary, bare dice technology is most suitable when dealing with repetitive stacking of identical ICs. When dealing with a range of ICs of different sizes, the MCM stacking approach tends to be the most efficient in terms of cost and complexity. The most efficient, in terms of physical volume, appears to be the technique where thin MCM flex boards are stacked and then potted in epoxy. This technique also is advantageous for large volume production, where reel-to-reel flexboard can be utilised, many units can be potted in parallel and the resulting strip can then be sliced up. In cases where military/aerospace standards disallow organic materials (such as epoxy), particular attention for robustness and heat-sinking

is required, then the various ceramic MCM stacking techniques can be employed. In this case the fuzz button approach appears to be the most widely used, due to its ability for high density vertical interconnect (about a factor of 3 better the surface mount connectors).

Finally, 3D stacking techniques place upon the system designer more demands in terms of thermal and crosstalk modelling – also design for testability and a carefully structured test procedure are crucial. Vendors that thoroughly address simulation and test issues, and that focus on reducing the number of fabrication steps of their stacking technology will meet the demands of the system designer.

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