

Application of Neuron MOS in Analog Design

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This paper demonstrates the design of a Schmitt trigger circuit and two controlled gain amplifiers using a neuron MOS transistor and based on key design parameters identified in this paper. Simulation results indicate the feasibility of using neuron MOS in designing analog circuits that have characteristics independent of process parameters.

1 What is a Neuron MOS Transistor?

The neuron MOS transistor (ν MOS), recently discovered by Shibata and Ohmi [1] in 1991, simply uses capacitively coupled inputs onto a floating gate. The resulting output is simply a weighted sum of the inputs, due to the capacitive input network, followed by a thresholding operation. The behaviour of the transistor resembles, very well, that of a biological neuron where the turn-on of the transistor is paralleled by the firing of a neuron. In this respect, the device is called a neuron MOSFET or a neu-MOS (ν MOS) for short. The structure, the symbol and the capacitance representation of the ν MOS transistor are shown in Figures 1.a-c. ν MOS circuits operate with mixed mode analog/digital functions and can even perform Boolean logical operations that are dynamically reconfigurable. The use of ν MOS circuits will greatly increase functionality/area [2] while still maintaining low cost via the use of standard CMOS fabrication. In addition to neural networks the application areas where ν MOS will have use are motion detectors [3, 4, 5], monolithic imaging/compression, spatial light modulators (SLMs) and optical neural arrays [6].

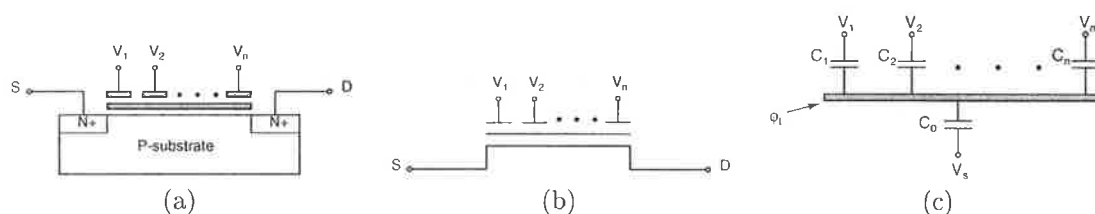


Figure 1: (a) The basic structure of an n- ν MOS transistor, (b) its electronic symbol. (c) Capacitance representation of the ν MOS, where C_0 is the sum of all the parasitic capacitances from the floating gate to the substrate including the floating gate to source.

In the literature, most ν MOS circuits have employed digital inputs [7], however a few groups have explored analog ν MOS techniques [8]. In this paper new analog circuits built using ν MOS transistor are discussed. Section 2 will discuss briefly the key design parameters for the ν MOS transistor. Section 3 will discuss a new design for a Schmitt trigger circuit that has its hysteresis width a function of capacitor ratios. Section 4 will discuss the design of controlled gain amplifier circuits in which gain is controlled by capacitor ratio rather than depending on process parameters.

2 Key Design Parameters for ν MOS Transistor

This section will identify some of the main key design parameters that can be used in designing analog and digital circuitry using ν MOS transistor.

- **Floating-Gate Gain Factor, γ**

The first design parameter to be considered is the floating-gate gain factor, γ , which is defined as

$$\gamma = \frac{C_1 + C_2 + \dots + C_n}{C_{TOT}} = \frac{C_{TOT} - C_0}{C_{TOT}} \quad (1)$$

The product of γ and V_{DD} represents the maximum floating-gate voltage obtained when all input gates are at V_{DD} . In the above equation C_0 can vary depending on the operating condition of the transistor. However, it can be approximated by the gate oxide capacitance when the device is 'ON' and can be regarded as a constant as long as the channel is formed [9]. The value of γ can be maximised by increasing $\sum_{i=1}^n C_i$ compared to C_0 . However, this would increase the size of the circuit and it should be considered as a trade-off.

- **Threshold Voltage Seen from the Floating Gate, V_{TH}^***

The second key design parameter is V_{TH}^* , which is the threshold voltage of the transistor seen from the floating gate. V_{TH}^* represents the boundary between the 'ON' and 'OFF' states of the transistor. So, for the transistor to turn 'ON', the following condition should be satisfied

$$\frac{C_1 V_1 + C_2 V_2 + \dots + C_n V_n}{C_{TOT}} > V_{TH}^* \quad (2)$$

Equation 2 states that when the linear weighted sum of all input signals exceeds a certain threshold value V_{TH}^* , the transistor turns 'ON.' V_{TH}^* is one of the main design parameters of the ν MOS transistor.

- **Floating Gate Offset Voltage, ϕ_F**

A shift or an offset on the floating gate voltage can be a result of two separate effects. The first is due to an initial charge on the floating gate that is trapped on the floating gate during the fabrication process. The magnitude of such shift can be as large as ± 200 mV [8]. A number of methods can be used to reduce this effect. The first is to shine UV light on the transistor while all terminals are grounded. This will excite some electrons to energy states above the conduction band of the oxide layer, resulting in an increase in the oxide layer conductance, allowing the discharge of the floating gate until its potential is the same as ground [8]. The second method is to inject some charge carriers to the floating gate. *ie.* programming the floating gate using Fowler-Nordheim tunnelling effect [10]. The third method is to electronically initialise the floating gate charge by connecting the floating gate to a predefined voltage. Such method is actually used in [11, 12, 13] to initialise the floating gate potential.

The second effect that might cause shift in the floating gate potential is the gate to drain capacitance, C_{gd} , as a result of feedback from the drain to ν MOS floating gate. This capacitance will have effect when the ν MOS transistor is operating in the linear region of operation [9]. The effect of such capacitance can be reduced by using minimum size ν MOS transistor and maximising the ratio of $\sum_{i=1}^n C_i V_i$ to $C_{gd} V_{ds}$. Where V_{ds} is the drain to source voltage of the ν MOS transistor.

3 Schmitt Trigger Circuits

A Schmitt trigger circuit can be designed using a dual input ν CMOS inverter, with a positive feedback from the circuit output to one of the input terminals through a digital inverter, as shown in Figure 2.a. The inverter is needed for two reasons, firstly to provide the right polarity at the ν CMOS inverter input, secondly, to increase the gain of output signal and its driving capability. The switching points of the Schmitt trigger circuit can be calculated by finding the condition under which the ν CMOS inverter switches, which can be formulated as

$$\frac{C_{in}}{C_{TOT}} V_{in} + \frac{C_o}{C_{TOT}} V_o \geq V_{TH}^* \quad (3)$$

Where C_{in} is the input coupling capacitor, C_o is the coupling capacitor from the output of the inverter to the floating gate, C_{TOT} is the sum of C_{in} and C_o , V_o is the inverter output voltage and V_{TH}^* is threshold voltage of the inverter seen from the floating gate.

The input voltage at which the Schmitt trigger circuit output, V_o , switches from low to high, V_{LH} , can be calculated by considering the circuit initial state when the ν CMOS inverter input is grounded. The output of the ν CMOS inverter, which will be high, forcing the output of the digital inverter to go low, leading to zero voltage coupling from the output to the floating gate. So, V_{LH} can be written as

$$V_{LH} = \frac{C_{TOT}}{C_{in}} V_{TH}^* \quad (4)$$

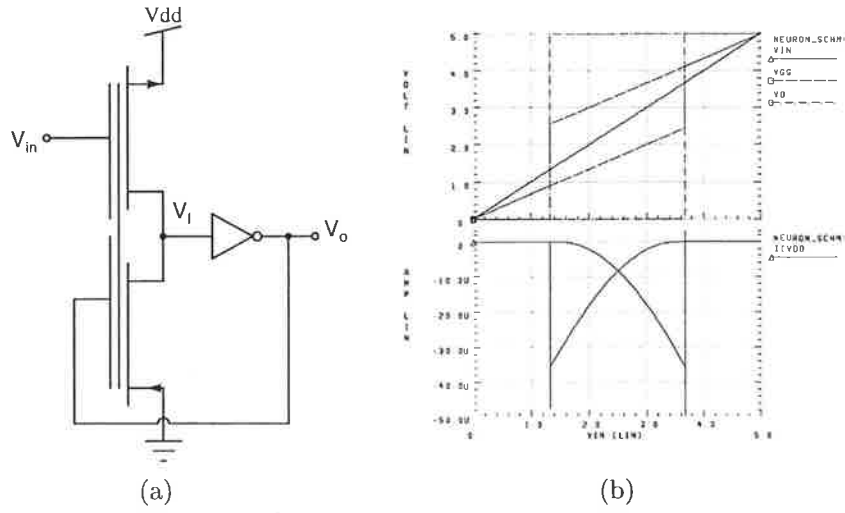


Figure 2: (a) A schematic diagram of a Schmitt trigger circuit designed using ν MOS transistor. (b) The simulation results of a Schmitt trigger shown in (a). (upper) The input-output characteristics of the Schmitt trigger circuit. Where V_{gg} is voltage at the floating gate of the ν CMOS inverter, V_o is the Schmitt trigger output and V_{in} is the input sweep. (lower) The current drawn from the supply voltage as function of the input voltage.

In a similar fashion, the input voltage at which the Schmitt trigger output switches from high to low, V_{HL} , can be calculated to be

$$V_{HL} = \frac{C_{TOT}}{C_{in}} V_{TH}^* - \frac{C_o}{C_{in}} V_{dd} \quad (5)$$

The hysteresis width of the Schmitt trigger circuit, V_{HW} , can be calculated by subtracting Equation 5 from 4 resulting in

$$V_{HW} = \frac{C_o}{C_{in}} V_{dd} \quad (6)$$

As can be seen from Equation 6, the hysteresis width is function of C_o/C_{in} and linearly dependent on V_{dd} . To make the hysteresis independent of V_{dd} , the switching point of the ν CMOS inverter and the inverter has to be independent of V_{dd} which is impractical.

The circuit shown in Figure 2.a was simulated using $C_{in} = 2$ pF and $C_o = 1$ pF. So the switching point of the Schmitt trigger according to Equations 4 and 5 should be $V_{LH} = 3.75$ V and $V_{HL} = 1.25$ V, respectively. Even though the simulation results shown in Figure 2.b were conducted using HSPICE level 13 model parameters for a $2 \mu\text{m}$ double poly, double metal n-well CMOS process, there is a very good agreement between the designed and the simulated switching points. As expected from the above first order analysis the switching point of the Schmitt trigger circuit and the hysteresis width are functions of the capacitors ratio and the supply voltage and independent of the process parameters. However, the physical implementation of such circuit should take into account possible charge injection of the switches and its effect on the Schmitt trigger circuit switching points.

4 Controlled Gain Amplifiers

This section describes the design of a controlled gain amplifier using ν MOS transistor, where the gain of the amplifier is controlled through capacitor ratio instead of transistor size ratio. The amplifier design is based on the linear grounded resistor discussed in [1]. Later in this section, another approach to the amplifier design using a 'neuron-inverter' (ν CMOS inverter) will be discussed. It will be shown that both approaches give the same results.

The first approach is to use two grounded resistors, one using n- ν MOS, while the other using p- ν MOS and connected as shown in Figure 3.a. The gain of the amplifier circuit can be found analytically by writing the current equations of the n- and p- ν MOS transistors as follows

$$I_n = \frac{\beta_n}{2} (W_{in_n} V_{in} + W_{o_n} + V_{gg} - V_{t_n})^2 \quad (7)$$

$$I_p = \frac{\beta_p}{2} (V_{dd} - W_{in_p} V_{in} - W_{o_p} V_o - V_{gg} + V_{t_p})^2 \quad (8)$$

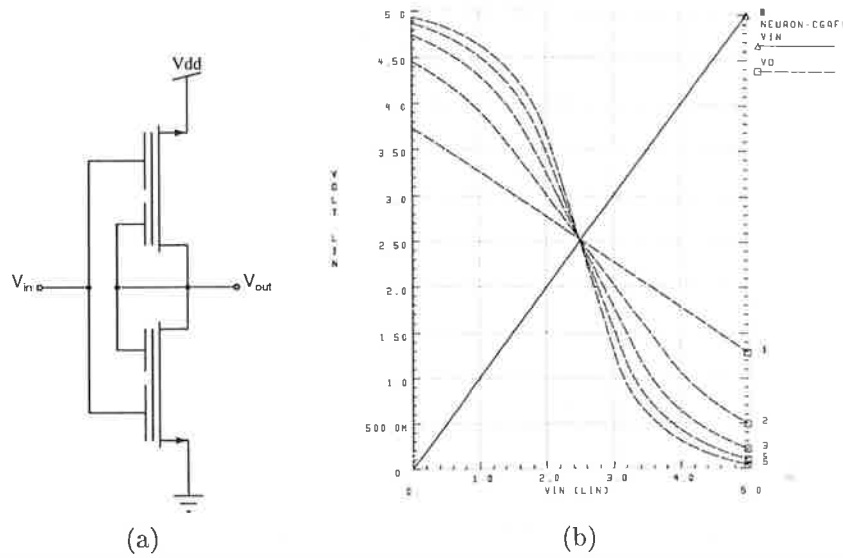


Figure 3: (a) A controlled gain amplifier circuit designed using linear grounded resistors. (b) The simulated input-output characteristics of the controlled gain amplifier shown in (a).

where

- I_n, I_p are the drain currents of the n- and p-MOS transistors, respectively ;
- β_n, β_p are the n- and p-MOS gain factors ;
- W_{in_k} is the ratio of the input coupling capacitance of transistor type k , C_{in_k} , to the total capacitances at that transistor, C_{TOT_k} . i.e $W_{in_n} = \frac{C_{in_n}}{C_{TOT_n}}$ and $W_{in_p} = \frac{C_{in_p}}{C_{TOT_p}}$;
- W_{o_k} is ratio of the output to input coupling capacitance of transistor type k , C_{o_k} , to the total capacitance at that transistor, C_{TOT_k} . i.e $W_{o_n} = \frac{C_{o_n}}{C_{TOT_n}}$ and $W_{o_p} = \frac{C_{o_p}}{C_{TOT_p}}$;
- V_o is the output voltage on the amplifier;
- V_{gg} is the initial voltage at the floating gate;
- V_{dd} is the supply voltage;
- V_{t_k} is the threshold voltages of transistor type k .

Solving Equations 7 and 8 for V_o results in

$$V_o = -\frac{\sqrt{\frac{\beta_n}{\beta_p}} W_{in_n} + W_{in_p}}{\sqrt{\frac{\beta_n}{\beta_p}} W_{o_n} + W_{o_p}} V_{in} - \frac{\sqrt{\frac{\beta_n}{\beta_p}} + 1}{\sqrt{\frac{\beta_n}{\beta_p}} W_{o_n} + W_{o_p}} V_{gg} + \frac{V_{dd} + V_{t_n} \sqrt{\frac{\beta_n}{\beta_p}} + V_{t_p}}{\sqrt{\frac{\beta_n}{\beta_p}} W_{o_n} + W_{o_p}} \quad (9)$$

Equation 9 can be simplified by setting $\beta_n = \beta_p$, $V_{t_n} = V_{t_p}$, $W_{in_n} = W_{in_p} = W_{in}/2$, $W_{o_n} = W_{o_p} = W_o/2$ and $V_{gg} = V_{dd}/2$, to

$$V_o = -\frac{C_{in}}{C_o} V_{in} \quad (10)$$

The above equation shows that the amplifier gain is purely a function of the capacitor ratio and it is independent of process parameters and the supply voltage. To confirm Equation 10, the amplifier circuit was simulated with $C_o = 10$ pF while C_{in} was swept from 5 pF to 25 pF in 5 pF steps. The simulation results are shown in Figure 3.b.

The second approach to the design of a controlled gain amplifier is to use 'νCMOS inverter,' which is simply a normal digital inverter that has N input terminals capacitively coupled to its gate. For the amplifier design a dual input 'neuron inverter' is used with one of the input terminals connected to the output of the inverter, while the other terminal is used as an input terminal, as shown in Figure 4. Once such a connection is made, the functionality of the circuit will be completely different from the 'neuron inverter,' [1] as in the case the 'neuron inverter' the output signal is a digital state of either '1' or '0.' While using this configuration the circuit will act as an amplifier.

The gain of the amplifier can be calculated by writing the current equations of the p-νMOS and n-νMOS transistors using a simple transistor model in the saturation region as follows

$$I_n = \frac{\beta_n}{2} (W_{in} V_{in} + W_o V_o + V_{gg} - V_{t_n})^2 \quad (11)$$

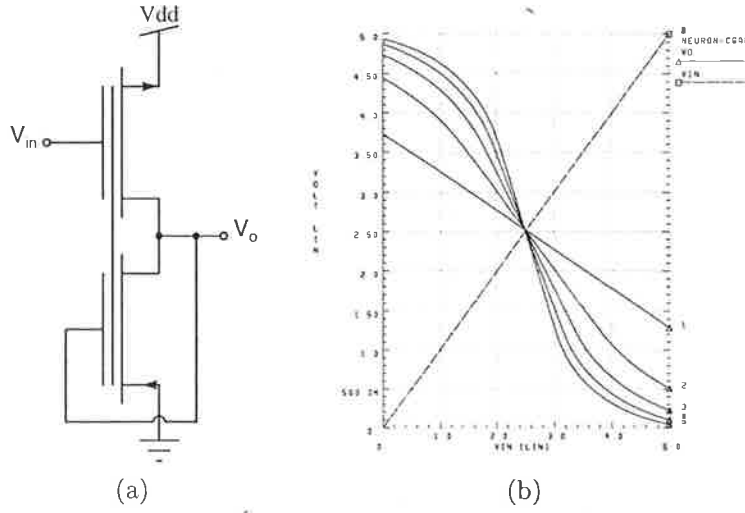


Figure 4: (a) A schematic diagram of a controlled gain amplifier using ν MOS transistor. (b) The simulation results of relationship between the output voltage, V_o , and the input voltage, V_{in} , of the controlled gain amplifier circuit with input coupling capacitor, C_{in} , swept from 10 pF to 50 pF with 10 pF increment, while C_o was fixed at 20 pF.

$$I_p = \frac{\beta_n}{2} (V_{dd} - W_{in}V_{in} - W_oV_o - V_{gg} + V_{t_p})^2 \quad (12)$$

where

W_{in} is ratio of the input coupling capacitance, C_{in} , to the total capacitance, C_{TOT} ;
 W_o is ratio of the output to input coupling capacitance, C_o , to the total capacitance, C_{TOT} ;

Solving Equations 11 and 12 for V_o gives

$$V_o = -\frac{W_{in}}{W_o}V_{in} - \frac{V_{gg}}{W_o} + \frac{V_{dd} + V_{t_n}\sqrt{\frac{\beta_n}{\beta_p}} + V_{t_p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad (13)$$

The above equation can be simplified by letting $\beta_n = \beta_p$, $V_{t_n} = V_{t_p}$ and $V_{gg} = V_{dd}/2$, resulting in

$$V_o = -\frac{C_{in}}{C_o}V_{in} \quad (14)$$

From the above first order analysis, it can be seen that the gain is also function of the ratio of C_{in}/C_o and independent of the process parameters and the supply voltage. The simulation results of the amplifier with C_{in} swept from 5 pF to 25 pF in 5 pF steps, while assuming that $\beta_n = \beta_p$ and $V_{t_n} = V_{t_p}$, are shown in Figure 4.b.

An interesting feature of the above circuits can be obtained by taking the special case when $C_{in} = C_o$, this will result in an inverting analog buffer circuit with linearity completely independent of the transistor parameters and purely function of the capacitor ratios.

5 Discussion and Conclusion

The Neuron MOS transistor has been used extensively in the design of digital circuitry, however, the use of such a transistor in analog design has not been fully investigated. In this paper a number of key design parameters for analog and digital circuits have been identified. The analog examples designed and discussed in this paper and based on these key design parameters are meant to demonstrate that the ν MOS transistor can be used to design useful analog circuitry. This was demonstrated by designing a Schmitt trigger circuit that has switching points a function of the ratio of the input coupling capacitors and the supply voltage. The circuit can be easily extended to provide a digitally programmable hysteresis width. The second demonstration was through the design of controlled gain amplifiers. These circuits have gain that is independent of the process parameters and also independent of the supply voltage. The designed circuits represent good candidates for basic building blocks in analog signal processing.

In conclusion, ν MOS transistor can be used successfully in designing useful analog building blocks and has the potential to provide low power circuitry because the input signals are capacitively coupled to the floating gates which are of small area. Moreover, as the functionality per unit area is increasing, this would enable the design of systems with complex functions with smaller silicon area compared to traditional MOS circuitry, and hence provide a step forward toward pseudo ULSI integration density.

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