Fabrication and Modeling of Ag/TiO_2/ITO Memristor

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***Abstract*— The nanometer scale feature of memristor created a broad range of opportunities for innovative architectures. The nature of the boundary conditions, the complexity of the ionic transport and tunneling mechanism, and the nanoscale feature of the memristor introduces new challenges in modeling, characterization, and measurements for Memristor-MOS (M^2) circuits. These new challenges can be addressed by a joint insight from the circuit designer and device engineers, which will dictate the needed modeling and layout rules to attain an accurate estimation of M^2 circuit performance. In this paper, memristive behavior of titanium dioxide (TiO_2) is studied using a novel combination of electrodes, silver (Ag) and indium thin oxide (ITO). Fabrication method and a modeling approach are also explained. The ITO electrode provide (a) an excellent transparency in visible light, (b) improved functional reproducibility, and (c) non-volatile characteristics as well as a promising unique application of the M^2 circuits in sensory applications. Furthermore, proposed modeling approach shows a good agreement between measurements and simulations of analog memory characteristics and reproducibility as well as long-term retention.**

I. Introduction

Since the first realization of capacitor in 1745 followed by conceptualization of resistor and inductor in 1827 and 1831 respectively, the design community has been limited to these three fundamental passive circuit elements [1], [2]. In 1971, Chua postulated that one could set up five different mathematical relations between the four fundamental circuit variables: electric current I, voltage V, electric charge q, and magnetic flux ϕ and according to the mathematical symmetry there should exist a fourth element to complete the symmetry [1]. This postulation implies that if charge $q(t)$ flows in one direction through a circuit, the resistance of the circuit approaches its OFF state (R_{OFF}) and the resistance approaches its ON state (R_{ON}), if charge flows in the opposite direction. If the flow of charge is stopped at any time by turning off the voltage source, the resistance state at the instant of disruption is retained, indicating that the circuit 'remembers' its past history.

In 2008, the Hewlett-Packard (HP) labs identified the link between the mathematical form of the Chua's memristor and Resistive-RAMs (ReRAMs). They demonstrated that the memristive behavior occurs by doping TiO_2 thin-film and creating a TiO_2/TiO_{2-x} layer sandwiched between two Platinum (Pt) nanowires [3].

Since 1971 many applications have been identified for memristors. For instance, memristive system of equations is similar to that the Hodgkin-Huxley model describes for the behavior of neural cells [1]. A preliminary experimental study has also shown that memristive state variable behavior is able to achieve spike-timing-dependent plasticity (STDP) in a form of synaptic weight update behavior [4]. Many other applications for an analog memristor can be identified such as, implementing multiple-valued logic (MVL), applications in fuzzy logic, image smoothing, edge detection, pattern recognition, and adaptive control. Digital applications of the memristor in implementing the binary logic gates and memory cells are perhaps the most industry-oriented research in this field. These applications need appropriate modeling and characterization of this device depend upon their requirements. For example, an analog application needs a detailed characterization of the memristor's state variable and its rate of change, whereas for a digital application more data is needed around ON and OFF state I-V curves and switching thresholds. Several SPICE models have provided insights into the memristor's behavior [5], [6], [7], [8], [9]. Some of the device level studies have also tried to explain underlying mechanisms observed for behavior [10], [11].

This research identified alternative metallic materials in order to pave the pathway toward a fully transparent memristive device for sensor applications and the concept of light-to-resistance (LTR) state transformation. We model the nonlinear switching behavior of a titanium dioxide (TiO_2) layer sandwiched between silver (Ag) and indium thin oxide (ITO) electrodes.

The paper is organised as follow. Section II reviews a simple demonstration of memristive system of equations. An alternative analytical model for the memristive equations is also shown in this section. In Section III fabrication and process technology is explained. This is followed by Section IV and V where measurement results and related remarks and conclusions are provided.

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II. Memristor Characterization

Strukov *et al.* [3] presented a physical model whereby the memristor is characterised by an equivalent time-dependent resistor whose value at a time t is linearly proportional to the quantity of charge q passing through it. They fabricated a proof-of-concept device, which consists of a thin layer of TiO_2 and a second oxygen deficient layer of TiO_{2-x} sandwiched between two Pt nanowires. A change in distribution of oxygen vacancies within these layers changes the resistance. When sufficient charge passes through the memristor that ions no longer move, the device enters a hysteresis region that is a fundamental characteristic of memristors and keeps q at an upper bound with fixed memristance, $M(q)$. The resistance change is non-volatile, hence, the cell acts as a memory element that remembers past history of ionic charge flow through the device. Similar scenario can be applied for our device using Ag (200 nm)/TiO_{2-x} (20 nm)/TiO_2 (2 nm)/ITO (200 nm).

A. Simplified Memristor Model

For convenience, we have an overview of a simplified memristor model. In its simplest form, the memristor is modeled in terms of the two doped and undoped regions, each having vertical width of w and lw, respectively. The current-voltage (I-V) relationship defined as memristance $M(q)$, is described by, $V(t) = (R_{\rm OFF} - x\Delta R)I(t)$, where $\Delta R = R_{\rm OFF} - R_{\rm ON}$ and $x \in (0,1)$ is the normalized version of the state variable, $w \in (w_{\rm min}, w_{\rm max})$. According to HP, the underlying mechanism is tunneling [10], [11]. Therefore, w represents tunneling barrier height that is in the range of $w \in (1.1\text{ nm}, 1.9\text{ nm})$ [10]. When $w \in (w_{\rm min}, w_{\rm ON}]$ the device's state is ON, whereas $w \in [w_{\rm OFF}, w_{\rm max})$ indicates OFF state as illustrated in Fig. 1. Here we used a normalized interpretation of such a dynamic using x as the parameter of interest. Assuming a uniform electric field across the barrier,

$$\frac{dx(t)}{dt} = \frac{V(t)}{\beta}\ , \tag{1}$$

where $\beta = L^2/\mu_{\rm ai}$ has the dimension of magnetic flux, ϕ. The parameter L is the device thickness and $\mu_{\rm ai}$ represents the average ionic drift mobility. Therefore, in a simplistic form, $x(t)$ is proportional to a ratio between the flux, $\phi(t)$, and the constant β. High nonlinearity at the boundaries can be addressed using a window function [5]. These simplistic equations represent that at least two equations are necessary to model a memristor, I-V curve, and switching dynamics.

B. Proposed Model

The electrical behavior of the memristor either as a switch or a memory cell is determined by the boundary between the two regions TiO_2/TiO_{2-x}. Here we utilize the Simmons tunneling theory, which commonly used to describes the conduction mechanism of a metal-insulator-metal (MIM) structure [12], [13]. Assuming that $dx/dt \propto g(\cdot)$, the behavior of function $g(\cdot)$ must be monotonically increasing. Furthermore, if the drift velocity of the oxygen vacancies is directly proportional

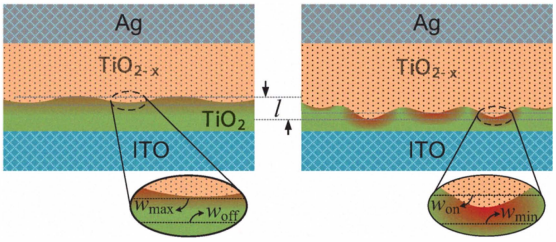

Fig. 1. Structure of fabricated Ag/TiO_{2-x}/TiO_2/ITO MIM layer. (a) shows OFF state, high resistance corresponding to $R_{\rm OFF}$, (b) illustrates ON state, high resistance corresponding to $R_{\rm ON}$. The l and w are the tunnel barrier length and the position of barrier (barrier width). There are two boundaries for w, namely $w_{\rm max}$ and $w_{\rm min}$ that show maximum and minimum positions of the tunneling barrier. In addition, $w_{\rm ON}$ and $w_{\rm OFF}$ indicate commencement of ON and OFF conditions for the bi-stable (digital) scenario.

to the applied electric field the rate of change in the device conductance, dG/dt, behaves similar to dx/dt. The model that we use shows a good agreement with the HP measurement data reported in [11], as shown in Fig. 2.

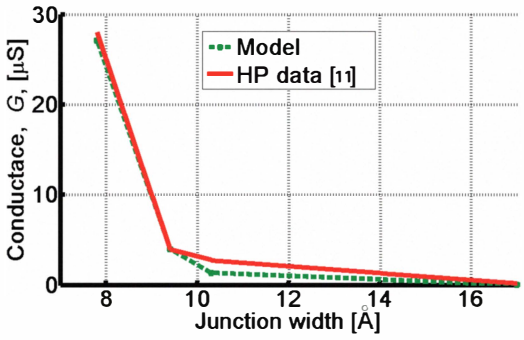

Fig. 2. Device conductance G (μmho) as a function of junction width (in Angstroms). Highly nonlinear change in conductance of the device can be observed based on Simmons theory of tunneling, which confirms the experimental results shown in [11].

The highly nonlinear relationship between the ionic drift velocity and the normalized state variable, x, is defined by:

$$\begin{cases} I(t) = x(t)I_{\rm ON} + (1 - x(t))I_{\rm OFF}\ , \\ \frac{dx}{dt} = \upsilon g(V, \rho(x), \varphi_0)\ , \end{cases}$$

where

$$g(V,\rho(x),\varphi_0) = \\ (1 - \frac{V}{2\varphi_0})\exp\Big(\rho(x)\varphi_0\Big(1 - \sqrt{1 - \frac{V}{2\varphi_0}}\Big)\Big) \\ -(1 + \frac{V}{2\varphi_0})\exp\Big(\rho(x)\varphi_0\Big(1 - \sqrt{1 + \frac{V}{2\varphi_0}}\Big)\Big)\ , \tag{2}$$

υ is a constant that identifies the ON and OFF switching speeds within the normalized distance derived from experimental results, φ_0 (in eV) is the equilibrium barrier height, and $\rho(\cdot)$ is the equilibrium shape factor in eV^{-1} and $\rho(x)$ is the new shape factor function modeled as

$$\rho(x) = \delta + \eta(1 - (2x - 1)^{2p})\ , \tag{3}$$

where $\delta(\geq 4)$ is an offset constant to retain the monotonically increasing condition, η is a constant that manages the nonlinearity (curvature) in the hysteresis loop, and hence the switching speed. Here we assumed that the ON and OFF switching (SET and RESET) speeds are similar. The window function described is in direct relationship with the drift velocity in [8]. The use of window function here has slightly different purpose. In fact, depends on the constant p ($\gg 1$) we are able to define a dimensionless and in this case a rectangular approximation of the barrier profile using this function for future works. The barrier height can be also considered as the state variable but it needs more complex model. We have also considered the hopping theory for ionic drift velocity and a $\sinh(\cdot)$ relationship between the velocity and applied electric field that needs further anaysis to be finalized.

SPICE macromodel has been implemented using [7] netlist and an approach introduced in [5] and [9]. Similar implementation using another analytical model that is introduced in [10] results in a significant nonlinearity (double exponential) and consequently the possibility of convergence error during simulations mainly due to an overflow. It worth also mentioning that another issue with the modeling is to get memristor dynamics according to the measurements with deferent completion current. In fact using the completion current would help a better understanding of the internal dynamics. Here we provide an approximation of the highly nonlinear behavior using a polynomial function in Eq. (3). According to the approach described in [5], two parts of the Eq. (2) have been implemented using two voltage controlled current sources with different directions between node x and the ground. A capacitor, C, used to carryout integration. Therefore, according to the Kirchhoff's circuit laws $\frac{dx}{dt} = \frac{i_{\text{charge}} - i_{\text{discharge}}}{C}$, where i_{charge} and $i_{\text{discharge}}$ can be found in the right hand side of Eq. (2) as two seperate equations.

III. Process Technology

Experimental devices have been fabricated on 136 nm glass substrates, percolated with ITO that has 13.7 Ω/sq sheet resistance. The ITO was patterned using chemical wet etching to define the bottom electrode. Then, the substrate was cleaned in sequential ultrasonic baths of soap, acetone, and isopropanol alcohol for 60 minutes each. Subsequently, two layers of TiO_2 were deposited on the cleaned ITO substrate.

The upper TiO_{2-x} layer was deposited by atomic layer deposition (ALD) using titanium tetraisopropoxide and O_2 as the precursor and oxygen source, respectively, having 5% oxygen removed. The lower TiO_2 formed is 2 nm thick while the upper TiO_{2-x} layer formed is 20 nm thick. Finally, 200 nm Ag layer is deposited as a top electrode that was thermally evaporated at room temperature at a pressure below 1×10^{-7} Torr. The side view of memristor together the micrograph of fabricated devices is shown in Fig. 3(a) and (b), respectively.

IV. Measurements and I-V Modeling

Application of appropriate biases shown in Fig. 4(a) changes the device resistance state from 83 kΩ to 1.5 kΩ giving a ratio of around 55. This is important to note that an initial irreversible electroforming process is required to activate switching behavior of the device under test. The nonlinearity, switching behavior, and reproducibility of a device under test are beleived to be related to the forming process. We have achieved significantly higher resistances for the both ON and OFF states and higher ratios but their functional reproducibility as well as appropriate forming process continue to be under further investigations. In this particular case, we have created an electric field around 6 MV/cm across the device to carryout the forming step.

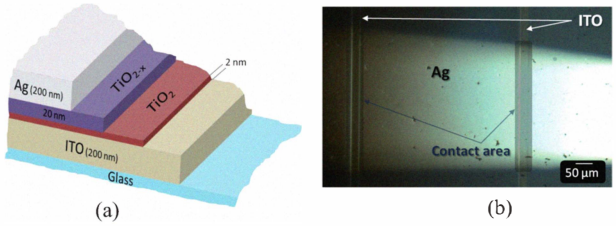

Fig. 3. Cross sectional view of a memristor device structure. (a) ITO and Ag are used as bottom electrode and top electrode, respectively, overlaid on glass substrate. (b) The fabricated memristor micrograph. Only two devices with different contact sizes are shown here. Device contact sizes vary from 32×32 μm^2 to 100×500 μm^2.

TABLE I

Parameters and Related Values

Parameter	Value	Parameter	Value
V^*	-2 V to 2 V	a	$1.2e-2$
x	Normalized state variable	b	$4.3e-6$
φ_0	1.2 eV [11]	c_1	$3.3e-4$
δ	6	c_2	$4.8e-4$
η_{ON}	22	d_1	2.1
η_{OFF}	28	d_2	1.6
p	5	v	$4.0e-3$

* We use a triangular voltage similar to the actual applied voltage across the device during the measurements. In several experiments we have set the completion current to 10 mA, however, in this particular case no completion current has been set.

The analog properties of the device are measured at 100 mV incremental steps as part of either presetting or pre-resetting the state. Fig. 4(b) illustrates several programming steps that were taken above 500 mV with 100 mV increments. The device is programmed at its low resistance state. Using this technique, the analog values can be stored in the memristor as an internal state. The incremental rate is around 10%. The positive sweeps (0 to 200 mV) do not contribute to any noticeable change in the device resistance state. Data were collected with a Keithley 4200-SCS semiconductor parameter analyzer. Both of the main graphs in Fig. 4, confirm the application of the Ag/TiO_2/ITO memristor in digital and analog applications. The state variable equation confirms the experimental data in Fig. 4(b). Preliminary results of this structure as a synaptic connection and a full consideration of a memristor-based spike-timing-dependent plasticity (mSTDP)

are left to future work. It worth mentining that analog and digital behaviors of a memristor device can be controlled with a careful control on the applied voltage (electric field).

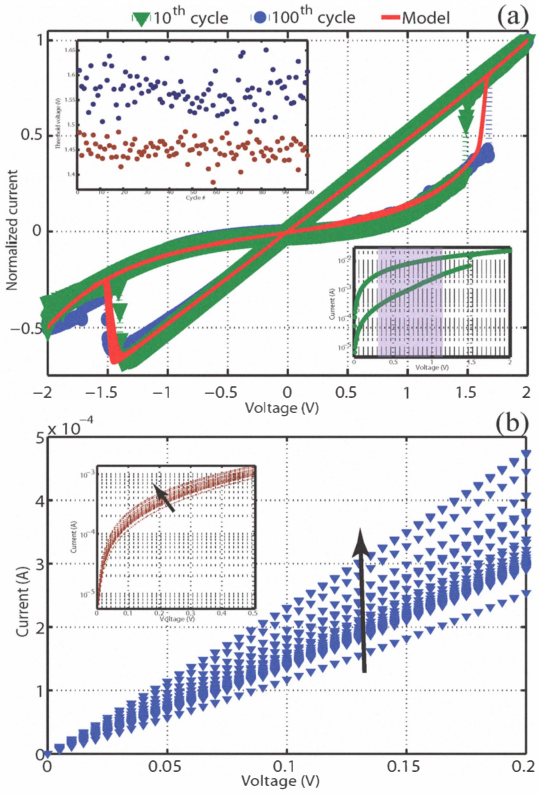

Fig. 4. Ag/TiO_2/ITO memristor characteristics. (a) current-voltage hysteresis loop. The green and the blue lines illustrate measured I-V curves at 10^{th} and 100^{th} switching cycles, respectively, using Keithley 4200-SCS Semiconductor Characterization System. The narrow red curves in (a) shows the model using our model highlighting good agreement. The top-left corner inset illustrates variation of switching threshold for SET (blue) and RESET (red, absolute value) processes for 100 cycles analysis. The bottom-right cornet inset demonstrates log scale I-linear V and the highlighted region approximately identifies safe region for READ operation (linear line and no switching). After 100 cycles of switching, a standard deviation of 26 mV in threshold voltage was observed. (b) analog memory property. The arrow in (b) shows that the evaluations commences with a low state to high state. Analog memory property of the fabricated memristor confirms implementation of a multistable states device which is able to retain its internal state for long term after disconnecting power supply. Each curve was measured two times, just before disconnecting the power supply and after connection. Inset demonstrates applied voltage up to 500 mV and log scale current.

The model for I-V curve is given by:

$$I = x^n(aV + b) + (1-x)^n(c_1 \exp(d_1 V) - c_2 \exp(d_2 V)) \ , \quad (4)$$

where a, b, c_1, c_2, d_1, and d_2 are parameters related to the device structure, materials, and dimensions. Here we fit appropriate values for these parameters for the ON and OFF currents. The parameter n defines the nonlinearity between x and I. This parameter is defined to address the non-uniformity of the step changes in Fig. 4(b). For sake of simplicity, it is assumed that $n = 1$. the The SPICE macromodel parameters are provided in Table I. The approach is consistent with the measurement results as illustrated in Fig. 4. In general, the presented form of $I = x^n I_{\text{ON}} + (1-x)^n I_{\text{OFF}}$ can be used as a general form to describe the I-V relationship of memristive devices.

V. Conclusion

In this paper, we have shown an alternative fabrication and modeling approach for the memristor to pave the pathway toward a fully transparent memristive device for direct application in sensors and detectors (e.g. ultraviolet photosensors). The modeling approach can be used in several aspects of memristive-based analog/digital circuit design. The accuracy of the model was confirmed using a SPICE macromodel implementation and experimental results. The fabricated MIM structure is based on Ag/TiO_{2-x}/TiO_2/ITO nano layers and it has shown promising results in terms of functional reproducibility and high speed switching for digital and low-voltage analog application.

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