Novel VLSI Implementation for Triplet-based Spike-Timing Dependent Plasticity

Mostafa Rahimi Azghadi, Omid Kavehei, Said Al-Sarawi, Nicolangelo Iannella, and Derek Abbott

Centre for Biomedical Engineering, School of Electrical and Electronic Engineering,
The University of Adelaide, Adelaide, SA 5005, Australia
{mostafa,omid,alsarawi,iannella,dabbott}@eleceng.adelaide.edu.au

***Abstract*—Spike Timing-Dependent Plasticity (STDP) is one of several plasticity rules that is believed to play an important role in learning and memory in the brain. In conventional pair-based STDP learning, synaptic weights are altered by utilizing the temporal difference between pairs of pre- and post-synaptic spikes. This learning rule, however, fails to reproduce reported experimental measurements when using stimuli either by patterns consisting of triplet or quadruplet of spikes or increasing the repetition frequency of pairs of spikes. Significantly, a previously described spike triplet-based STDP rule succeeds in reproducing all of these experimental observations. In this paper, we present a new spike triplet-based VLSI implementation, that is based on a previous pair-based STDP circuit [1]. This implementation can reproduce similar results to those observed in various physiological STDP experiments, in contrast to traditional pair-based VLSI implementation. Simulation results using standard 0.35 μm CMOS process of the new circuit are presented and compared to published experimental data [2].**

I. Introduction

Spike Timing-Dependent Plasticity (STDP) is an unsupervised synaptic plasticity rule that induces changes in individual synaptic weights, based on the timing difference between pre- and post-synaptic spikes [2], [3]. The classical STDP model employs a pair of spikes (pre-post or post-pre) as the trigger for changes in synaptic plasticity [3]. However, if the repetition frequency of spike pairs is increased, this model fails to correctly reproduce synaptic weight changes as observed in physiological experiments [4]. Furthermore, it is not able to account for experiments using triplet or quadruplet of spikes [5]. An explanation for these shortcomings is that traditional pair-based STDP does not account for known nonlinear interactions between successive spikes when more complex spike patterns are used [6]. In order to resolve the short-comings of the classical pair-based model, a simple yet elegant STDP model was proposed [2] where synaptic weight change using triplets of spikes was developed.

Research focusing on translating computational models into neuromorphic devices including VLSI implementations of both spiking neurons and synaptic plasticity, in particular STDP, has increased in popularity over the last decade. When considering a VLSI implementation of STDP, several issues need to be addressed such as power consumption, circuit area, noise, output dynamic range, etc. Currently there are several VLSI implementations of pair-based STDP [7]–[9], where the circuit proposed by Indivieri *et al.* stands out as an exemplar [1]. Here, we model the STDP circuit using three different types of inputs namely: (i) spike triplets, (ii) spike quadruplets and (iii) spike pairs with increased repetition frequency between pairs. Our simulation results show that the circuit in [1] can reproduce pair-based learning window, however, this circuit is unable to reproduce the frequency effects akin to those seen in electrophysiological experiments when varying the repetition frequency of spike pairs, nor it is able to mimic the outcomes of triplet and/or quadruplet based spike protocols. In this paper, (i) we propose a new VLSI circuit, which builds on Indiveri's STDP circuit, that implements the spike triplet-based STDP rule [2], and (ii) we demonstrate how the new circuit can mimic the physiological experiments reported in [2].

The rest of the paper is organized as follows; Section II provides a brief review of pair-based and triplet-based STDP models. Experimental results for the new triplet-based STDP circuit as well as Indiveri's pair-based circuit are presented and discussed in section III followed by a conclusion.

II. STDP Synaptic Modification Rules

A. Classical pair-based STDP

In classical pair-based STDP, potentiation occurs when a presynaptic spike precedes a postsynaptic spike; otherwise depression occurs, where weight changes can be governed by a temporal learning window. The classical STDP temporal learning window can be expressed as [10]

$$\Delta w = \begin{cases} \Delta w^+ = A^+ e^{\left(\frac{-\Delta t}{\tau_+}\right)} & \text{if } \Delta t \geq 0 \\ \Delta w^- = -A^- e^{\left(\frac{\Delta t}{\tau_-}\right)} & \text{if } \Delta t < 0 \ , \end{cases} \tag{1}$$

where $\Delta t = t_{\rm post} - t_{\rm pre}$ is the time difference between a single pair of post- and pre-synaptic spikes, τ_+ and τ_- are time constants of the learning window, and finally A^+ and A^- represent the maximal weight changes for potentiation and depression, respectively.

B. Triplet-based STDP

Previous studies illustrated that classical pair-based STDP fails to reproduce the experimental outcomes involving higher order spike patterns such as triplets and quadruplets of spikes [5], [6] and, furthermore, fails to account for the observed dependence on repetition frequency of pairs of spikes [4]. To resolve these issues, pair-based STDP was

extended to include spike triplets resulted a spike-triplet-based STDP learning rule which could sufficiently reproduce previously reported physiological experiments [2]. Based on the triplet synaptic learning rule presented in [2], the triplet synaptic modification rule can be written as

$$\Delta w(t) = \begin{cases} \Delta w^+ = e^{\left(\frac{-\Delta t_1}{\tau_+}\right)}\left(A_2^+ + A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)}\right) \\ \Delta w^- = -e^{\left(\frac{\Delta t_1}{\tau_-}\right)}\left(A_2^- + A_3^- e^{\left(\frac{-\Delta t_3}{\tau_x}\right)}\right), \end{cases} \quad (2)$$

where $\Delta w = \Delta w^+$ if $t = t_{\text{post}}$ and $\Delta w = \Delta w^-$ if $t = t_{\text{pre}}$. A_2^+, A_2^-, A_3^+ and A_3^- are constants, $\Delta t_1 = t_{\text{post}} - t_{\text{pre}}$, $\Delta t_2 = t_{\text{post}(n)} - t_{\text{post}(n-1)} - \epsilon$ and $\Delta t_3 = t_{\text{pre}(n)} - t_{\text{pre}(n-1)} - \epsilon$, are time difference between combinations of pre- and post-synaptic spikes, τ_-, τ_+, τ_x and τ_y are time constants, and finally ϵ is a small positive value which selects the contribution to the weight change just before the final spike of the presented triplet [2]. Hence, triplet-based model induces weight change in proportion to eight parameters (in comparison to four parameters for classical pair-based model); four potentiation parameters (A_2^+, τ_+, A_3^+, and τ_y) and four depression parameters (A_2^-, τ_-, A_3^-, and τ_x).

III. STDP VLSI Implementation

A. VLSI Circuit for Pair-based STDP

There are several VLSI implementations of pair-based STDP in the literature [1], [7]–[9]. The implementation by Indiveri *et al.* [1] was adopted, due to its low power and small area. Fig. 1(a) depicts the Indiveri's pair-based STDP circuit schematic and Fig. 1(b) demonstrates its resulting temporal learning window for various τ_+ and τ_- (V_{tp}, V_{td}). The timing of pre- and post-synaptic spikes are used to induce weight changes across C_w. This circuit results in a learning window which captures the essential features of STDP, where there are two distinct regions, one for potentiation where $\Delta t \geq 0$ and depression for $\Delta t < 0$. When a pre-synaptic pulse, V_{pre}, or a post-synaptic pulse ($\overline{V}_{\text{post}}$) occurs, V_{pot}(V_{dep}) will be set to zero (V_{dd}). Note that V_{pot} (V_{dep}) then changes linearly over time to reach V_{dd} (zero), and represents the required time constants τ_+ (τ_-). These time constants can be set by changing the gate voltage of the corresponding transistor, i.e. V_{tp} (V_{td}). Fig. 1(b) demonstrates the variation of the learning window for different values of V_{tp} (V_{td}), i.e. τ_+ (τ_-). So, if a V_{pre} ($\overline{V}_{\text{post}}$) pulse occurs during time determined by its corresponding time constant, τ_- (τ_+), the output capacitor will be discharged (charged) by a current that is proportional to the value of V_{dep} (V_{pot}) and V_{A^-} (V_{A^+}). For further details, the reader is referred to [1].

B. VLSI Circuit for Triplet-based STDP

Unlike the pair-based model, in the triplet model, a pre-synaptic (post-synaptic) spike further to having an affect on its successive post-synaptic (pre-synaptic) spike can also have an affect on its consecutive pre-synaptic (post-synaptic) spike(s). In the proposed triplet circuit two more pulses, $V_{\text{post}(n-1)}$ and $\overline{V}_{\text{pre}(n-1)}$, are used in addition to $\overline{V}_{\text{post}(n)}$ and $V_{\text{pre}(n)}$,

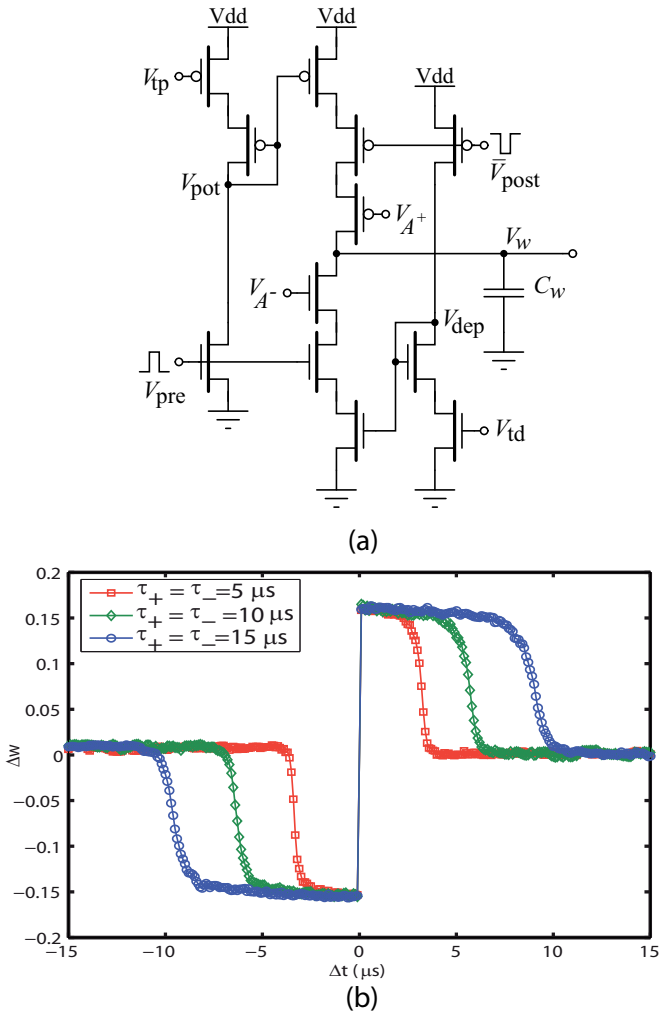

Fig. 1. VLSI implementation of classical pair-based STDP. (a) Schematic circuit diagram of Indiveri *et al.* circuit [1]. (b) The learning window of the circuit based on our simulations.

as shown in Fig. 2. These extra pulses result in the required nonlinearity in the triplet-based model [2]. The circuit works as follows: upon the arrival of a post-synaptic pulse, $\overline{V}_{\text{post}(n)}$, the M5, M10 and M18 transistor switches turn on. Then M10 sets a depotentiating voltage V_{dep1} to V_{dd}. This voltage then starts decaying linearly in time which can result in depression, if a pre-synaptic pulse, $V_{\text{pre}(n)}$ arrives during the time V_{dep1} is decaying to zero (τ_- time constant). In this situation, C_w will be discharged through M7-9 by a current that is limited by the M7 bias voltage ($V_{\text{A}_2^-}$). In contrast to M10, which can result in depression after receiving a post-synaptic pulse, M5 and M18 can lead to two different potentiations. The first one can occur if M5 turns on during time constant of V_{pot1} (τ_+). This potentiation will be through M4-6 and is proportional to the bias voltage at M6 ($V_{\text{A}_2^+}$). The second potentiation term can charge C_w through M16-19 and is proportional to $V_{\text{A}_3^+}$ if M18 is on at the required time, i.e. when V_{pot1} and V_{pot2} have still kept M16 and M17 on. This is the term that distinguishes triplet from pair-based STDP, as there is no such

term in pair-based STDP. Similarly, upon the arrival of a pre-synaptic pulse, $V_{\mathrm{pre}(n)}$, a potentiating voltage V_{pot} is set to zero and starts increasing linearly in time which can result in potentiation when a $\overline{V}_{\mathrm{post}(n)}$ pulse arrives within the τ_+ time constant. In addition, two possible depressions proportional to A_2^- and A_3^- can take place, if this pre-synaptic pulse is in the interval area of effect of V_{dep1} and V_{dep2}, i.e. in τ_- and τ_x time constants. It is worth mentioning that the required time constants in the proposed circuit, τ_-, τ_+, τ_x and τ_y, can be easily adjusted by altering their corresponding bias voltages, V_{td1}, V_{tp1}, V_{td2} and V_{tp2}.

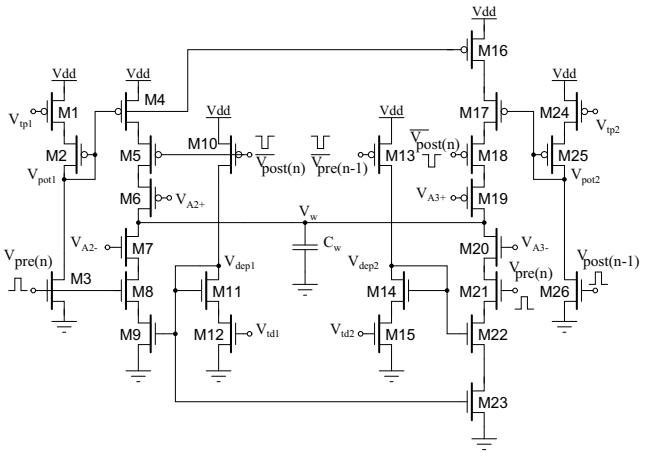

Fig. 2. Proposed VLSI implementation of triplet-based STDP.

C. Experimental protocols and data fitting method

In order to compare pair-based and triplet-based VLSI implementations to experimental data, the same experimental protocols and experimental data sets that were used in [2] are also adopted in the present study. One of the data sets originates from experiments on the visual cortex [4] that investigated how altering the repetition frequency of spike pairings affects the overall synaptic weight change. The other experimental data set that was utilized originates from hippocampal cultures experiments from [5] which examined pairing, triplet and quadruplet protocols effects on synaptic weight change. This data and a full description of the *pairing*, *triplet* and *quadruplet* experimental protocols are fully described in [2]. It should be noted that, during all experiments presented in this paper, the nearest spike interaction as described in [2] is employed.

D. Applied protocols and data fitting method

In order to fit the required parameters in both pair-based (A^+, τ_+, A^- and τ_-) and triplet-based circuit (τ_+, τ_-, A_2^+, A_2^-, τ_x, τ_y, A_3^+ and A_3^-), for a given set of parameters, the mentioned circuits with a given pairing, triplet, or quadruplet protocol were simulated. The voltage across C_w is recorded and the total weight change is divided by the maximum possible weight change, $\Delta V_w/V_{\mathrm{dd}} = \Delta w_{\mathrm{cir}}$. These results are then compared to the weight changes given in the experimental data Δw_{exp} obtained from Sjöström *et al.* and Wang *et al.* reported in [2]. The model parameters are optimized by minimizing of the normalized mean-square error (NMSE) defined by Eq. 3, as used in [2],

$$E = \frac{1}{p}\sum_{i=1}^{p}\left(\frac{\Delta w_{\mathrm{exp}}^i - \Delta w_{\mathrm{cir}}^i}{\sigma_i}\right)^2, \tag{3}$$

where $\Delta w_{\mathrm{exp}}^i$, $\Delta w_{\mathrm{cir}}^i$ and σ_i are the mean weight change obtained from biological experiments, the weight change obtained from the circuit under consideration, and the standard error mean of $\Delta w_{\mathrm{exp}}^i$ for a given data point i, respectively; p represents the number of data points in a specified data set.

Any resulting weight change observed in triplet-based/pair-based circuit is directly related to the model parameters that are a function of physical transistors sizes and bias voltages. In order to reduce E, an averaging mechanism combined with HSPICE optimization approach was used to find the optimum bias voltages in four different cases to have minimal NMSE. These four cases include: (i) pairing protocol with increasing frequency applied to the pair-based circuit with four parameters and (ii) to the triplet-based circuit with eight parameters; (iii) pair-based, quadruplet, and triplet protocols applied to the pair-based circuit with four parameters, and (iv) to the triplet-based circuit with eight parameters.

IV. Experimental Circuit Results

A. Classical pair-based STDP circuit results

In order to test the accuracy of classical pair-based STDP circuit (Fig. 1(a)), the same stimuli used in [2] are employed as follows: (1) firstly, we optimized the circuit parameters by using the visual cortex data, such that the final set of parameters were those where the NMSE was minimal ($E = 10.03$). This error is near to the error reported in the best case of parameters obtained from classical pair-based STDP in [2] ($E \cong 7.5$, data obtained from Fig. 6 in [2]). Despite using optimum parameters, the VLSI implementation of pair-based STDP clearly fails to generate the experimental data (see Fig. 3(a)). In addition, further simulations on pairing, quadruplet and triplet protocols were conducted. Again, we optimized the parameters of the VLSI implementation of pair-based STDP so that the NMSE was minimal across the entire data set, i.e. for all three protocols, we employed similar V_{A^+}, V_{A^-}, τ_+ and τ_- values. Again, the classical VLSI implementation for pair-based STDP, like its mathematical model, fails to reproduce the experimental data obtained using quadruplet and triplet protocols (Fig. 3(b)-(d)). The NMSE in this case was $E = 11.3$, which is close to the optimal value obtained from the pair-based model in [2] ($E \cong 10.5$, data obtained from Fig. 6 in [2]).

B. Proposed triplet-based STDP circuit results

A parameter readjustment was needed in order to obtain weight changes near to those seen in experiments. This was achieved using eight various bias voltages in the new circuit that are selected for having a minimal NMSE. These bias

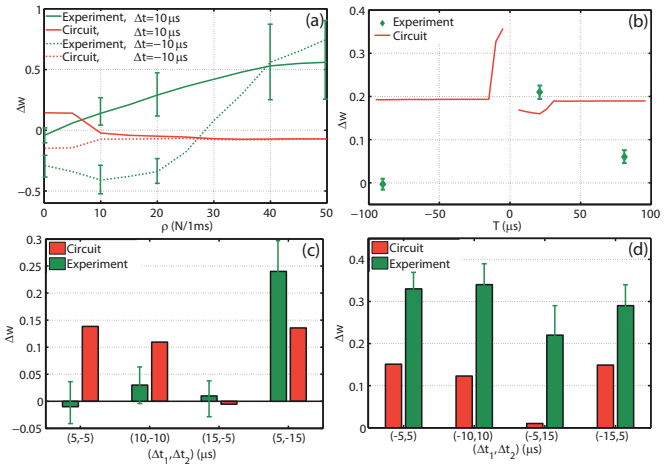

Fig. 3. Pair-based STDP circuit experiments. (a) Pairing protocol applied to the circuit for various pulse repetition rates. ρ is the pulse repetition rate of pre- and post-synaptic spike pairs in 1 ms. (b) Quadruplet protocol applied to the circuit for various Ts. T is the time difference between two different pairs of spikes as described in [2]. (c) and (d) Triplet protocols applied to the circuit for various delays. (c) is the pre-post-pre triplet and (d) is the post-pre-post triplet. Δt is used as described in [2].

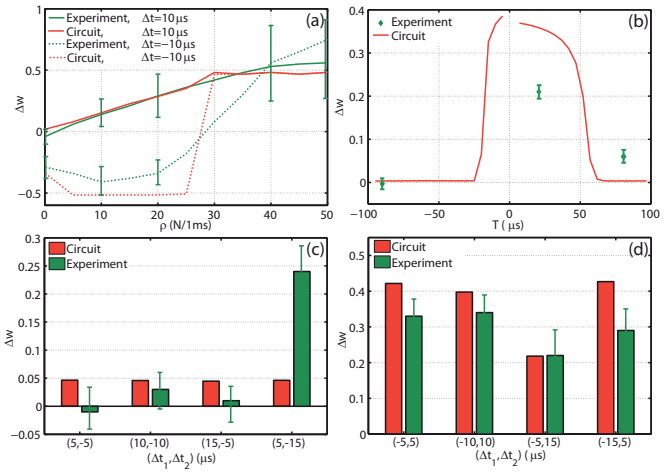

Fig. 4. Triplet-based STDP circuit experiments. (a) Pairing protocol applied to the circuit for various frequencies. (b) Quadruplet protocol applied to the circuit for various Ts. (c) and (d) Triplet protocols applied to the circuit for various delays. The values of ρ, T and Δt are used as described in [2].

voltages are as follows: V_{tp1}, V_{tp2}, V_{td1} and V_{td2} set τ_+, τ_y, τ_- and τ_x, respectively. In addition, $V_{A_2^+}$, $V_{A_2^-}$, $V_{A_3^+}$ and $V_{A_3^+}$ set A_2^+, A_2^-, A_3^+ and A_3^- correspondingly. It should be mentioned that the current circuit implementation in its present form is sensitive to variations in bias voltages, as it is the case with the original circuit by Indiveri et al. [1]. Hence, in the targeted implementation, each bias voltage will be provided by using a diode-connected MOS device in series with a current source (i.e for V_{tp1}, V_{tp2}, V_{td1}, V_{td2}, V_{A2+}, V_{A3+}, V_{A2-} and V_{A3-}).

The simulation results shown in Fig. 4(a)-(d) demonstrate that the proposed VLSI triplet-based circuit has a significantly improved weight change prediction capability in comparison to its pair-based counterpart. Like pair-based circuit experiments, Fig. 4(a) shows the total weight change induced by a pairing protocol for various pulse repetition rates. As can be seen from the figure, a better match between different experiments and simulations was observed. The NMSE achieved was $E = 0.82$, which is far better than the pair-based case and much closer to the analytical calculation of the triplet-based model given in [2] ($E = 0.22$, data obtained from Table 3 in [2]).

In addition, results for the triplet-based circuit, stimulated using the quadruplet or the triplet protocols, are also shown in Fig. 4(b)-(d). These results confirm that the triplet-based VLSI implementation can better mimic the corresponding weight changes observed in experiments, when compared to the pair-based circuit. For instance, the pair-based circuit induces similar weight changes for both $\Delta t_1 = -\Delta t_2 = 5$ μs and $-\Delta t_1 = \Delta t_2 = 5$ μs cases in triplet protocol experiments (Fig. 3(c)-(d)). However, the triplet-based circuit demonstrates a significantly better prediction in this case, as well as the other cases (Fig. 4(c)-(d)). The minimal NMSE for pairing, triplet and quadruplet protocols for the proposed triplet circuit was $E = 3.46$ which is consistent with the full-triplet model presented in [2] using analytical calculations ($E = 2.9$, data obtained from Table 3 of [2]).

C. Time scaling

In order to conduct all experiments given in [2], the pair-based or triplet based circuit should preserve the last value of the weight (capacitor value) and update it after the arrival of next set of spikes. In some cases it takes several seconds. To address this requirement, a large capacitor, in the order of tens of pico farad capacitance value would be needed. This issue was addressed in [1] through the use of a bistable circuit which drives the synaptic weight to either a high or low state on long time scales. Clearly this bistable circuit cannot be used to address the issue in the proposed circuit as synaptic weight in these experiments has an analog range and its last value must be kept and be updated at the required time to faithfully reproduce the required form of STDP. So, a scaling time by factor of 1000 was used. A similar strategy was used in [9], [11]. As a result, all time constants and delays are scaled accordingly. However, the presented results are consistent with biology and the mentioned scaling does not affect the circuit performance or functionality (compare Fig. 1(b) of this paper to Fig. 9(a) of [1]).

Conclusion

This paper proposes a novel VLSI implementation for the triplet-based STDP model first introduced by [2]. The triplet-based STDP circuit is a significant improvement in terms of mimicking biological experiments, when compared to the classical pair-based STDP circuit that is the conventional model for carrying out synaptic weight modifications. Using the new triplet-based STDP circuit, our simulation results show synaptic weight modifications that are much closer in form to what has been observed in electrophysiological experiments [5], [6], when compared with classical pair-based

implementation. Since the core parts of the proposed triplet-based STDP circuit, as it is the case with Indiveri's pair-based STDP circuit, are operating in the subthreshold region, they are susceptible to process variations in deep submicron technologies. Investigating the process variation effects on the functionality of the proposed design, and fabricating a learning chip based on triplet STDP are some of the next steps of this research.

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