A 250 MHz Level 1 Trigger and Distribution System for the GlueX Experiment

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Abstract– **The GlueX detector now under construction at Jefferson Lab will search for exotic mesons though photoproduction (10^8 tagged photons per second) on a liquid hydrogen target. A Level 1 hardware trigger design is being developed to reduce total electromagnetic (> 200 MHz) and hadronic (> 350 kHz) rates to less than 200 kHz. This trigger is deadtimeless and operates on a global synchronized 250 MHz clock. The core of the trigger design is based on a custom pipelined flash ADC board that uses a VXS backplane to collect samples from all ADCs in a VME crate. A custom switch-slot board called a Crate Trigger Processor (CTP) processes this data and passes the crate level data via a multi-lane fiber optic link to the Global Trigger Processing Crate (also VXS). Within this crate detector sub-system processor (SSP) boards can accept all individual crate links. The subsystem data are processed and finally passed to global trigger boards (GTP) where the final L1 decision is made.**

We present details of the trigger design and report some performance results on current prototype systems

I. Introduction

Thomas Jefferson National Accelerator Facility (Jlab) in Newport News, Virginia is home to a 6 GeV continuous electron beam accelerator with three fixed target experimental areas (Halls A, B, C). It has been in operation since 1994 and is now beginning construction of an upgrade to the facilities. This will include increasing the maximum energy of the accelerator to 12 GeV as well as upgrading the spectrometers and detector systems in all three experimental halls. In addition, there will be a brand new experimental area (Hall D) built.

The new physics program for the upgraded facility is expected to substantially increase demands on triggering and data acquisition particularly in Hall D where the GlueX experiment will require up to a 200 kHz Level 1 trigger rate and a 3 GB/s data rate off the front-end. In order to meet these requirements we are designing a pipelined, dead-timeless front-end coupled with a high-speed, low latency, synchronous, deterministic Level 1 trigger and distribution system. One of our secondary goals for this design, however, is to make sure that we take into consideration the substantial existing data acquisition infrastructure – including the crates, modules, cabling, CPUs, software, firmware, etc… This is particularly important for the existing Halls. The degree to which we can support older hardware and software while slowly migrating to the new technologies is critical both for the seamless operation of the current experimental programs as well as mitigating some of the substantial costs associated with upgrading all the existing systems to the new design.

In this paper we will describe all the components of the new design for a Level 1 trigger system. It is based on a distributed synchronous 250 MHz clock that drives both the deterministic calculation of the triggers as well as the distribution of the trigger information to all front-end systems. We will also discuss an implementation of this system for the new GlueX experiment under construction at Jlab (Hall D).

II. The GlueX Detector

The GlueX experiment (*glu*onic *ex*citations) is attempting to study quark confinement in the production and spectroscopy of hybrid mesons through the interaction of linearly polarized photons on a liquid hydrogen (proton) target. The partial-wave analysis necessary to study this spectrum requires a detector hermetic in energy and very large statistics. Bremstrahlung photons produced by a continuous beam of 12 GeV electrons on a diamond crystal will be collimated providing a total flux incident on the target of up to $3x10^9$ photons/sec and 10^8 photons/sec in the coherent peak ($8.4<E_\gamma<9.0$ GeV). The total hadronic production rate from the target will be around 360 kHz with an energy spectrum shown in Fig. 1. In addition to the low energy hadronic background there is also a very large electromagnetic background generated through Compton scattering and pair-production in the target and detector. This background production is expected to be on the level of 200 MHz.

The GlueX experiment will implement two levels of triggering. Level 1 (L1) will be hardware-based and will have a goal of reducing the total rate to less than 200 kHz (3 GB/s) by eliminating a majority of the electromagnetic and making a low-energy cut on the hadronic background (Fig. 1). A Level 3 cut (L3) will be in software and will attempt to reduce the L1 rate by another order of magnitude. It will be implemented as an online farm. Final rates to storage are expected to be less than 20 kHz and 300 MB/s.

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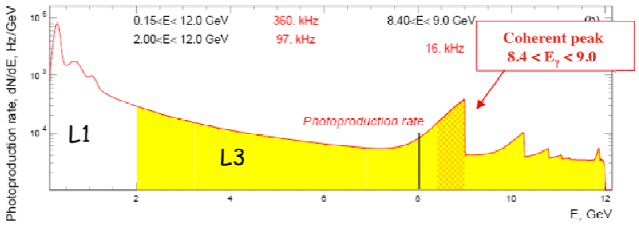
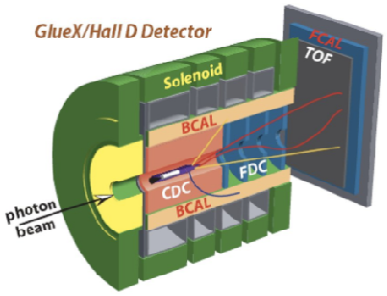


Fig. 1 Hadronic photoproduction rates as a function of photon energy for bremstrahlung photons produced from a 12 GeV incident electrons. L1 and L3 represent approximate cuts anticipated by hardware and software triggers for the GlueX detector.

A schematic drawing of the GlueX detector subsystems is shown in Fig 2 along with channel count information and a list of sub-subsystems that are expected to contribute to the L1 trigger. Of the five listed the two most important systems are the Forward and Barrel Calorimeters (FC and BC). Distributions of the total energy in the forward verses transverse directions will be critical. The Tagger will be of limited use at the highest luminosities due to large count rates. The Start Counter and Forward Drift chambers may be able to provide additional information on track counts.



Total Channels: ~22k
L1 Data rate: ~3 GB/sec
L3 Farm: 20 kHz, 300 MB/s to Disk
Detector subsystems:
- **Tagger (L1 -Hits)**
- **Pair spectrometer**
- **Start Counter (L1 - Hits)**
- **Central Drift Chamber**
- **Forward Drift Chambers**
- **Time of Flight (L1 – Hits)**
- **Barrel Calorimeter (L1 - Energy)**
- **Forward Calorimeter (L1 - Energy)**

Fig. 2 GlueX Detector sub-systems. Those systems expected to be included in the Level 1 trigger are indicated. The two calorimeters are the primary contributing systems.

III. Level 1 Design

In order to realize the L1 requirements, front-end data processing times must average less than 5 µs. We must also provide a high speed, synchronous and deterministic method to collect the trigger-related data to make a decision. We decided to base our electronic designs on the commercial standard VITA 41 [1] or VXS (VME switched serial). This combines a standard VME64X backplane with an additional high-speed serial fabric as an alternative data path. Two standard VME slots are replaced with special "switch" slots, so there are only a total of 18 VME "payload" slots remaining in the crate. In particular we are using the VITA 41.2 (RapidIO) specification [1] that defines a dual-star topology including a total of eight full-duplex lanes (4 in and 4 out) to each of the two resident switch slots. Use of VXS has the added benefit of supporting much of the legacy electronics that are being used in the current 6 GeV program, and we can seamlessly mix and match new hardware designs with the old for future experiments.

Instrumentation of the GlueX detector will require up to 50 VXS crates and 12 standard VME64X crates. The detector sub-systems that will contribute to the L1 trigger will house electronics in the VXS crates. The idea behind the trigger is to build a decision with data from an individual VME *Board* then to the *Crate* level. Each crate will contribute to their specific *Sub-System*, and all sub-systems will pass data to a *Global* processor.

At the board level we have designed a 16 channel flash ADC (FADC). It supports a 10 or 12 bit resolution sampling at 250 MHz (every 4 ns). A functional diagram of the board is shown in Fig. 3. Two Xilinx LX25 FPGAs [2] keep a pipeline of 8 µs of samples for each of eight channels. In addition they process data (clocked every 4 ns) and provide sums and hits (i.e. samples over programmed channel thresholds) to a third FPGA (Xilinx FX20). This FPGA is responsible for local trigger processing or for passing serialized data out via the VXS P0 connector. We use the FX20 RocketIO ports and Xilinx's Aurora protocol to bond two of four available VXS lanes to send data at 2.5 Gbps per lane. Utilizing 8b/10b encoding this effectively provides a 500 MB/s link to switch slot A. Meanwhile, if an external trigger arrives at the FADC board, the relevant data in the LX20 pipeline is copied out and buffered locally for readout over the standard VME channel. The FADC board supports the new high-speed VME block readout modes (2eSST transfers) at up to 200 MB/s. The Jlab FADC supports several different processing modes and can be loaded with new FPGA firmware via VME at runtime.

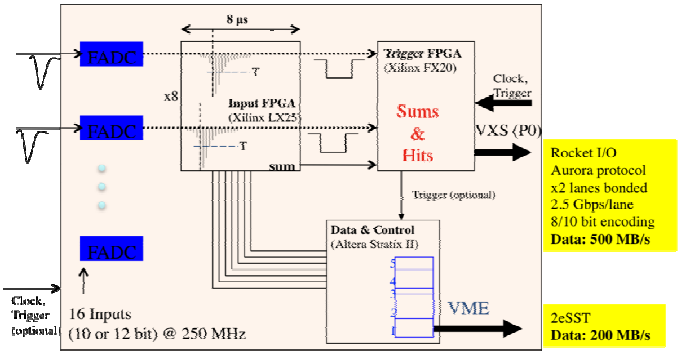


Fig. 3 Jlab 250 MHz Flash ADC functional diagram. It is a 6U VME64X/VXS board with 16 input channels.

The second board design at the crate level is the Crate Trigger Processor (CTP). It resides in switch slot A. It can accept up to 16 FADC trigger data streams via VXS from the payload slots and can make a crate level trigger decision. The

board houses two Xilinx LX50 FPGAs [2] for collecting and aligning the VXS data, and a third LX110 [2] for trigger processing. The LX110 can also transport trigger data off the crate via four bonded RocketIO ports (also 2.5 Gbps). This represents a total bandwidth of 1 GB/s (or 64bits @ 125 MHz). The external fiber link utilizes the Avago HFBR-7934 parallel fiber optic module [3] (4 chan full duplex) and a multi-fiber (12) ribbon cable that supports 3.125 Gbps for up to 150 meters. Each front-end crate participating in the L1 trigger will require a CTP.

A companion board residing in switch slot B that we have designed for all VXS crates is the Signal Distribution Board (SD). It is responsible for distribution to all slots: the common 250 MHz clock, the accepted trigger signal, synchronization pulses. It is also capable of collecting status signals from all front-end boards indicating errors or buffer full conditions.

A. Global Trigger Crate

The Sub-System and Global Level processing for the L1 trigger design is implemented within a single VXS crate (The Global Trigger Crate). The architecture includes two additional board designs. Functional block diagrams for these boards are shown in Fig. 4.

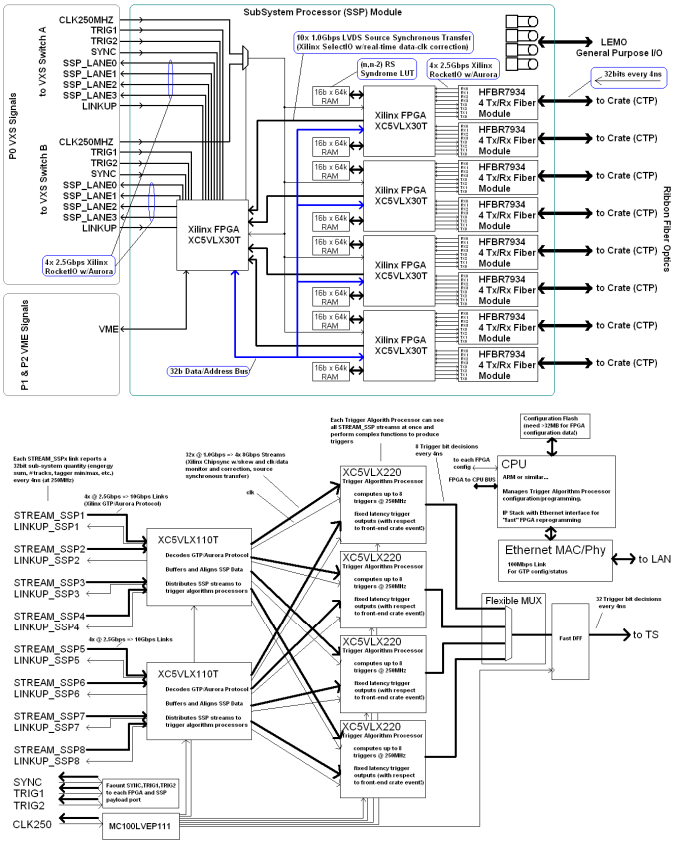


Fig. 4 Sub-System Processor (SSP) and Global Trigger Processor (GTP) functional block diagrams are shown. Both boards reside in the global trigger crate.

The first board is the Sub-System Processor (SSP). It resides in a payload slot and is responsible for collecting external serial inputs from up to eight separate CTP modules (via multi-fiber cable). For the GlueX experiment up to eight separate SSP modules will be necessary to collect all trigger data from front-end VXS crates. Both calorimeter sub-systems will require two SSPs to aggregate the data. All other detector systems will need only single SSPs. All SSPs are identical in hardware design, however individual SSPs can be loaded via VME at runtime with firmware that is specific to the different detector systems they are responsible for. Each SSP is capable of an independent trigger decision but can also pass its data to both switch slots (A&B) via a bound four-lane serial link on VXS P0 (total bandwidth 1GB/s).

The second board is the Global Trigger Processor (GTP). It resides in either switch slot or in both if additional processing is required. It is responsible for collecting all sub-system data and computing the final trigger decisions. Its behavior is similar to a two-stage event-building switch. The first stage decodes serial data from up to eight inputs (the SSPs) and aligns the data with respect to timestamps and programmable delays. It then distributes this data to four separate FPGAs. Each FPGA in the second stage is responsible for calculating up to eight separate triggers. All processing is driven by the 250 MHz common clock. The 32 independent triggers are mux'd and output on a ribbon differential twisted pair cable every 4ns. This serves as the input to the Trigger Distribution System.

B. Trigger/Clock Distribution

The Trigger Distribution System is the link between the trigger system and the data acquisition system. It is the central control point for managing multiple sources of triggers (physics and calibration). It must prescale and distribute trigger information to the front-end with a fixed but programmable latency, and it must collect and monitor all status and error information returning from the crates in order to manage the pipeline. Finally, it is the source and synchronization point for the master 250 MHz clock.

The trigger distribution crate will utilize a VXS backplane as well. In this crate there are three types of custom boards. In VME payload port 18 the Trigger Supervisor (TS) resides. It is responsible for accepting the 32 bit GTP output as well as any additional asynchronous triggers. Inputs are subject to prescaling and a coincidence window before being latched. All accepted inputs are synchronized to the 250 MHz clock. A User programmable lookup table establishes a 16 bit primary trigger "strobe" word to be distributed to the front-end crates with fixed latency. Optional secondary words can be generated that include additional information but are not prompt. The accepted trigger data, the 250 MHz clock and a clock synchronization signal (CLKSYNC) are serialized, encoded and bonded and sent via three lanes on the VXS backplane to switch-slot B.

An SD card in slot B fans-out the TS data to each of 16 payload ports in the crate. Each payload port holds a custom board called the Trigger Distribution Module (TD). The TD has eight HFBR-7934 multi-fiber transceivers that can distribute the TS data to the crates. With a total of sixteen TD modules in the trigger distribution crate the system has the ability to support up to 128 total front-end crates. This is

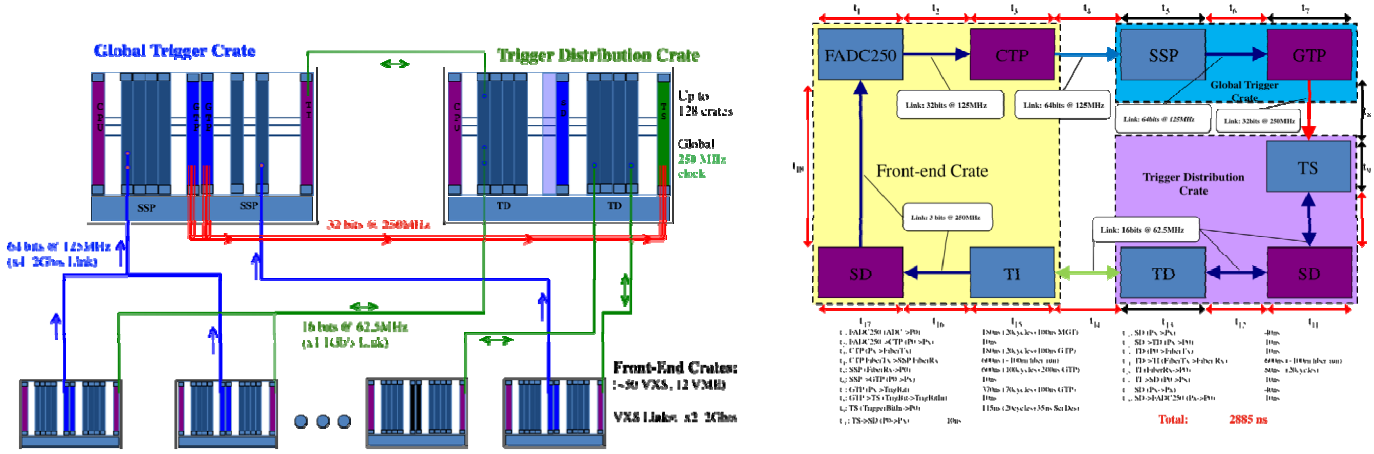


Fig. 5 An example L1 trigger and distribution system layout is shown for the GlueX experiment. L1 data fiber uplinks are shown in blue, and the accepted trigger distribution links are shown in green. All front-end crates – both VME and VSX receive accepted trigger and clock info. Only those crates contributing data to L1 have uplinks (via CTP) to the global trigger crate. A Timing diagram for the L1 trigger and distribution system is shown on the right. Total latency from input to the FADC to the return of an accepted trigger is less than 3 µs.

significantly more than any anticipated expansions of experiments at the lab.

The link back to the front-end crates is completed with one final custom board that sits in payload slot 18. This module is called the Trigger Interface (TI), and it is a simplified version of the TS. It accepts the point-to-point link with the TD and decodes the trigger/clock/sync data. With the highest expected L1 accepted trigger rates on the order of a few hundred kilohertz, the TD-TI link runs only at 16 bits @ 62.5 MHz (i.e. every 16 ns). Trigger words are stored in a local FIFO and are processed synchronously. The TI is responsible for distributing these signals to the local crate SD (in switch slot B), and for buffering up accepted trigger data, time stamps, etc. for VME readout. The TI also has the ability of operating in a local mode without the distribution system so that crates can be used individually for detector testing or development. Finally, the TI has a high-speed return path to the TD over the same multi-fiber cable it receives data on. It can use this to send crate status. This includes busy or error conditions, but it can also operate in a handshake mode whereby each trigger is acknowledged before the next one is sent from the TS.

A diagram of an example L1 trigger and distribution system is shown in Fig. 5. Details on the serial data links are specified as are the positions of all the custom modules in the various crates (e.g. payload slot 18 is the left most slot, while switch-slots are in the middle). Also in Fig. 5 we show the same system with an analysis of the all the times for transport and processing of data at each stage of the system. Most times have been measured in the lab but some are estimates based on simulations for various trigger types. We have attempted to be conservative in those estimates. The total time from sampling data at the FADC to returning an accepted trigger to the FADC board to initiate VME readout is less than 3 µs. This is well below the required 4 µs latency required by some of the front-end electronics.

IV. Status

Currently four of the eight VXS board designs for the trigger system have been prototyped and tested in the lab (FADC, CTP, TI, and SD). The FADC is being used in existing production experiments. We have established the proof of principle for crate-level summing with up to four FADCs in a single crate contributing via the VXS backplane. In addition we have demonstrated multi-crate clock synchronization and fixed-latency trigger distribution with two crates separated by 150 m. Relative stability of the 250 MHz timestamps and trigger counts have remained synchronized (with no loss) over many hours at 150 kHz rates.

We are currently beginning prototypes of the remaining boards (SSP, GTP, TS, TD) and hope to integrate testing within the next year.

V. Conclusion

The 12 GeV upgrade for Jlab is bringing with it new challenges for triggering and data acquisition. With the adoption of the VITA 41 VME switched-serial extensions (VXS) we believe we have developed a system that will not only meet the increased demands but also provide support for the existing systems running in the 6 GeV program. The new L1 trigger and distribution system is modular such that pieces can be used at the individual board, crate, subsystem or global level. We have demonstrated with the new system that the demands for the GlueX Experiment in Hall D can be met with only a fraction of the available bandwidth that is specified by the hardware standards and serial protocols. This will allow for future expansion as experiments require.

References

[1] ANSI/VITA 41.X-2006 standard specifications are available from http://www.vita.com/

[2] Xilinx Corporation, San Jose, CA. http:/www.xilinx.com/

[3] Manufactured by Avago Technologies, San Jose, CA.