A New Compact Analog VLSI Model for Spike Timing Dependent Plasticity

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Abstract—Spike Timing Dependent Plasticity (STDP) is a timebased synaptic plasticity rule that has generated significant interest in the area of neuromorphic engineering and Very Large Scale Integration (VLSI) circuit design. During the last decade, STDP and STDP-like learning mechanisms have shown promising solutions for various real world applications, ranging from pattern recognition to robotics. This paper presents a novel analog VLSI model for STDP that possesses advantages compared to previously published VLSI STDP designs. The presented STDP circuit is capable of reproducing the outcomes of several well known experiments using various plasticity rules inducing STDP protocols that utilise pairs, triplets, and quadruplets of spike patterns. When the circuit is compared to state-of-the-art VLSI STDP circuits, it shows a compact and symmetric design that makes the proposed circuit a powerful component for use in designing STDP or time-based Hebbian learning experiments and applications.

I. INTRODUCTION

Neuromorphic VLSI is the realm of design and implementation of phenomenological and biophysical models of neurons and synapses. It dates back to the early 90's with early research pioneered by Carver Mead [1]. Ever since, many neuromorphic engineers have been attempting to implement neurons and synapses in VLSI with various degrees of details and levels of abstraction aimed at benefiting from the low power and compact implementations offered by VLSI technology. There are many examples of VLSI neurons and synapses in the literature [2]-[6]. Neurons are the producers of action potentials (spikes), and synapses are the interfacing elements among neurons, believed to be where learning and memory takes place in the brain. When implementing a synapse within a larger system, such as a network, one should implement the mechanism under which the synaptic efficacy can be altered by pre-synaptic and post-synaptic activities, also referred to as the synaptic plasticity rule [7]. This is in order to ensure that the strength of a synapse can adjust to changes in response to these activities, thus allowing the system to adapt to a dynamic environment [8]. In the past, there have been various rules presented that modify the synaptic weights in response to different parameters including but not limited to, i) the activity of pre- and post-synaptic neurons [7], ii) the timing of the spikes from pre- and post-synaptic neurons [9], iii) the membrane potential of the post-synaptic neuron [10], or iv) a cooperative and simultaneous interaction of parameters mentioned in (i) to (iii) [11]. Various VLSI implementations of these rules exist in the literature [5], [12]. In these implementations, the main

goal has been to reproduce the results of neurophysiological experiments but, simultaneously, there has always been effort aimed at reducing the area occupied by these learning circuits and/or minimising their power consumption.

This paper presents a novel analog VLSI circuit model for triplet-based STDP (TSTDP). The new design presents a significant improvement in terms of physical implementation area and less power compared to previous implementations presented in [2], [5], [6], [12]–[14] without compromising the output response performance when compared to biological experiments. More details on how we achieve this improvement is presented in Section III. The circuits are also compared in the discussion and comparison section of the paper.

II. PREVIOUS PAIR AND TRIPLET SPIKE TIMING DEPENDENT PLASTICITY CIRCUITS

A. Pair-based STDP Circuits

Pair-based STDP is the conventional form of a synaptic plasticity rule that potentiates the synaptic efficacy of a synapse, if a pre-synaptic spike precedes the post-synaptic action potential. In contrast, synaptic depression occurs when the order of spikes is reversed, namely if a post-synaptic neuron fires a spike before its pre-synaptic afferent [15]. A well-known phenomenological representation of the PSTDP that implements the above mentioned mechanism is shown in Eq. 1,

$$\Delta w = \begin{cases} \Delta w^+ = A^+ e^{\left(\frac{-\Delta t}{\tau_+}\right)} & \text{if } \Delta t \ge 0\\ \Delta w^- = -A^- e^{\left(\frac{\Delta t}{\tau_-}\right)} & \text{if } \Delta t < 0 \end{cases},$$
(1)

where $\Delta t = t_{\text{post}} - t_{\text{pre}}$ is the time difference between a single pair of post- and pre-synaptic spikes, τ_+ and τ_- are time constants of the learning window, and A^+ and A^- represent the maximal weight changes for potentiation and depression, respectively [16].

From a circuit designer point of view, one can represent the synaptic weight (w) with a voltage stored across a capacitor and hence implement the changes in synaptic weight (Δw) with charging and discharging the capacitor. The amount of the charging and discharging that represents the required potentiation and depression of the synaptic weight can be controlled using circuitry that respectively determine the amount of current flowing in and out of the capacitor.

There are a number of circuits e.g. those presented in [2], [4], [6], [12], [17] that approximate Eq. 1. Some of these circuitries implement the potentiation and depression mechanisms of this equation and do not implement the exact exponential form shown in the PSTDP phenomenological model presented in Eq. 1. Although these circuits cannot generate the exponential learning window, they can regenerate some of the biological experiments and also show the potentiation and depression potentials as the basic parts of the PSTDP rule. Examples of these circuits that implement PSTDP rule are in [4], [13]. These circuits are able to generate a learning window with depression and potentiating components occuring for the expected combination of spikes, however it is not the exponential learning window typically used in simulation studies [18], [19].

On the contrary, there are some other VLSI designs for PSTDP that are good approximations of Eq. 1. These designs utilise transistors in their sub-threshold (weak inversion) area of operation and therefore take advantage of their exponential Drain-Source current to charge and discharge the synaptic weight capacitor in an exponential manner. The circuit proposed in [20] is a good example of this type of design.

B. Triplet-based STDP Circuits

In addition to pair-based interactions between pre- and postsynaptic spikes, the TSTDP rule takes into account higher order interactions between combinations of triplets of preand post-synaptic spikes to alter the synaptic weight [21]. A mathematical representation of this learning rule is given by

$$\Delta w = \begin{cases} \Delta w^{+} = e^{\left(\frac{-\Delta t_{1}}{\tau_{+}}\right)} \left(A_{2}^{+} + A_{3}^{+} e^{\left(\frac{-\Delta t_{2}}{\tau_{y}}\right)}\right) \\ \Delta w^{-} = -e^{\left(\frac{\Delta t_{1}}{\tau_{-}}\right)} \left(A_{2}^{-} + A_{3}^{-} e^{\left(\frac{-\Delta t_{3}}{\tau_{x}}\right)}\right), \end{cases}$$
(2)

where $\Delta w = \Delta w^+$ for $t = t_{\text{post}}$ and if $t = t_{\text{pre}}$ then the weight change is $\Delta w = \Delta w^-$. Here A_2^+ , A_2^- , A_3^+ and A_3^- are potentiation and depression amplitude parameters, $\Delta t_1 = t_{\text{post}(n)} - t_{\text{pre}(n)}$, $\Delta t_2 = t_{\text{post}(n)} - t_{\text{post}(n-1)} - \epsilon$ and $\Delta t_3 = t_{\text{pre}(n)} - t_{\text{pre}(n-1)} - \epsilon$, are the time differences between combinations of pre- and post-synaptic spikes. Here, ϵ is a small positive constant that ensures that the weight update uses the correct values occurring just before the pre or postsynaptic spike of interest, and finally τ_- , τ_+ , τ_x and τ_y are time constants [2].

In analogy to the PSTDP circuits, the TSTDP circuits can be designed using two different approaches. The first approach designs the circuit in a way that it has the capability to reproduce an exponential behavior shown in Eq. 2, e.g. the design presented in [20]. The second approach, however, does not result in the exponential behavior and only implements the timing-based potentiation and depression mechanisms such as the design presented in [4]. Using these approaches, a number of VLSI designs for TSDTP have been presented in the literature. As already mentioned, the benefit of implementing a TSTDP circuit is its increased capabilities in reproducing behavior found in complicated biological experiments that the PSTDP circuit fails to reproduce. Our previous studies show that the exponential form of the PSTDP and TSTDP hypothesis are not really necessary for generating the experimental results observed in hippocampal [22] and visual cortex experiments [21], [22]. The TSTDP circuit presented in [6], [17] does not demonstrate the exponential learning window, nonetheless, it is still able to reproduce the behavior of the targeted biological experiments fairly similar to its counterparts with exponential capabilities that are presented in [2], [12].

This paper presents a new design for a TSTDP rule that utilises the second approach and aims at implementing the required synaptic dynamics for potentiation and depression and not the hypothetical exponential behavior presented in Equations 1 and 2. The circuit and its simulation results are presented in the following sections.

III. PROPOSED TRIPLET-STDP CIRCUIT

The proposed circuit for the triplet STDP rule (shown in Eq. 2) is demonstrated in Fig. 1. This circuit operates as follows: When a pre-synaptic spike, $V_{\text{pre}(n)}$, is received at the gate of M6, V_{pot1} reaches ground resulting in switching on M8, and then starts to increase linearly toward V_{dd} with a rate determined by V_{tp1} that is applied to the gate of M5. In fact, V_{pot1} that controls the existence of the potentiation in the first place and allows the current to flow through the potentiation branches (M7-M9 and/or M15-M16-M8-M9) at the time of arrival of a post-synaptic spike at M9, represents the first potentiation term in Eq. 2 shown as $e^{\left(\frac{-\Delta t_1}{\tau_+}\right)}$.

Furthermore, the addition term shown in the second term of first line of Eq. 2 that determines the amount of potentiation as a result of both pair and triplet terms, is approximated through a sum of two currents. The first current is controlled by $V_{A_2^+}$, while the second one is controlled by $V_{A_3^+}$ and the second potentiation dynamic, V_{pot2} . This voltage depends on the arrival time of the previous post-synaptic spike, $V_{\text{post}(n-1)}$. When a post-synaptic spike arrives at M18, V_{pot2} reaches ground and after the post-synaptic pulse duration is finished, it starts to increase linearly toward V_{dd} with a rate determined by V_{tp2} that is applied to the gate of M17. Therefore, the current flowing through M15-M16 approximates $A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)}$. This current accumulates in the circuit with another current controlled by $V_{A_2^+}$ and forms an approximation to $\left(A_2^+ + A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)}\right)$, which represents the second term of the first line of Eq. 2.

The same dynamic operates in the depression half of the proposed circuit, in which current flows away from the weight capacitor, C_w . In this part, current will flow through M10-M12 if there has been a post-synaptic action potential in a specified time window defined by V_{td1} (which corresponds to τ_-), before a pre-synaptic spike. In addition, another current that can discharge the capacitor and results in a depression, will flow through M10-M11 and M3-M4, if there has been a previous pre-synaptic spike in a specified time window, set by V_{td2} (which corresponds to τ_x), before the current pre-synaptic spike arrives at M10 and with the condition of having a post-synaptic spike arrived at M13 in a specified time



Fig. 1. Proposed circuit for the full TSTDP rule. The circuit for minimal TSTDP does not include transistors M1-M4 shown in the dashed box.

window set by V_{td1} before the current and after the previous pre-synaptic spikes.

This circuit is a major improvement over our previous circuit presented in [6]. In our previous design, there are four branches resulting in increases or decreases in the voltage across the weight capacitor, two of which are associated with depression and the other two with potentiation. In the new proposed design, there is only one pull-up transistor branch (M7-M9) for potentiation and one pull-down branch (M10-M12) for depression. In other words, the previous design approximates a rearrangement of Eq. 2 shown as

$$\Delta w = \begin{cases} \Delta w^+ = A_2^+ e^{\left(\frac{-\Delta t_1}{\tau_+}\right)} + A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)} e^{\left(\frac{-\Delta t_1}{\tau_+}\right)} \\ \Delta w^- = -A_2^- e^{\left(\frac{\Delta t_1}{\tau_-}\right)} - A_3^- e^{\left(\frac{-\Delta t_3}{\tau_x}\right)} e^{\left(\frac{\Delta t_1}{\tau_-}\right)}. \end{cases}$$
(3)

Hence as Eq. 3 shows, two instances of $e^{\left(\frac{-\Delta t_1}{\tau_+}\right)}$ during potentiation and two instances of $e^{\left(\frac{\Delta t_1}{\tau_-}\right)}$ during depression are needed. As a result more transistors are used to duplicate similar dynamics of the equation. We can also remove four transistors from the time constants dynamics in the design and use only a single transistor to form potentiation and depression dynamics. Considering these insights, the new circuit uses eight transistors less to implement the full TSTDP rule and therefore it requires only 18 transistors arranged in a symmetric and compact form as shown in Fig. 1. This potentially represents an area saving of 30%.

IV. SIMULATION RESULTS

This section presents simulation results of a minimal triplet circuit that corresponds to the minimal TSTDP rule presented in [21]. As the rule is minimised, the proposed circuit also can be further modified and hence the number of transistors is reduced. According to the minimal rule presented in [21], the depression contribution of the spikes triplet interactions can be neglected without having a significant effect on the circuit performance in reproducing the targeted biological experiments. The triplet depression part in the full TSTDP circuit (Fig. 1), is the four transistors surrounded in the reddashed box. Therefore, the minimal TSTDP circuit, is the one shown in Fig. 1 minus the part enclosed in the red dashed box, i.e only 14 transistors are needed to generate all desired biological experiments.

The minimised circuit was simulated in HSpice using the 0.35 μ m C35 CMOS process by AMS. All transistors in the design (shown in Fig. 1) are set to 1.05 μ m wide and 0.7 μ m long. The weight capacitor value is set to 50 fF. It should be noted that the circuit was simulated in an accelerated time scale of 1000 times compared to real time. However, for the sake of simplicity when comparing the results to the experiments, all shown results are scaled back to real time. Furthermore, in the shown simulation for the hippocampal experiments, we have used one pair, triplet or quadruplet of spikes to perform the required weight modifications under various protocols that will be discussed in the following subsections. In addition, the nearest-spike interaction of spikes to the nearest-spike model of TSTDP rule presented in [21].

In each of the following subsections a figure is presented that shows how the circuit performs weight modifications compared to the experimental data. In each figure, the data in black represents the experimental mean weight change under a specific protocol (i.e. pairing, quadruplet, and triplet) and the black bars show the standard error mean of weight changes. In addition, the red lines show the weight change, Δw , predicted by the circuit under the same protocol as the experiments. The data points and the error bars are exactly those that have been used in [21], in order to test their proposed TSTDP model. Since the proposed design in this paper is a synthesis of this TSTDP model, same data points and error bars have been utilized to test the designed circuit.

A. Pairing experiments (STDP learning window)

The first simulation performed on the proposed circuit was reproducing the STDP learning window that demonstrates spike timing dependent potentiation and depression. Fig. 2 shows how the proposed circuit can successfully perform the timing dependent weight modifications. This figure shows the normalised experimental data extracted from [9] in blue. It suggests that the proposed circuit behavior under a pairing (window) protocol, which considers a pair of pre- and postsynaptic spikes with a delay of $\Delta t = t_{\text{post}} - t_{\text{pre}}$ can approximate the experimental data generated with the same protocol. Beside the blue experimental data, two other experimental values for $\Delta t = 10$ and $\Delta t = -10$ are shown with their standard error mean represented by black bars. These points are those used in [21] and therefore we use them for testing our circuit performance as we are implementing the circuit for the model presented in [21].

B. Quadruplet experiments

In addition to the pairing experiments, the proposed circuit is also able to generate the result produced in biological



Fig. 2. STDP learning window produced by the proposed minimal TSTDP circuit under pairing protocol.

experiments using quadruplet of spikes in the forms of prepost-post-pre or post-pre-post. The utilised quadruplet protocol in our simulation is the same protocol that has been used in the hippocampal experiments in [22] and also has been used to model the TSTDP rule in [21]. Figure 3 shows the simulation results along with the biological experiment results performed in the hippocampal and under quadruplet protocol. One quadruplet of spikes has been used to generate the shown results. The quadruplet is composed of either a postpre pair with a delay of $\Delta t_1 = t_{post1} - t_{pre1} < 0$ precedes a pre-post pair with a delay of $\Delta t_2 = t_{\text{post}2} - t_{\text{pre}2} > 0$ with a time T > 0, or a pre-post pair with a delay of $\Delta t_2 = t_{\rm post2} - t_{\rm pre2} > 0$ precedes a post-pre pair with a delay of $\Delta t_1 = t_{post1} - t_{pre1} < 0$ with a time T < 0, where $T = (t_{\text{pre2}} + t_{\text{post2}})/2 - (t_{\text{pre1}} + t_{\text{post1}})/2$. Similar to [21], in the quadruplet experiment in this paper, $\Delta t = -\Delta t_1 = \Delta t_2 =$ 5 μs . Figure 3 depicts that our simulation results are in a good agreement with the behavior observed in the experiments and also it is similar to the results obtained using mathematical model of TSTDP presented in [21].

C. Triplet experiments

In addition to window, and quadruplet experiments shown in previous sections, the proposed circuit can replicate similar behavior to biological experiments under spike triplet protocol. This protocol is as follows: There are two different patterns of triplet spikes. The first triplet pattern is composed of two presynaptic spikes and one post-synaptic spike in a pre-post-pre configuration. As a result, there are two delays between the first pre and the middle post, $\Delta t_1 = t_{\text{post}} - t_{\text{pre1}}$, and between the second pre and the middle post $\Delta t_2 = t_{\text{post}} - t_{\text{pre2}}$. The second triplet pattern is analogous to the first but with two post-synaptic spikes, one before and the other one after a pre-synaptic spike (post-pre-post). Here, timing differences are defined as $\Delta t_1 = t_{\text{post}1} - t_{\text{pre}}$ and $\Delta t_2 = t_{\text{post}2} - t_{\text{pre}}$.

Figure 4 demonstrates a good match between experiments and the triplet simulation results obtained using the proposed minimal TSDP circuit. This figure depicts how well the proposed TSTDP circuit can distinguish between pre-post-pre (Fig. 4-a) and post-pre-post (Fig. 4-b) experiments, the ability



Fig. 3. Quadruplet experiments performed in the hippocampal and qualitatively replicated using the proposed minimal TSTDP circuit.

TABLE I MINIMAL TSTDP CIRCUIT BIAS PARAMETERS FOR REPLICATING THE HIPPOCAMPAL EXPERIMENTS INCLUDING PAIRING, TRIPLET AND QUADRUPLET EXPERIMENTS.

Parameter name	$V_{\rm tp1}$	$V_{\rm tp2}$	$V_{\rm td1}$	V_{A2+}	V_{A2-}	V_{A3+}
Bias voltage (V)	2.73	2.75	0.25	2.69	0.37	2.96

that all previous PSTDP circuits are clearly lacking [6], [21].

The bias voltages used to generate the results in Figs. 2 to 4 are shown in Table I. These are corresponding bias voltage parameters that are used for the triplet, quadruplet and pairing (window) experiments. In order to show how good the circuit can approximate all these experiments, the Normalised Mean Square Error (NMSE) can be defined as

$$\text{NMSE} = \frac{1}{p} \sum_{i=1}^{p} \left(\frac{\Delta w_{\text{exp}}^{i} - \Delta w_{\text{cir}}^{i}}{\sigma_{i}} \right)^{2}, \tag{4}$$

where Δw_{exp}^i , Δw_{cir}^i and σ_i are the mean weight change obtained from biological experiments, the weight change obtained from the circuit under consideration, and the standard error mean of Δw_{exp}^i for a given data point *i*, respectively; *p* represents the number of data points in a specified data set (in the case of this paper, p = 13). These 13 points include, eight points from triplet experiments shown in Fig. 4, three points from quadruplet experiments shown in Fig. 3, and finally two points from pairing experiments shown in Fig. 2. These 13 points are selected in a way similar to the main TSTDP study [21].

Circuit simulation results show a NMSE equal to 1.40 which is better than the reported NMSE value of 2.9 that was calculated using the mathematical model of minimal TSTDP rule and optimised parameters presented in [21].

V. DISCUSSION AND COMPARISON

Simulation results in Section IV demonstrate how the proposed minimal TSTDP circuit that has only 14 transistors can replicate the results of various STDP experiments and obtain a low NMSE for different experiments. In this regard, there are a number of points that should be noted.

1) Here the circuit does not show an exponential learning window for potentiation and depression, but simulation results



Fig. 4. Triplet experiments performed in the hippocampal and qualitatively replicated using the proposed minimal TSTDP circuit. The black bars represent the experimental mean weight change and the lines on them show the standard deviations observed in the experiments and for various values of Δts . (a) Simulation using a pre-post-pre combination of spikes with shown Δt_1 and Δt_2 , (b) Simulation using a post-pre-post combination of spikes with shown Δt_1 and Δt_2 .

in this paper as well as [6] suggest that the exponential behavior is not necessarily needed for regenerating the required biological behaviors. One should keep in mind that the exponential behavior shown in Eq. 1 is only a hypothesis that can approximate the behavior found in some biological experiments including the learning window, but in its pair-based form it is not able to account for more complicated experiments e.g. triplet, quadruplet and pairing frequency experiments. The proposed circuit is an efficient design, that can reproduce the results from complicated experiments reported in [21], [22], while using a fewer number of transistors compared to other designs with the same capabilities.

2) In terms of the number of transistors, the proposed circuit is simpler and takes fewer transistors to implement the minimal TSTDP rule, compared to all previous designs presented in [2], [6], [12]. More importantly, the proposed design that implements the complex TSTDP rule has a fewer number of transistors than several of other VLSI circuit designs for the PSTDP rule presented in [13], [14], [20]. This highlights an improved design in two very significant aspects for neuromorphic VLSI design, compactness and low power consumption.

3) The proposed design uses a 50 fF capacitor, which makes the design suitable for plasticity experiments either for short term plasticity or with high spike frequency. However, for lower spike frequencies and long term plasticity, the latest updated value across the capacitor will start to leak away. This is a well-known problem that has been tackled in different ways by neuromorphic engineers [3]. A possible approach to address this issue is to employ a bistability mechanism proposed and used by Indiveri et al. in [4]. Using their approach, the weight is modified in the presence of pre- and post-synaptic spikes using the STDP circuit, and when there is no spike arriving at the STDP circuit, the stored voltage across the weight capacitor is pushed either upward to a predetermined maximum, or downward to a specified minimum voltage. Another approach is to utilise standard memory such as SRAM to store the latest value of the weight that has been recently updated by a circuit similar to the proposed circuit in this paper. It should be noted that in this case, we need bulky DAC and ADC circuits that is far from the design ideal of compactness and low power consumption. A recently proposed approach is to utilise reverse-biased transistors to decrease the leakage currents and therefore increase the duration the weight value can be stored on the capacitor [3]. Although this is a nice approach for reducing the leakage in the circuit, it is not really useful for long-term plasticity experiments in the order of seconds.

4) The other point that should be taken into account when designing any analog VLSI circuit, including neuromorphic circuits, is the process variation associated with VLSI technology. As the proposed design uses the voltage applied to the gate of transistors to tune the required parameters of the model and reaches the targeted behavior to mimic the experiments, it is sensitive to the variation of bias voltages and therefore susceptible to process variation. Although these bias voltages can be generated using an off/on chip bias generator [23], the circuit was modified to alleviate the effect of process variation. The modified circuit is demonstrated in Fig. 5. In this circuit, the tuned currents in any of the current mirror transistors will set one of the TSTDP rule parameters (see Eq. 2). These parameters can be adjusted by means of a single current source, I_{bias} , and adjusting the aspect ratio of the respective transistors. For instance, the width of M5 will tune the pairing potentiation time constant, τ_+ , with respect to the value of the circuit main bias current, I_{bias} . An NMSE = 2.04 is achieved using transistor sizes shown in Fig. 5. Although the mismatch among these transistors will result to some drop in the circuit performance, our simulations (not presented here due to the lack of space) show, it is more stable than the previous design using bias voltages (Fig. 1).

In addition, there are other approaches that can be utilised in order to either decrease the effect of process variations like the design technique employed in [24] in neuromorphic modelling of ion channel and ionic dynamics in large scale neuronal networks, or to compensate for the variations caused by the fabrication process with a post-fabrication calibration technique [2]. Although the latter is simpler and does not need extra circuitry for alleviating the effect of process variation, it is not applicable for large scale neural networks. On the other hand, the former causes an increase in the complexity of the



Fig. 5. Minimal TSTDP circuit modified from the initial design presented in Fig. 1 in order to gain more stability against process variation. The used bias current is $I_{\rm bias}$ =1.5 nA. The transistor lengths are all 0.7 μ m and widths are all $3w_{\rm min}$ =1.05 μ m, unless shown beside transistors.

designed circuit that results in an inefficient realisation of large scale networks. Hence, a trade off between design complexity, and accuracy should be considered. As a next step for this research, we also plan to compare both mentioned approaches for tackling process variations in the proposed design.

VI. CONCLUSION

A novel compact VLSI design for pair, triplet and quadruplet STDP is introduced. Simulation results show that the proposed circuit can reproduce behavior found in some biological experiments including pairing, triplet, and quadruplet experiments in the hippocampus. The presented circuit consists of a fewer number of transistors compared to many of its pairbased STDP counterparts, and all previous TSTDP circuits. This can lead to a compact and low power implementation of the proposed circuit that makes it promising for use in large scale spiking Neural Networks with the synapses with increased abilities.

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