Invited Paper

GaAs for Optical Smart Sensors

D. Abbott

Centre for High Performance Integrated Systems and Technologies (CHiPTec)
The University of Adelaide, SA 5005, Australia
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ABSTRACT

A number of physical and optoelectronic properties of GaAs make it a highly suitable medium for optical smart sensors. In this paper, these properties are discussed with a view to smart image sensors (a) in a stand-alone context and (b) in the context of spatial light modulators (SLMs).

Keywords: GaAs, Optical Smart Sensors, SLMs

1. INTRODUCTION

The motivation to explore smart sensors in GaAs technology arises from the fact that (a) the optical absorption coefficients in GaAs are such that light is absorbed 10 times closer to the surface, than in silicon, resulting in more efficient photocollection and tighter control over optical overload (blooming)[1] (b) the diffusion lengths in SI GaAs are over an order of magnitude shorter than in silicon, resulting in improved spatial resolution, showing promise for HDTV applications[2] (c) GaAs has superior dark current characteristics, as evidenced by the successful realisation room temperature GaAs X-ray detectors[3] and (d) there is promise of integration of high-speed processing (eg. image compression) on the same chip as the sensor.

This paper demonstrates the superiority of GaAs in all areas over silicon, but reveals that shot noise degradation is the main area of weakness for MESFET technology. However, newly emerging GaAs technologies such as HIGFETs,[11] anisotype FETs[10] and MOS-GaAs[12] are discussed, showing promising results.

2. GALLIUM ARSENIDE SMART IMAGE SENSORS

In this context, the 'smart sensor' paradigm implies the integration of processing circuitry (eg. for image compression) with the image sensor. The superior power-delay product of GaAs becomes ideal for such high-speed processing in real-time. Such integration rules out the possibility of using a CCD process – CCD technology cannot support conventional digital circuits. Therefore, such a GaAs image sensor must use a standard or near-standard VLSI GaAs technology. The type of imager in this technology uses an XY addressable array of transistors as shown in Fig. 1.

There are two methods of readout: (a) charge sensing and (b) voltage sensing. In a voltage sensing approach, signal charge is converted to a voltage at each pixel node. As the conversion capacitance at each pixel is small, this results in reduced kTC noise and hence improved dynamic range. However, the downside is that capacitor and source follower mismatching between pixels lead to high fixed pattern noise (fpn).

In the charge sensing approach, this source of fpn is eliminated by dumping the charge from each pixel on to the output node. In this way, charge-to-voltage conversion occurs at the final output – thus only one source follower is required at the output. Due to the architecture of the array a large output node capacitance is unavoidable, leading to increased kTC noise and reduced dynamic range.

However, due to the semi-insulating (SI) substrate, capacitances are reduced making the *charge sensing* XY array, in Fig. 1, the best choice in GaAs.

Further advantages with the shift to GaAs, as outlined in Sec. 1, include shallow optical absorption lengths and small carrier diffusion lengths. The superiority of the GaAs over silicon, in terms of absorption length, is illustrated in Fig. 2. As can be seen, light is absorbed about ten times closer to the surface in GaAs than in silicon. This implies tighter control over blooming, increased photocollection efficiency and greater spatial resolution.

Email: dabbott@eleceng.adelaide.edu.au; Telephone: +61-8-8303-5748; Fax: +61-8-8303-4360

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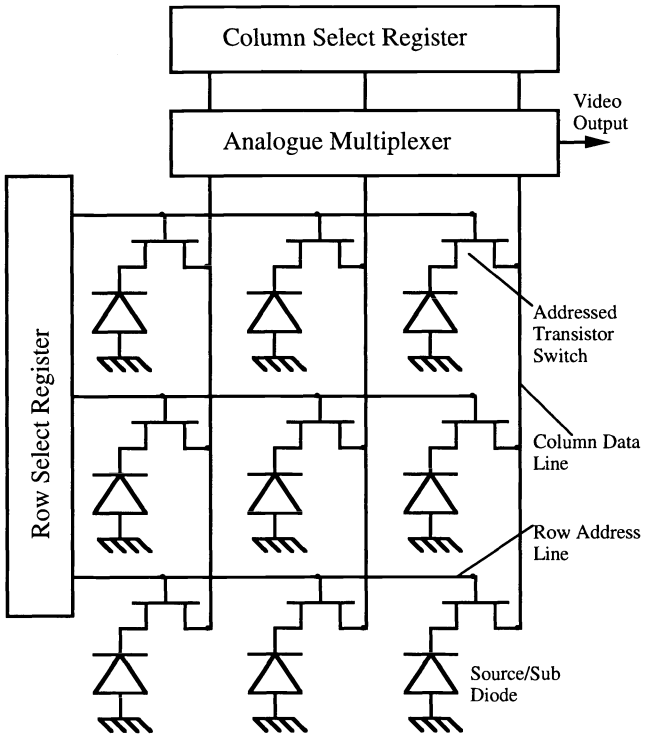

Figure 1. XY Array imager architecture – charge sensing approach.

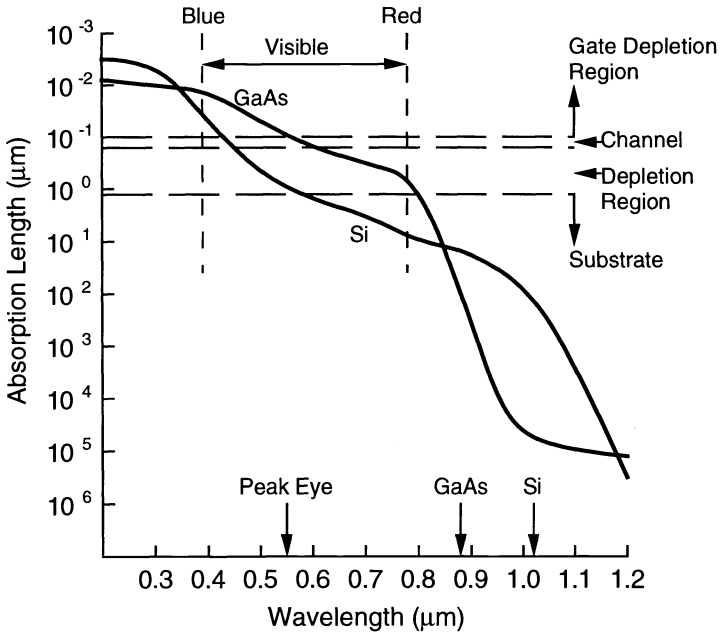

Figure 2. GaAs v. silicon absorption length

The graph in Fig. 3 represents MESFET drain current response to XY position of a focussed laser beam on the surface of the transistor. It has been shown that under conditions of photovoltaic self-biasing,[2] the peaks in Fig. 3 lie exactly on the substrate/transistor boundary. Thus from the decay of the peaks into the substrate, it can be estimated that the carrier diffusion length is $<10\mu$m. This is much smaller than in CMOS where minority carrier diffusion lengths are in the 200-400μm range.

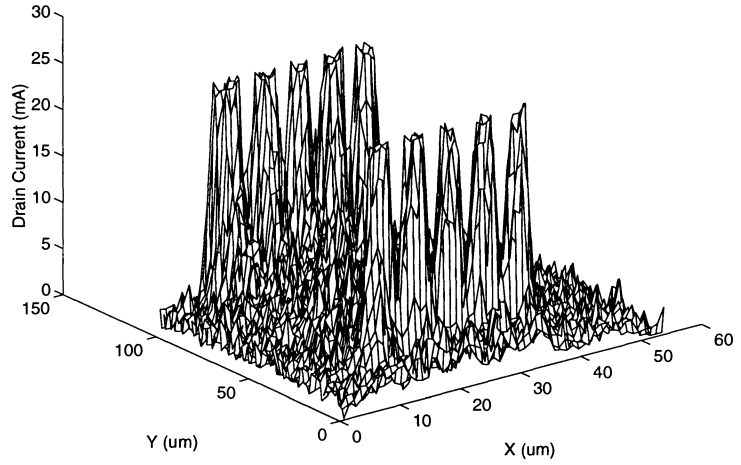

Figure 3. Diffusion length measurement.

The implication of short diffusion length together with shallow absortion length is excellent spatial resolution for HDTV applications.[4] However, in practice, for silicon imagers, good spatial resolution is obtained at the expense of responsivity, by use of a thin epi layer. Therefore in practice, with GaAs, improved spatial resolution translates into improved responsivity over silicon, as the epitaxial approach can be dispensed with. This improved responsivity impacts not only on GaAs HDTV sensors, but on the GaAs smart sensors discussed herein.

3. SPATIAL LIGHT MODULATORS

SLMs are basically 2-D arrays that output image patterns reflectively (eg. via Ferroelectric Liquid Crystal or FLC) or directly (eg. a micro-array of LEDs or a VCSEL). These light patterns can be modulated either electrically (ie. an electrically addressable SLM or EASLM) or optically (ie. an optically addressable SLM or OASLM). Thus these devices essentially perform optical spatial filtering functions.

The EASLM can consist of an array of smart pixels sandwiched to either a LED or FLC display device. Further to this, the OASLM utilises a smart image sensor for optical addressing.

GaAs offers two significant possibilities: an LED/GaAs, Fig. 4, or an FLC/GaAs, Fig. 5, architecture. The advantages of GaAs are numerous. Firstly the larger absorption coefficient in GaAs leads to improved optical addressing characteristics.[1] Secondly, FLC technology is sensitive to surface planarity and wafer warp as little as 1 μm – GaAs offers excellent planarity due to the absence of field oxide steps and a warp of less than 0.5 μm has been achieved. In silicon, for typical devices, the warp is greater than 1 μm leading to critical non-uniformities in the FLC layer. GaAs also offers the potential to move away from LC technology altogether as LED arrays can be monolithically integrated.[5] With the emergence of low-power complementary GaAs, already available with VLSI maturity, the traditional problems with power dissipation are no longer of concern. Other advantages of GaAs include no latchup, fewer masking layers (simpler) and existing techniques for through-substrate-vias (this has implications for future 3-D mounted SLMs).

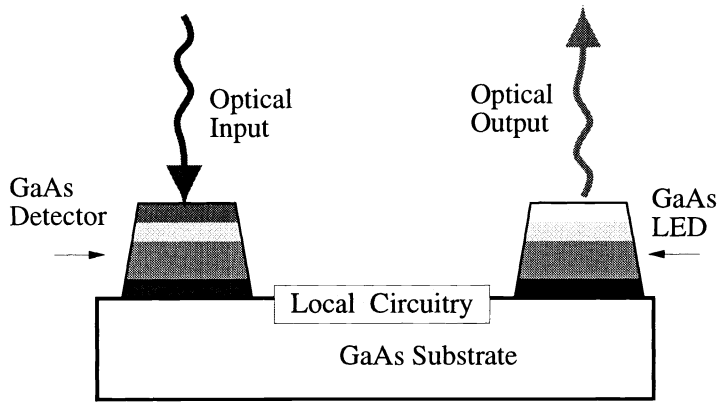

Figure 4. A LED/GaAs smart pixel

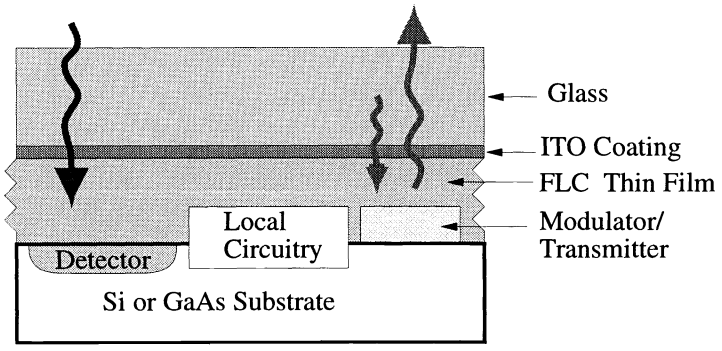

Figure 5. A FLC/Si or FLC/GaAs smart pixel

GaAs has a number of advantages with respect to the smart pixel concept. Firstly in order to enable optical input, a 2D image sensor must be vertically stacked with parallel connections to the display device using, for example, flip-chip techniques. Fortunately, the GaAs crystal has excellent crystal properties enabling etching of through-substrate-vias with relative ease and this is a known technique in GaAs MMICs that use vertical connections to a backside groundplane. Smart pixel functions can be embedded either in the sensor or display device or both.

Another feature of GaAs is that wafer warp across a chip is superior to silicon and <1 μm. Silicon has the disadvantage that a warp >1 μm degrades the performance of the FLC display, creating a deleterious dispersion in phase across the area of the device. The digital GaAs process is also intrinsically more planar than CMOS (eg. no field oxide) and therefore variations in FLC thickness are further reduced.

Due to the improved power-delay product of GaAs over silicon, either throughput rate can be increased or, for the same speed, power dissipation is reduced. This becomes important for stacked devices as greater care over thermal management is required.

4. NOISE PERFORMANCE

In practice, flicker and kTC noise are removed by correlated double sampling (CDS)[6] or delayed double sampling (DDS),[7] for example, and thus we concentrate on the thermal and shot noise analysis.

The curves in Figs. 6 & 7, were obtained using the procedure described in.[9] We see from Fig. 7, that shot noise dominates the noise of the GaAs imager output circuit. Unfortunately it is impossible to remove shot noise by correlated double sampling. This means that the circuit cannot be optimised for this MESFET technology. Hence to realise a proof-of-concept imager, in the short term, two options are available: (a) use off-chip output circuitry or (b) use ammonium sulphide, $(NH_4)_2S$, annealed MESFETs – which is is reported as reducing gate leakage currents by 3 orders of magnitude.[8]

Option (a) would add 1-2 pF of parasitic capacitance to the output node, but this total capacitance would still be less than in the case of silicon. With option (b) there is a question over the stability of sulphide treatments in GaAs. In the short term, (a) provides the simplest solution for producing a proof-of-concept demonstrator.

In the longer term, two emerging GaAs technologies are promising: the HIGFET and the anisotype FET. The HIGFET[10] uses a semi-insulating AlGaAs layer in the gate to reduce leakage currents – the middle shot noise curve in Fig. 7 represents this case. The anisotype FET[11] uses a graded semiconductor InGaAs/GaAs layer in the gate, producing yet a further improvement in gate leakage – the shot noise for this case is the lowest dashed curve in Fig. 7.

Recently Lucent have announced a true MOS-GaAs,[12] using a mixture of gallium oxide and gadolinium oxide $Ga_2O_3(Gd_2O_3)$. If oxide stability and high integration levels are eventually proven, this will be the ideal medium for the proposed sensor.

5. CONCLUSIONS

For smart image sensors GaAs is promising in its ability to integrate high-speed processing circuitry – recent developments in complementary GaAs makes this prospect more attractive. GaAs also offers increased spatial resolution and responsivity, which can be traded against each other. In terms of SLMs the process planarity and wafer warp characteristics of GaAs make it attractive for the FLC approach. For the LED approach, GaAs is the natural medium for monolithic integration of LEDs. The major stumbling block to GaAs smart sensors appears to be in the poor shot noise performance of the output circuit, due to gate leakages. We have shown, however, that an adequate proof-of-concept device can be produced with an off-chip output circuit. In the meantime, rapid developments in the technology of semi-insulating and insulating gates for GaAs transistors are very promising and will allow complete monolithic GaAs smart image sensors in the near future.

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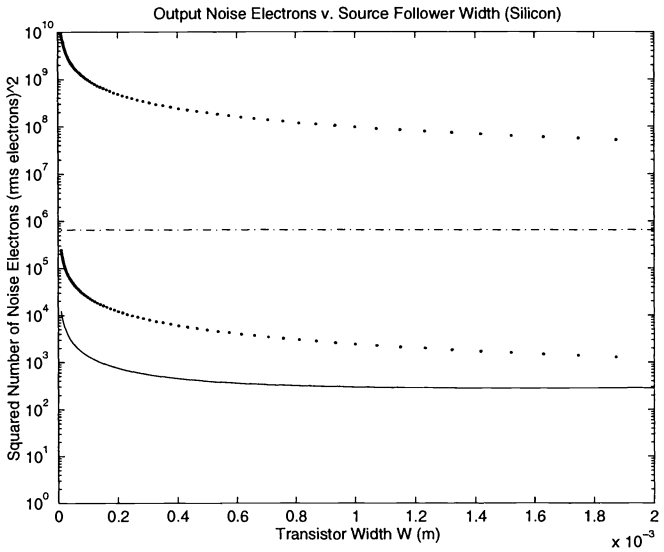

Figure 6. Noise sources (silicon). Solid line: thermal noise. Chained line: kTC noise. Dotted lines: maximum minimum flicker noise (frequency dependent).

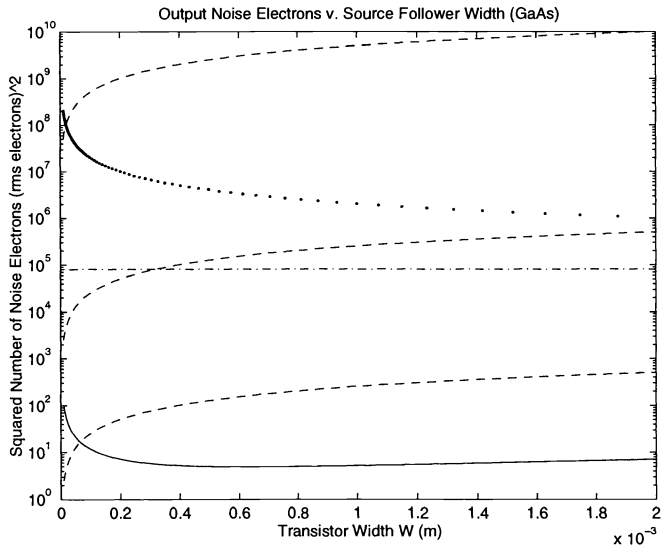

Figure 7. Noise sources (GaAs). Solid line: thermal noise. Chained line: kTC noise. Dotted line: maximum flicker noise. Dashed lines: shot noise (upper curve, MESFET, $I_g = 2 \times 10^{-8}$A/m; middle curve, HIGFET, $I_g = 10^{-12}$A/m; lower curve, anisotype FET, $I_g = 2 \times 10^{-15}$A/m.

REFERENCES

1. D. Abbott, *et al,* "A new VLSI smart sensor for collision avoidance inspired by insect vision," *Proc. SPIE,* **2344**, pp. 105-115, Boston, 2-4 Nov., 1994.
2. D. Abbott *et al,* "Photovoltaic edge-effect in planar GaAs MESFETs," *SPIE 17th Congress of the ICO,* **2778**, 2, pp. 955-996, Taejon, Korea, Aug. 19-23, 1996.
3. D.S. McGregor *et al,* "Development of bulk GaAs radiation detectors," *IEEE Nuc. Sci.,* **39,** 5, pp. 1226-1236, 1992.
4. D. Abbott *el al,* "Improved image sensor for HDTV," *Proc. IREE 14th Micro. Conf. (Micro'97),* pp. 191-194, Melbourne, Sep. 29-Oct. 1st, 1997.
5. A.C. Grot and D. Psaltis, "Large Scale integration of LEDs and GaAs circuits fabricated through MOSIS," *Tech. Digest,* Optical Computing 94, MA2/3-4, 1994.
6. D.F. Barbe, *Proc. IEEE,* **63,** pp. 38-67, 1975.
7. M. Obho and S. Yamamoto, *ICCE,* pp. 58-59, Chicago, June 8-10, 1988.
8. J.A. Cooper, *Advances in Electronics and Electron Physics,* **86,** pp. 1-79, 1993.
9. D. Abbott *et al,* "Output circuit noise analysis of the XY array imager," *14th Int. Conf. on Noise in Physical Sys. and 1/f fluctuations (ICNF'97),* Leuven, Belgium, 14-18th July, pp. 482-487, 1997.
10. J.K. Abrokwah, "A manufacturable high-speed low-power complementary GaAs Process," *Int. Conf. Solid State Devices and Materials,* pp. 592-594, Yokohama, Aug. 23-26, 1994.
11. J.K. Abrokwah, "Anisotype-gate self-aligned p-channel heterostructure field-effect transistors," *IEEE Trans. E.D.,* **40,** 2, pp. 278-284, 1993.
12. F. Ren *el al, IEDM Tech. Dig.,* p. 943, 1996.