Novel Extension of neu-MOS Techniques to neu-GaAs

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ABSTRACT

The neu-MOS transistor, recently discovered by Shibata and Ohmi in 1991,[1] uses capacitively coupled inputs onto a floating gate. Neu-MOS enables the design of conventional analog and digital integrated circuits with a significant reduction in transistor count.[2,3] Furthermore, neu-MOS circuit characteristics are relatively insensitive to transistor parameter variations inherent in all MOS fabrication processes. Neu-MOS circuit characteristics depend primarily on the floating gate coupling capacitor ratios. It is also thought that this enhancement in the functionality of the transistor, ie. at the most elemental level in circuits, introduces a degree of flexibility which may lead to the realisation of intelligent functions at a system level.[4] This paper extends the neu-MOS paradigm to complementary gallium arsenide based on HIGFET transistors. The design and HSPICE simulation results of a neu-GaAs ripple carry adder are presented, demonstrating the potential for very significant transistor count, area and power dissipation reduction through the use of neu-GaAs in VLSI design. Due to the proprietary nature of complementary GaAs data and SPICE parameters, the simulation results are based on a representative composite perameter set derived from a number of complementary GaAs processes. Preliminary simulations indicate a factor of 4 reduction in gate count, and a factor of over 50 in power dissipation over conventional complementary GaAs. Small gate leakage is shown to be useful in eliminating unwanted charge buildup on the floating gate.

Keywords: neuron MOS, GaAs, low power techniques

1. INTRODUCTION

Complementary GaAs has a number of highly desirable properties for low-power, high-speed digital and mixed RF/digital applications. These include low voltage operation (0.9V to 1.5V), very low static power dissipation using CMOS-like designs and significantly higher operating speeds than CMOS.

The neuron-MOS transistor (neu-MOS for short) was originally developed at Tohoku University in 1991.[1] The structure of a neu-MOS transistor is identical to an ordinary MOS transistor, but with a number of additional inputs capacitively coupled onto a floating gate, as shown in Figure 1. The floating gate potential is a weighted sum of the inputs, the weightings being determined by coupling capacitor ratios.

The use of neu-MOS transistors provides additional functionality which allows, for example, the design of a full adder cell with only 8 transistors as compared to 28 in CMOS and an area of 55% of the CMOS design.[5]

The goal of this article is to extend the neu-MOS paradigm to the complementary GaAs technology. In particular, we demonstrate the suitability of HIGFET transistors for application to neu-GaAs,[6] present a basic neu-GaAs circuit structure and the simulation results of a neu-GaAs 4 bit ripple carry adder.

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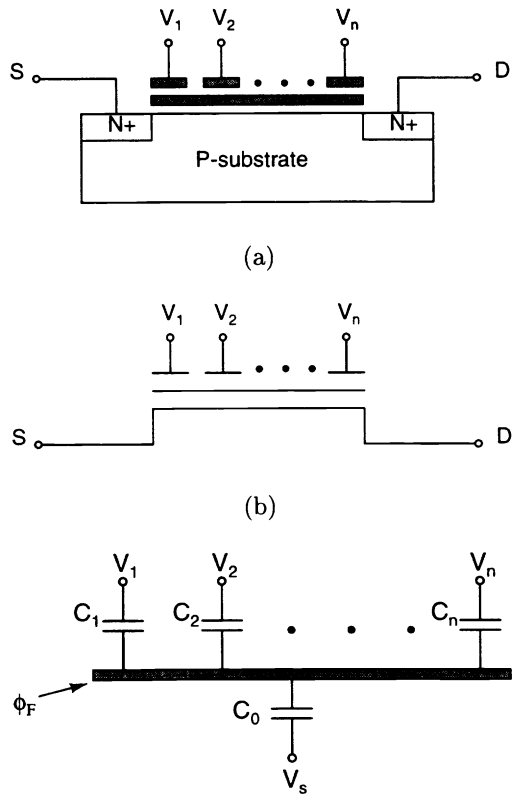


Figure 1. (a) The structure of an n-type neu-MOS transistor, (b) its electronic symbol and (c) the capacitance model

2. NEU-GAAS BASIC STRUCTURE

The neu-GaAs transistor is shown in Figure 1. The analysis of this structure is identical to that of the neu-MOS transistor given in,[1] and the floating gate potential is given by

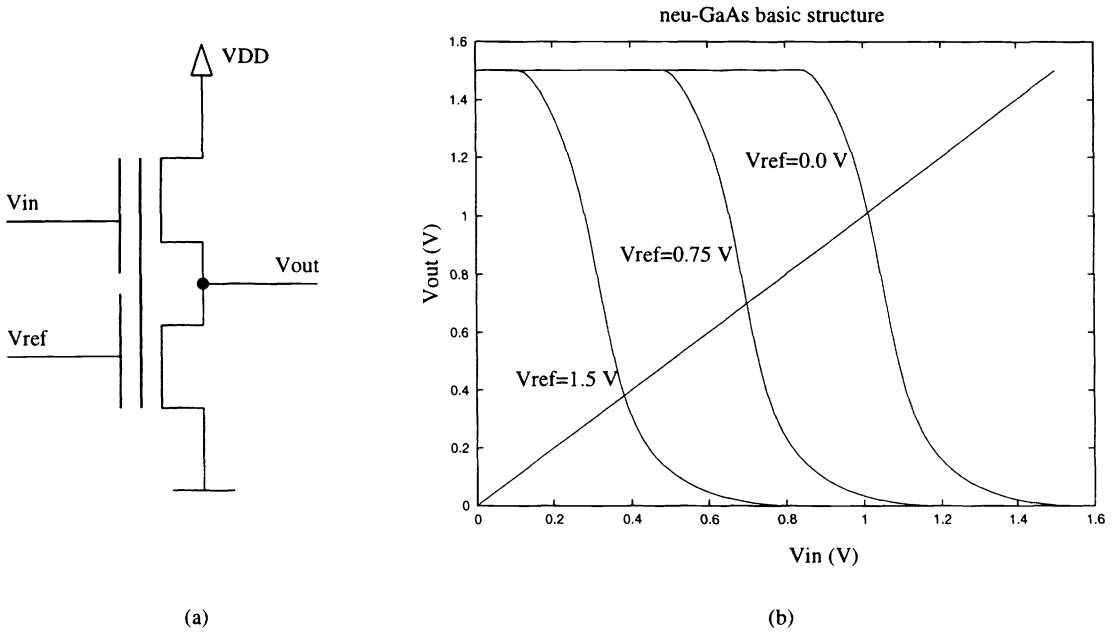
$$\phi_F = \frac{C_1V_1 + C_2V_2 + ... + C_NV_N}{C_T}$$

where C_T is the sum of the coupling capacitors C_1 to C_n and C_0. C_0 is the sum of all parasitic capacitances from the floating gate to the substrate, including the floating gate to source and drain capacitances.

A basic variable threshold neu-GaAs inverter structure is shown in Figure 2. This neu-GaAs inverter is a fundamental building block in digital neu-GaAs design and is similar to an ordinary CMOS like ratioless inverter consisting of a p-type GaAs pull-up and an n-type pull-down transistor. The gates of the two transistors are connected and two inputs which are capacitively coupled to this floating gate are added. When the floating gate potential exceeds the inverter threshold, the inverter output becomes low and vice versa. By using two inputs, one which we wish to invert, V_{in}, and one as a threshold control, V_{ref}, the effective neu-GaAs inverter threshold *as seen from the input* V_{in} can be made variable. The simulation results for three values of V_{ref} are shown in Figure 2.

3. CHOICE OF GAAS TECHNOLOGY

The realisation of neu-GaAs circuits requires that the floating gate voltage remain stable for periods of time depending on the clock frequency being used. This means that a low gate leakage current is needed. The HIGFET uses a semi



(a) (b)

Figure 2. Basic neu-GaAs Inverter Structure

insulating AlGaAs layer to reduce gate leakage currents and it appears, at least in the short term, as the most viable option for complementary neu-GaAs applications.

The simulations which have been performed are based on a realistic composite SPICE parameter set derived from a number of complementary GaAs processes, including Honeywell,[7] Sandia,[8] Univ. Lille[9] and MIT.[10] It must also be mentioned that the neu-GaAs simulation results are somewhat hypothetical in that convenient capacitors, such as polysilicon 1 to polysilicon 2 in CMOS, do not exist in complementary GaAs. The added benefits of neu-GaAs as well as its possible integration into mixed RF/digital applications should provide strong justification for the inclusion of a special capacitive (metal-insulator-metal) layer to existing HIGFET processes.

4. A 4-BIT NEU-GAAS RIPPLE CARRY ADDER

A 4-b RCA was chosen as a simple circuit to demonstrate the feasibility of circuit design using neu-GaAs. Ripple carry adders have relatively low power dissipation, but the delay for computing the final carry depends on the number of bits to be added because the carry propagates successively from the first stage to the last. The basic neu-GaAs full-adder (FA) is implemented based on the following expressions obtained from the truth table for addition:

$$c_i = 1 \iff a_i + b_i + c_{i-1} \geq 2$$
$$s_i = 1 \iff a_i + b_i + c_{i-1} - 2c_i \geq 1$$

where a_i and b_i are the two bits at the i^{th} position and c_i is the carry generated at the i^{th} position.

As there are no negative voltages in the circuit (there is only a 1.5 V supply), $-2c_{i+1}$ must be converted into $2(\overline{c_{i+1}} - 1)$ and hence:

$$c_i = 1 \iff a_i + b_i + c_{i-1} \geq 2$$
$$s_i = 1 \iff a_i + b_i + c_{i-1} + 2\overline{c_i} \geq 3$$

It should be noted that in order to compute s_i, $\overline{c_i}$ has to be pre-computed. The neu-GaAs realisation of the two inequality expressions for c_i and s_i is shown on the right hand side of Figure 3. Figure 3 also compares the full adder cell design in both conventional complementary GaAs and neu-GaAs and shows a signficant transistor count reduction in the neu-GaAs design.

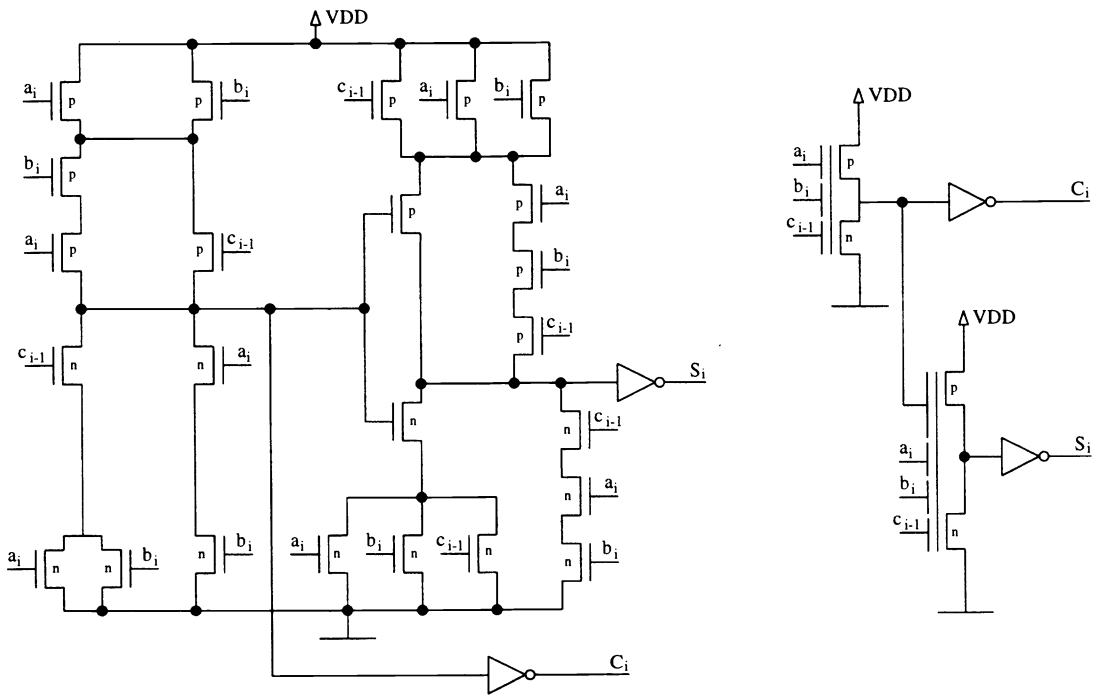


Figure 3. Conventional GaAs and neu-GaAs Full Adder Designs

5. SIMULATION RESULTS FOR THE NEU-GAAS RCA

The technique used to simulate the RCA structure using HSPICE is as follows. The two input words were set to (a_3 a_2 a_1 a_0) = (0 0 0 0) and (b_3 b_2 b_1 b_0) = (1 1 1 1) as shown in Figure 4. The c_{in} was switched from 0 to 1.5 V at a frequency of 200 MHz. This causes the output carry c_3 to switch when the input carry c_{in} propagates through the four bit slices.

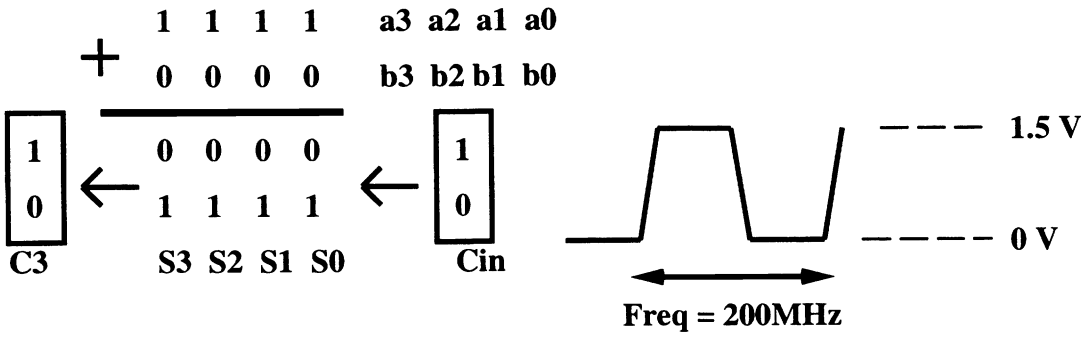


Figure 4. Switching of c_3 during the HSPICE simulation

Figure 5 below shows the simulation results for a single full adder while c_{in} is switched. The graph on the right in Figure 5 shows that there is no degradation of the c_{out} output even when c_{in} is maintained high for an extended period of time (25ns).

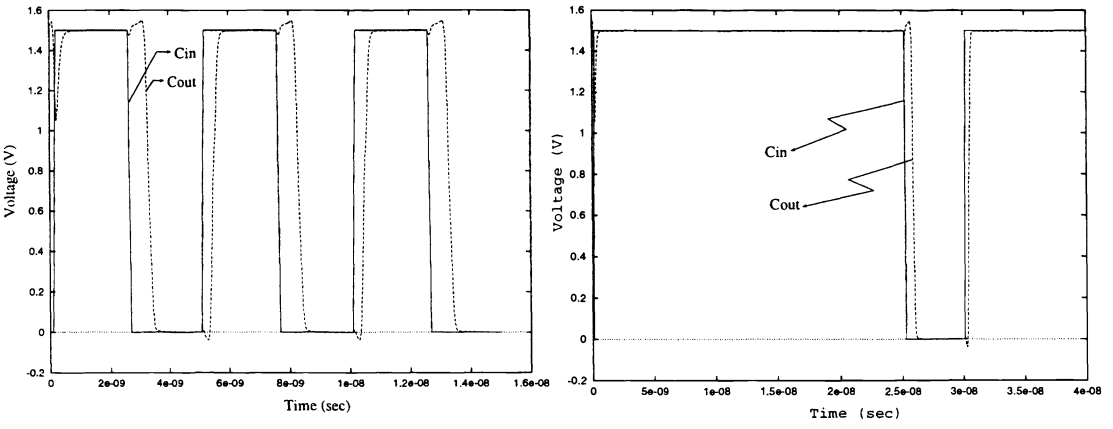


Figure 5. C_{out} and C_{in} Simulation for a neu-GaAs Full Adder

The propagation delay and power dissipation of the carry signal through a single full adder operating at 200MHz were then measured as a function of the supply voltage. The results are plotted in Figure 6.

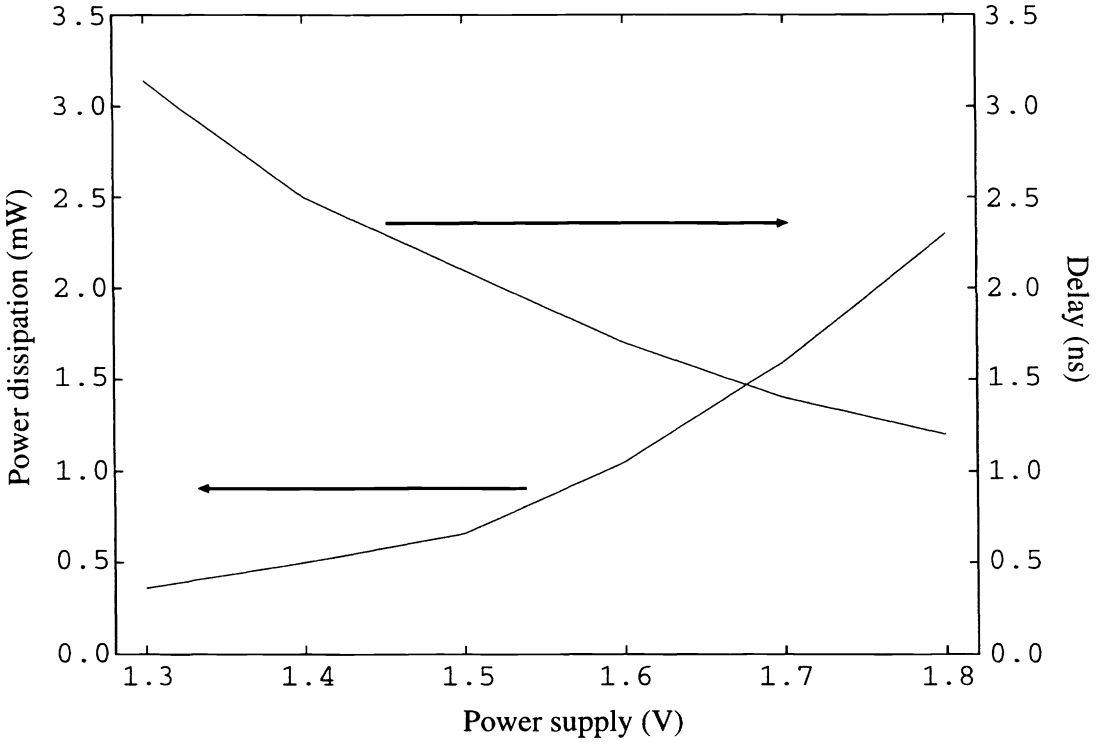


Figure 6. Delay and Power Dissipation vs Supply Voltage for a 1-bit neu-GaAs RCA

6. EFFECTS OF GATE LEAKAGE CURRENT

Net charge present on the floating gate after the fabrication process in neu-MOS transistors causes fluctuations in transistor inversion threshold voltage.[1] The residual charge on the floating gate can be removed by irradiating the neu-MOS structure with ultraviolet (UV) light. This, however, is an additional step necessary in the construction of neu-MOS circuits.

The proposed neu-GaAs transistor structure does not require a specific procedure to remove residual floating gate charge. The reason for this is the presence of a small gate leakage current. This is of the order of a few nA.

7. CONCLUSION

A complementary neuron GaAs structure has been proposed and a ripple carry adder based on this structure has been simulated. It has been shown that by using neu-GaAs, a very significant reduction in the number of transistors is attainable over conventional complementary GaAs adder designs.

The use of neu-GaAs techniques in HIGFET transistor designs promises to give VLSI designers more freedom in designs where area, delay and power dissipation are critical and hence provides a step forward towards ULSI integration density.

ACKNOWLEDGMENTS

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REFERENCES

1. T. Shibata and T. Ohmi, "An intelligent MOS transistor featuring gate-level weighted sum and threshold operations," in *International Electron Devices Meeting, Technical Digest*, IEEE, (New York, NY, USA), Dec 1991.
2. L. S. Y. Wong, C. Y. Kwok, and R. G. A., "0.9 V 5 MS/S CMOS D/A converter with multiple-input floating-gate MOS," in *Proc. of the 1997 IEEE Custom Integrated Circuits Conference*, IEEE, May 1997.
3. B. Gonzalez, D. Abbott, Al-Sarawi, A. Hernandez, J. Garcia, and J. Lopez, "Efficient transistor count reduction for a low power GaAs A/D converter," in *Proceedings XIII Design of Circuits and Integrated Systems conference (DCIS'98)*, pp. 62–66, (Madrid, Spain), November 1998.
4. T. Ohmi and T. Shibata, "Intelligence implementation on silicon based on four-terminal device electronics," in *Proc. of 20th Int. Conf. on Microelectronics*, vol. 1, pp. 11–18, September 1995.
5. K. Hirose and H. Yasuura, "A comparison of parallel multipliers with neuron MOS and CMOS technologies," in *Proceedings of IEEE Asia Pacific Conference on Circuits and Systems 96*, pp. 488–491, IEEE, November 1996.
6. D. Abbott, S. Al-sarawi, B. Gonzalez, J. Lopez, J. Austin-Crowe, and K. Eshraghian, "Neu-MOS (MOS) circuits for smart sensors and an extension to a novel neu-GaAs (GaAs) paradigm," in *IEEE ICECS98*, vol. 3, pp. 379–404, (Lisbon), Sept 1998.
7. D. Fulkerson, S. Baier, J. Nohava, and R. Hochhalter, "Complementary heterostructure FET technology for low power, high speed, digital applications," *Solid State Electronics* **39**(4), pp. 461–469, 1996.
8. A. Baca, J. Zolper, D. Dubbert, V. Hietala, L. Sloan, R. Shul, M. Sherwin, and M. Hafich, "Complemetary HFET technology for wireless digital and microwave applications," in *Proc. of the Symposium on High Speed III-V Electronics for Wireless Applications and the 25th State of the Art Program on Compound Semiconductors*,
9. J. Thiery, H. Fawaz, N. Bourzgui, L. Nuyen, and G. Salmer, "Temperature dependence of pseudomorphic complementary HIGFET devices electrical characteristics," in *Proc. of the 23rd Inter. Symposium on Compound Semiconductors*, Shur and Suris, eds., pp. 523–526, IOP Publishing, (UK), 1997.
10. C. Chen, L. Mahoney, K. Nichols, and E. Brown, "Self-aligned complementary GaAs MISFETs using a low-temperature-grown GaAs gate insulator," *Electronics Letters* **32**(4), pp. 407–409, 1996.