A High Frequency Divider in 0.18 um SiGe BiCMOS Technology

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ABSTRACT

High speed frequency dividers are critical parts of frequency synthesisers in wireless systems. These dividers allow the output frequency from a voltage controlled oscillator to be compared with a much lower external reference frequency that is commonly used in these synthesisers. Common trade-offs in high frequency dividers are speed of division, power consumption, real estate area, and output signal dynamic range. In this paper we demonstrate the design of a high frequency, low power divider in 0.18 μm SiGe BiCMOS technology. Three dividers are presented, which are a regenerative divider, a master-slave divider, and a combination of regenerative and master-slave dividers to perform a divide-by-8 chain. The dividers are used as part of a 60 GHz frequency synthesizer. The simulation results are in agreement with measured performance of the regenerative divider. At 48 GHz the divider consumes 18 mW from a 1.8 V supply voltage. The master-slave divider operates up to 36 GHz from a very low supply voltage, 1.8 V. The divide-by-8 operates successfully from 40 GHz to 50 GHz.

Keywords: regenerative divider, mixer, master-slave, emitter-coupled logic, 60 GHz, frequency synthesizer

1. INTRODUCTION

Recently, the 60 GHz band has emerged as a frequency region of great interest in RF wireless communication. This high frequency band presents a considerable challenge in the design of RF transceivers including the frequency synthesizer. A phase-locked loop is commonly used building block for a frequency synthesizer. The phase-locked loop locks the high frequency output from a voltage-controlled oscillator (VCO) to a much lower frequency reference clock. In order to compare the two signals, a high speed frequency divider is required to decrease the VCO output frequency. The frequency dividers are a part of a frequency synthesizer for a 60 GHz RF receiver. The double-conversion receiver architecture is shown in Figure 1. Two local oscillators (LO) at 48 GHz and 12 GHz are used. The first LO is the output of a voltage-controlled oscillator (VCO), while the second LO is a quarter of the first LO. The second LO is obtained by dividing the first LO, utilizing two frequency dividers. The first divider is required to handle a 48 GHz signal from the VCO. This very high frequency signal could not be handled by static master-slave divider architecture. Hence, a dynamic divider is used. This regenerative dynamic divider is utilized to divide-by-2 the VCO signal, yielding 24 GHz from 48 GHz. The 24 GHz output from the regenerative divider is divided-by-2, utilizing a master-slave divider to obtain a 12 GHz signal. The 12 GHz signal, which is the second LO is fed to the mixers to downconvert the IF signal to baseband. Another master-slave divider is used after the second LO to produce a total of 8 divisions. A few more frequency dividers might be required before the signal goes to a phase frequency detector (PFD). However, only high frequency dividers are of concern in this paper.

Three frequency divider circuits are implemented, a regenerative divider, a master-slave divider, and a divide-by-8 chain. Section 2 details the circuit design. These circuits were fabricated in 0.18 μm SiGe BiCMOS

technology with $f_t = 155$ GHz. The regenerative divider operates up to 50 GHz and consumes only 18 mW at 1.8 V supply voltage. The master-slave divider operates from a supply voltage as low as 1.8 V. Section 3 provides experimental results.

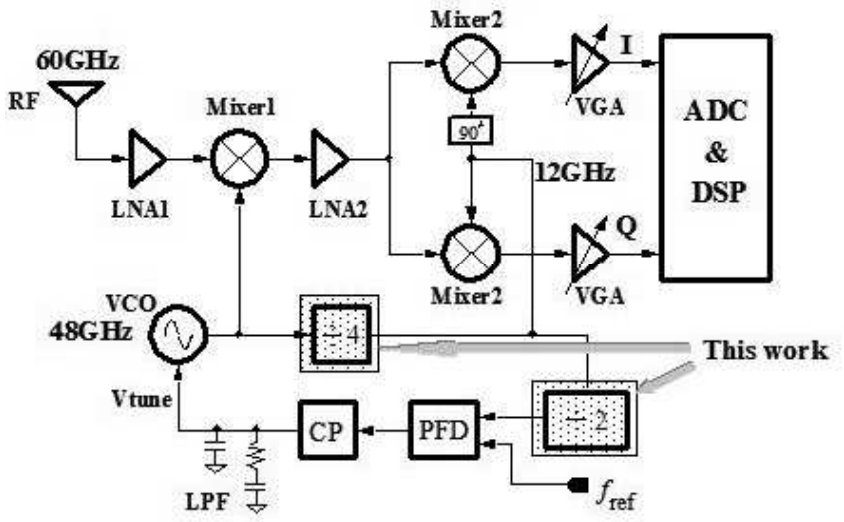


Figure 1. A 60 GHz receiver using a double-conversion architecture. By utilizing the 48 GHz first LO, a 60 GHz RF signal is translated to a 12 GHz IF. Then, the 12 GHz second LO converts the IF to baseband (ADC & DSP). The first LO is generated by a VCO, while the second LO is obtained after dividing the first LO by 4. The second LO provides a quadrature output. A PLL is used for the frequency synthesizer. Frequency dividers divide the VCO output before a phase frequency detector (PFD) compares the signal to a reference. Then a charge pump (CP) and a low pass filter (LPF) translate the errors into a voltage (V_{tune}) to control the VCO.

2. CIRCUIT IMPLEMENTATION

2.1. Regenerative Frequency Divider

The basic concept of a regenerative divider is to produce oscillation at half of the input frequency with the aid of a feedback network. The regenerative divider consists of a mixer and a loop filter as shown in Figure 2. The input signal at frequency f_{in} is mixed with the output signal at frequency $f_{in}/2$. The mixer generates the output at $f_{in}/2$ and also contains odd harmonics $3f_{in}/2$, $5f_{in}/2$ etc. These harmonics are filtered out by a band-pass filter. Thus, only $f_{in}/2$ is feed back to the mixer, second input. To obtain a stable half-frequency, the loop gain must be greater than unity[1,2] and the total loop phase must be within $\pm\pi/2$.[1] In addition, to ensure no spurious oscillation, the loop gain must be smaller than one when the input signal is absent.[3]

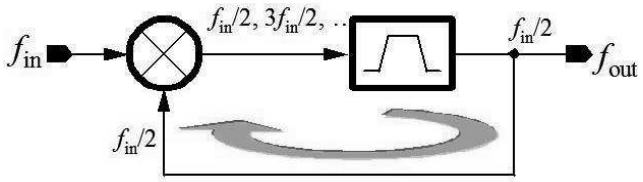


Figure 2. Regenerative frequency divider. The mixer generates the output at $f_{in}/2$, $3f_{in}/2$ etc. A band pass filter filtered the mixer output to obtain a signal at $f_{in}/2$.

An important part of the regenerative divider is the mixer. A Gilbert mixer is used with parallel load resistors and inductors as shown in Figure 3. The input signals applied to transistors Q1 and Q2 are amplified during

the mixing operation. The output is fed back to the top transistors (Q3, Q4, Q5 and Q6). This circuit does not include the band-pass filter because the divider output is maximum at half of the operating frequency.

Figure 4 shows the die micrograph of the fabricated regenerative divider. The circuit consumes 0.7 mm × 0.6 mm in area, including pads.

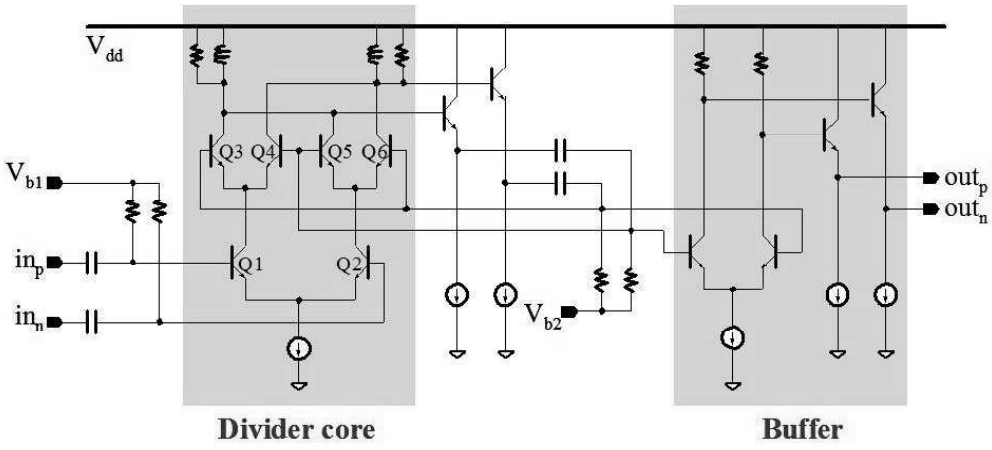


Figure 3. Regenerative divider schematic.

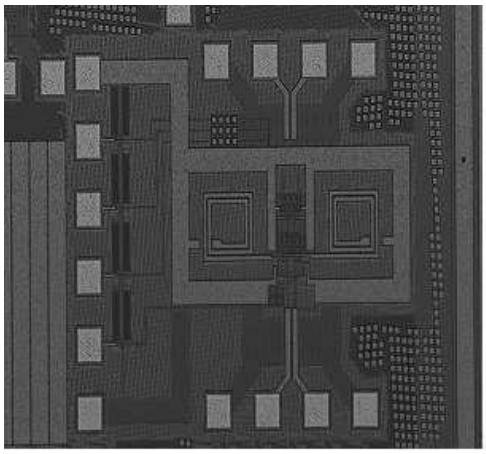


Figure 4. Die micrograph of the regenerative divider in 0.18 μm SiGe BiCMOS technology. The circuit area is 0.7 × 0.6 mm^2.

2.2. Master-Slave Frequency Divider

The master-slave frequency divider circuit is implemented using a conventional emitter-coupled logic (ECL) D flip-flop, as shown in Figure 5. The divider output is buffered before being used to drive other circuits. The output buffer consists of a pair of emitter followers and a differential amplifier. This circuit operates from a 1.8 V supply voltage.

The D flip-flop consists of two D latches. The output of first D latch must be able to drive the input of second D latch. Normally, emitter follower circuits are added between the D latches to provide voltage level shifting to drive the next stage.[4,5] However, with 1.8 V supply voltage, a voltage level shifter becomes complicated. The

proposed circuit design eliminates the emitter follower between the D latches. This was achieved by careful circuit design to enable the output level of the first D latch to drive second latch at appropriate level.

The layout is designed to be symmetrical to ensure the same delay for the differential signal. The track from input to output was designed to be as short as possible to reduce the propagation delay. The circuit consumes 0.6 mm × 0.6 mm area including the pads. Figure 6 shows the micrograph of the master-slave divider.

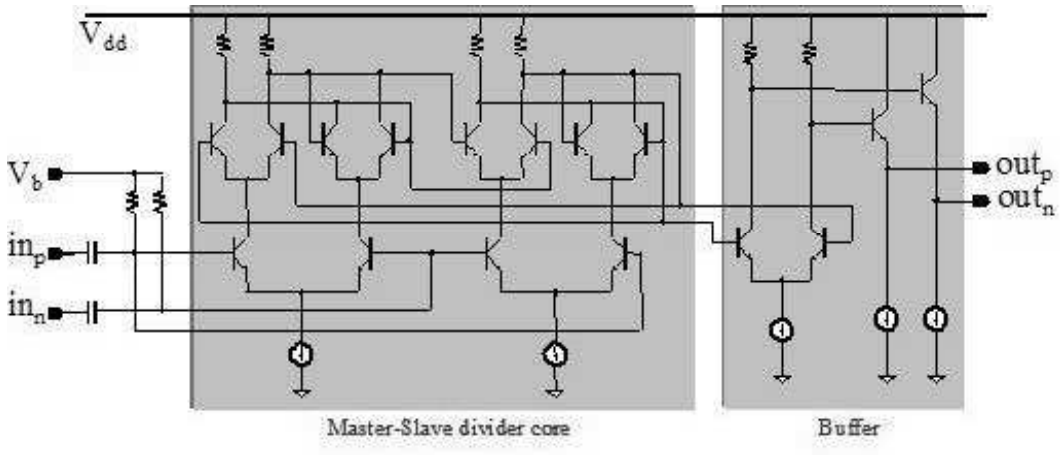


Figure 5. Master-slave divider schematic. The divider consists of two D latches. The output of the first latch is enabled to drive the second input latch. Hence, no voltage level shifter is required between the two latches.

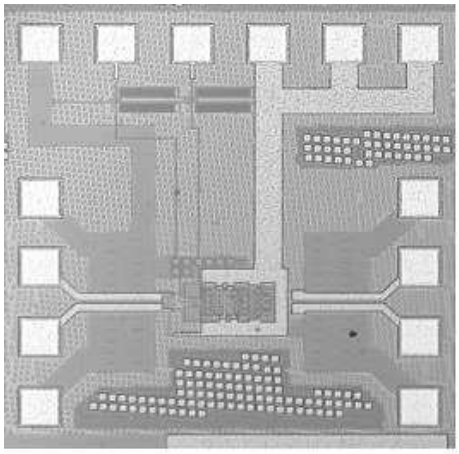


Figure 6. Die micrograph of the master-slave divider in 0.18 μm SiGe BiCMOS technology. The circuit area is 0.6 × 0.6 mm^2.

2.3. Divide-by-8 Chain

The divide-by-8 chain consists of a regenerative divider followed by two master-slave dividers as shown in Figure 7. The output of each stage should be able to drive the next stage. From the simulation, each stage output is estimated to generate more than 60 mV to enable to drive the next stage.

Figure 8 shows the die micrograph of the divide-by-8 chain. The circuit consumes 0.7 mm × 0.8 mm area including the pads. This is due to the fact that most of the master-slave divider test circuit is consumed by the test pads. Hence, the combined circuit resulted in a small area that is mainly dominated by the regenerative divider.

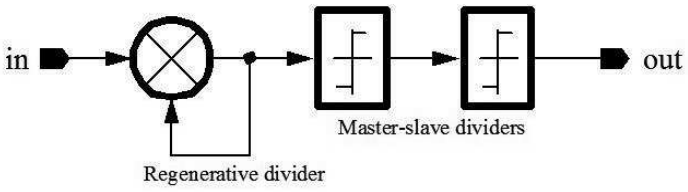


Figure 7. Divide-by-8 chain. This chain consists of three dividers, a regenerative divider and two master-slave dividers.

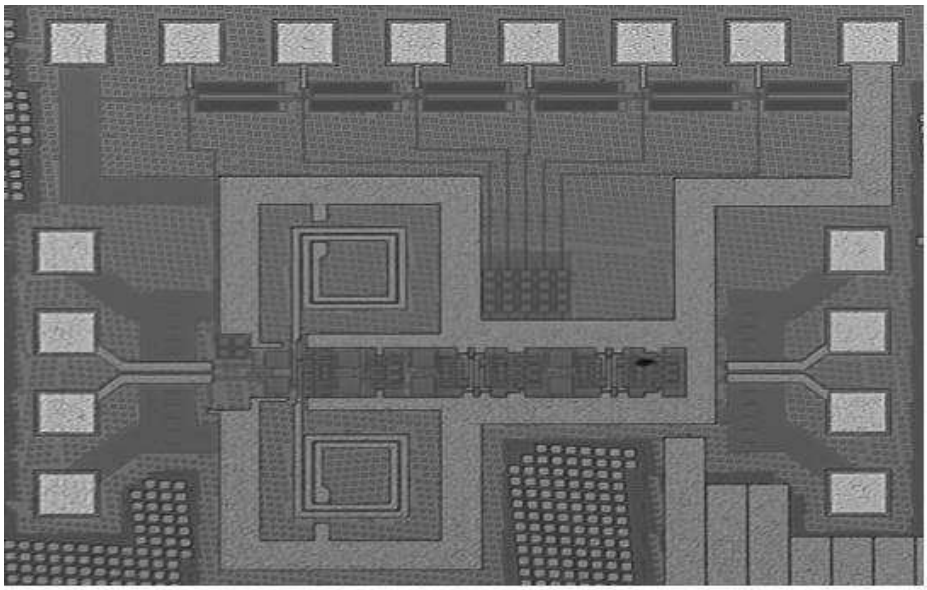


Figure 8. Die micrograph of the divide-by-8 chain in 0.18 μm SiGe BiCMOS technology. The circuit area is 0.7 $\times$ 0.8 mm^2.

3. EXPERIMENTAL RESULT

The circuits are tested by a pico-second probe with a single-ended input signal. Figure 9 shows the testing configuration for the divide-by-8 chain. External bias voltages are used for optimum circuit operation.

The regenerative frequency divider consumes only 18 mW from 1.8 V supply including the buffer. This circuit is tested using 40 GHz to 50 GHz input range. Figure 10 shows the output spectrum of the divider circuit for three different input frequencies, 46 GHz, 48 GHz and 50 GHz. The output frequency reading is shown on the middle left of each sub-figure, as 23 GHz, 24 GHz and 25 GHz, respectively. Table 1 gives the comparison between input frequency, power consumption and chip area of recently reported regenerative frequency divider.

For the master-slave divider, with 1.8 V supply, it consumes 54 mW including the buffer. The maximum operation frequency is 30 GHz. Figure 11 shows the output spectrum at 24 GHz input frequency. Table 2 gives the comparison between input frequency, power consumption, supply voltage and chip area of recently reported static frequency divider in SiGe.

For the divide-by-8 chain, it drains 65 mA from 1.8 V supply voltage. The circuit is tested from 40 GHz to 50 GHz input frequency with 1 GHz frequency steps. Figure 12 shows the output spectrum at six different input frequencies, 45 GHz, 46 GHz, 47 GHz, 48 GHz, 49 GHz and 50 GHz. The output frequency reading is shown on the middle left of each sub-figure, as 5.625 GHz, 5.75 GHz, 5.875 GHz, 6 GHz, 6.125 GHz, and 6.25 GHz, respectively.

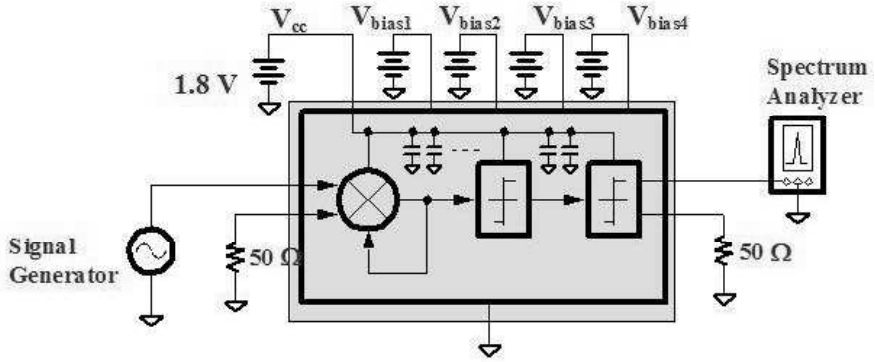
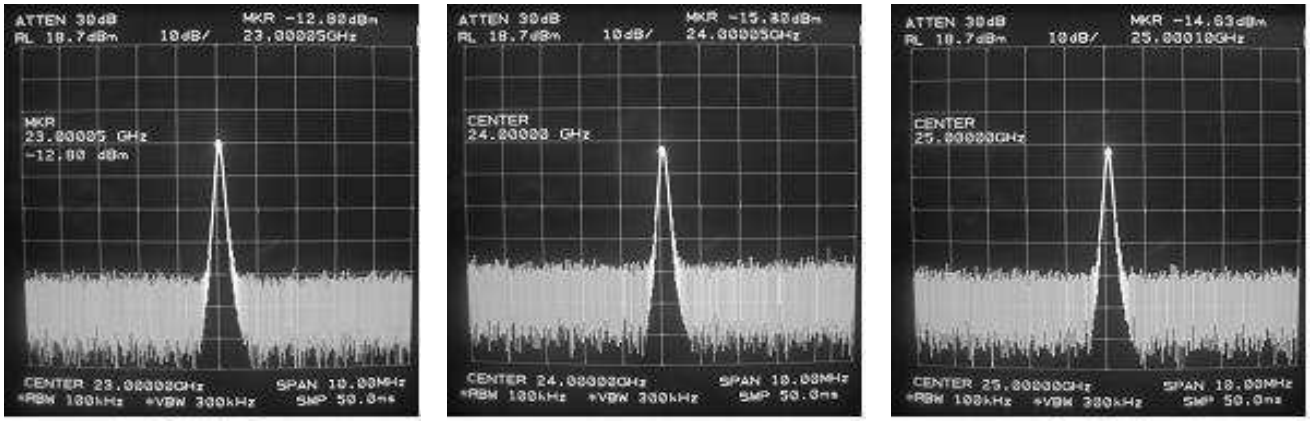


Figure 9. Single-ended input test configuration.



(a) (b) (c)

Figure 10. Output spectrum for regenerative frequency divider at (a) 46 GHz, (b) 48 GHz, (c) 50 GHz input frequency.

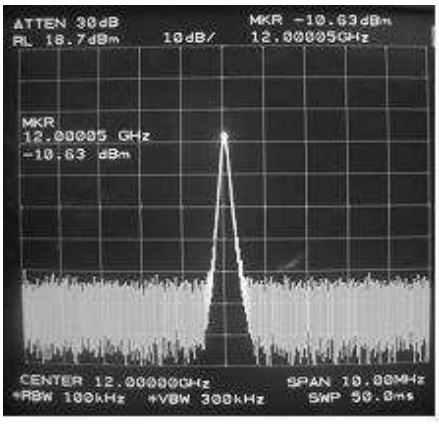


Figure 11. Output spectrum for master-slave frequency divider at 24 GHz input frequency.

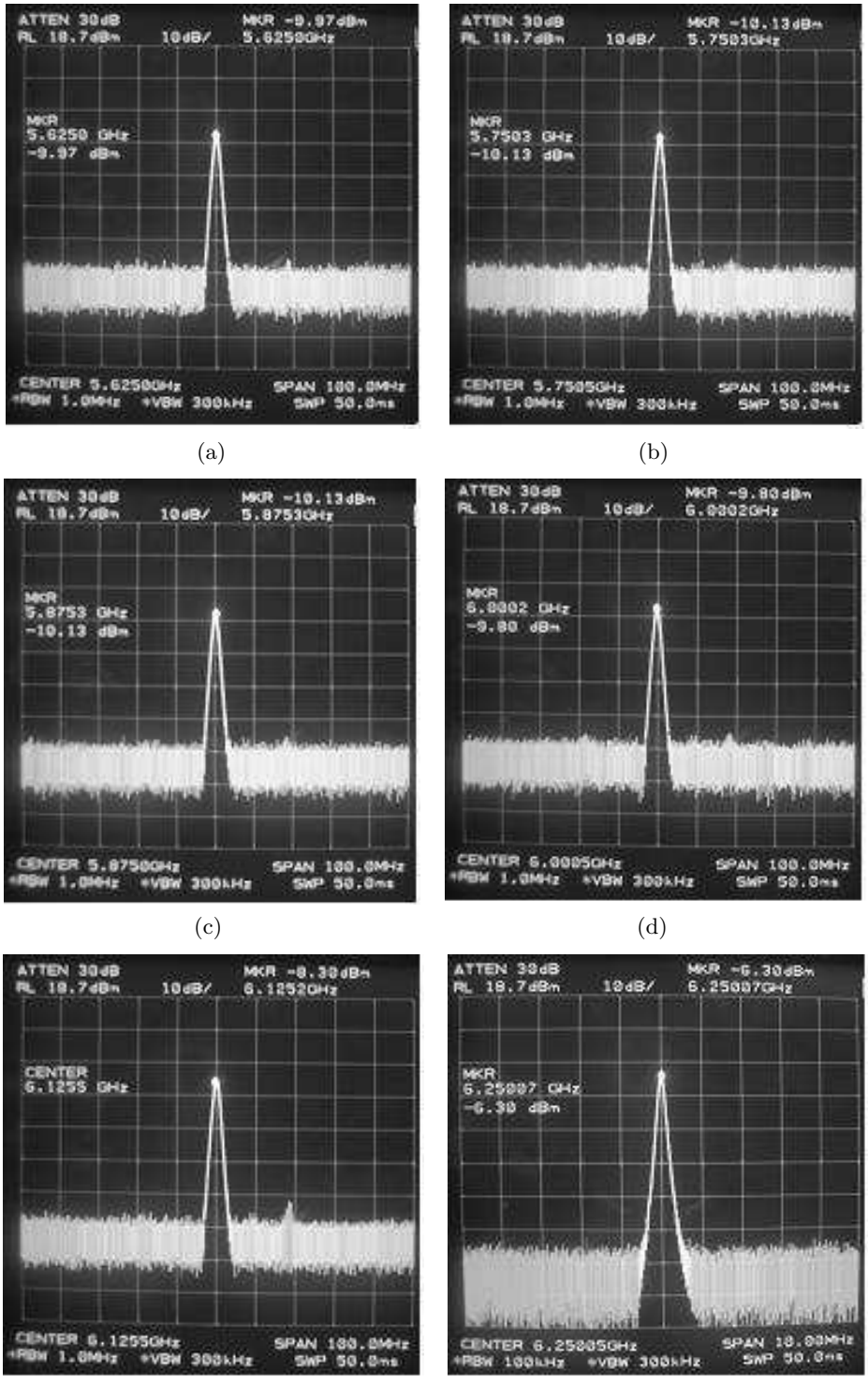


Figure 12. Output spectrum for divide-by-8 frequency divider at (a) 45 GHz, (b) 46 GHz, (c) 47 GHz, (d) 48 GHz, (e) 49 GHz, (f) 50 GHz input frequency.

Table 1. Comparison between input frequency, power consumption, and chip area for various regenerative dividers.

Ref	Technology	Frequency (GHz)	Power (mW)	Area including pads (mm^2)
[4]	0.25 μm SiGe	103	195	0.50
[6]	0.15 μm SiGe	110	310	0.25
[7]	SiGe	63	470	0.81
[8]	0.15 μm GaAs	28	100	4.50
This work	0.18 μm SiGe	48	18	0.42

Table 2. Comparison between input frequency, power consumption, supply voltage, and chip area for various static dividers in SiGe.

Ref	Technology	Frequency (GHz)	Power (mW)	Supply voltage (V)	Area including pads (mm^2)
[4]	0.25 μm SiGe	71	140	3.5	0.50
[9]	0.18 μm SiGe	42	160	2.1	0.28
[10]	0.35 μm SiGe	71.8	594	4.5	0.25
This work	0.18 μm SiGe	30	54	1.8	0.36

4. CONCLUSION

Three types of dividers fabricated in 0.18 μm SiGe BiCMOS technology are reported. The dividers are part of a frequency synthesizer for a 60 GHz receiver. The dynamic divider employs a regenerative structure. The regenerative divider handles very high frequencies, up to 50 GHz and consumes 18 mW from 1.8 V supply voltage. Meanwhile, the static divider employs a conventional master-slave structure. The master-slave divider operates up to a 30 GHz input frequency from a very low supply voltage, 1.8 V. In addition, a divide-by-8 chain, which is a combination of a regenerative and two master-slave dividers has been presented.

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