# A SiGe 6 Modulus Prescaler for a 60 GHz Frequency Synthesizer

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## ABSTRACT

A prescaler is widely used in frequency synthesizers in order to handle channel selection. The division ratio has to be chosen carefully to achieve the desired frequency. In this paper, we present a 6 modulus prescaler in a 0.18 $\mu$m SiGe BiCMOS technology. The prescaler is part of a 60 GHz frequency synthesizer. In addition, we present a frequency planning for the 60 GHz frequency synthesizer. The prescaler employs an integer-$N$ architecture. The circuit has a programmable divider with a division ratio of 7 and 8 and two counters to control the division ratio. The programmable divider utilizes ECL circuits, while the counters utilise CMOS circuits. Therefore an ECL-to-CMOS converter is used to bridge these two kinds of circuits. Simulation results show that the prescaler operates up to 4 GHz from a 1.8 V supply voltage.

**Keywords:** frequency synthesizer, prescaler, dual-modulus divider, integer-$N$ architecture

## 1. INTRODUCTION

Recently, 60 GHz band is of interest for many RF researchers. The band offers a number of advantages, such as free licence, wide channel bandwidth, and high oxygen absorption which is beneficial for security applications.[1,2] However, a very high frequency RF transceiver is required in order to exploit this band.

One of the important circuits in a RF transceiver is the frequency synthesizer. A phase-locked loop (PLL) is commonly used for the frequency synthesizer, which provides a reference frequency for translating baseband to RF signal in the up-conversion process. Also the reference signal is used to translate an RF signal to baseband signal in the down-conversion process. For channel selection, the frequency synthesizer must be able to provide different reference frequencies according to the selected channel.

A number of researchers have reported on PLL design for a 60 GHz transceiver.[3,4] However, their research concentrates only on the PLL architectures and circuit blocks regardless of the channel selection in the synthesizer. In addition, there is no proper frequency planning for the synthesizer. This paper discusses the frequency planning for a PLL based frequency synthesizer and a prescaler for a 60 GHz transceiver. The prescaler enables 6 different channel frequencies in the synthesizer. For the 60 GHz frequency synthesizer, the prescaler is required to operate at high frequency. By contrast, for a low GHz frequency synthesizer, only a low frequency prescaler is required. In this paper, we propose a prescaler design that operate at high frequencies and fulfill the frequency planning requirement for the 60 GHz frequency synthesizer.

Frequency planning is required before a prescaler is designed. The frequency planning determines the prescaler input frequency and determines how six different channel frequencies are achieved. Section 2 discusses details of the frequency planning.

Two types of architecture are commonly used for the prescaler design: an integer-$N$ architecture and a fractional-$N$ architecture. The proposed prescaler employs an integer-$N$ architecture. Section 3 reviews the integer-$N$ architecture and the reason it is chosen for this work. Section 4 present and discusses the prescaler circuit implementation. It is followed by the simulation results and conclusion in Section 5 and 6, respectively.

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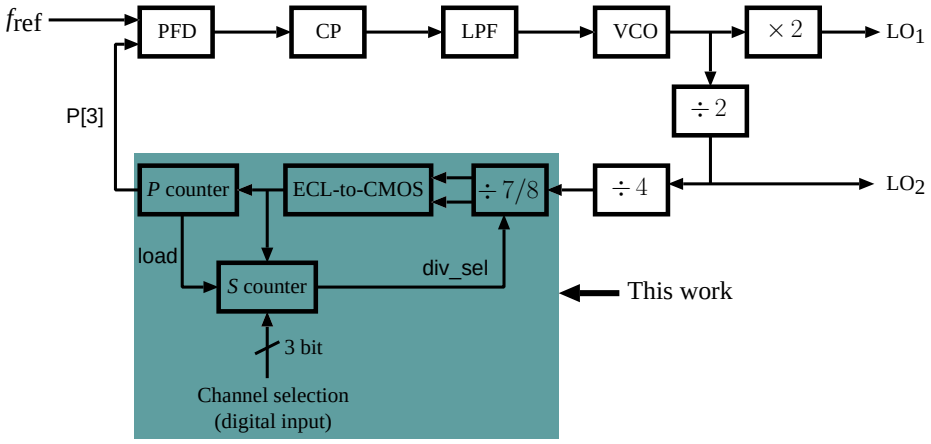


**Figure 1.** A Phase-Locked Loop (PLL) with a prescaler. The $LO_1$ is 4/5 of the RF frequency and $LO_2$ is 1/5 of the RF frequency. The prescaler input frequency is 1/4 of the $LO_2$. PFD is a Phase-Frequency Detector, CP is a Charge Pump, LPF is a Low Pass Filter and VCO is a Voltage-Controlled Oscillator.

## 2. FREQUENCY PLANNING

The proposed prescaler is part of the frequency synthesizer for a 60 GHz RF transceiver. The Phase-Locked Loop (PLL), part of the transceiver is shown in Figure 1.

The first LO ($LO_1$) is 4/5 of the RF frequency and second LO ($LO_2$) is 1/5 of the RF frequency. The VCO output (which is half of the $LO_1$ signal) has 6 possible frequencies from 47.2 to 51.2 GHz, pointing to 6 different channels. The VCO output is divided by 4 to get $LO_2$. Then the $LO_2$ signal is divided by 4, yielding the frequencies from 2.95 to 3.2 GHz. The prescaler divides the $LO_2$ according to channel selection.

Three main components in the prescaler are dual-modulus divider ($N/N+1$), P counter and S counter. The signal is divided by $N+1$ (which is 8) for $S$ times. Then the signal is divided by $N$ (which is 7) for $P-S$ times. This complete cycle division gives a fixed value of 50 MHz, which can be used for the PLL to lock to a fixed reference clock. Table 1 summarize the frequency planning.

**Table 1.** Frequency planning for the frequency synthesizer for a 60 GHz transceiver.

| Channel | $f_{VCO}$ (GHz) | $f_{LO_1}$ (GHz) | $f_{LO_2}$ (GHz) | $f_{LO_2}/4$ (GHz) | Division Ratio (M) | $f_{ref}$ (MHz) |
|---|---|---|---|---|---|---|
| 0 (000) | 23.6 | 47.2 | 11.8 | 2.95 | 59 | 50 |
| 1 (001) | 24.0 | 48.0 | 12.0 | 3.00 | 60 | 50 |
| 2 (010) | 24.4 | 48.8 | 12.2 | 3.05 | 61 | 50 |
| 3 (011) | 24.8 | 49.6 | 12.4 | 3.10 | 62 | 50 |
| 4 (100) | 25.2 | 50.4 | 12.6 | 3.15 | 63 | 50 |
| 5 (101) | 25.6 | 51.2 | 12.8 | 3.20 | 64 | 50 |

## 3. INTEGER-$N$ ARCHITECTURE

There are two types of frequency synthesizer architecture, (i) a fractional-$N$ architecture and (ii) an integer-$N$ architecture. In this research an integer-$N$ architecture is adopted because of its suitability to the proposed frequency planning. The integer-$N$ architecture is implemented using a dual-modulus divider, a program counter

($P$ counter), and a swallow counter ($S$ counter), as shown in Figure 2. The dual-modulus divider is controlled by the $P$ and $S$ counters. The prescaler division ratio, $M$ is given by

$$M = N \times P + S, \tag{1}$$

where $N$ is divider, $P$ is program counter value and $S$ is swallow counter value. The $S$ counter value depends on the selected channel.

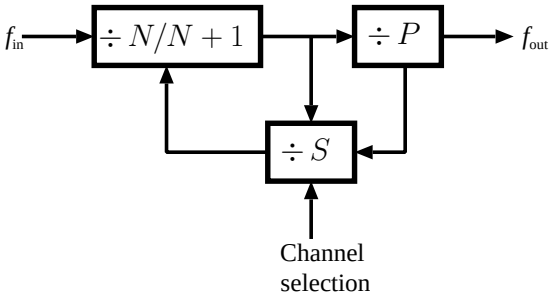


**Figure 2.** An integer-$N$ architecture is implemented by three main components, which are a dual-modulus divider, a $P$ counter and an $S$ counter.

An integer-$N$ architecture provides channel spacing at one or multiple of the reference frequency. For example, if the reference frequency is 1 MHz, possible channel spacing are 1 MHz, 2 MHz, 3 MHz etc. Current low GHz RF communication has a limited channel bandwidth. Therefore, the system can only afford small channel spacing. Because of the integer-$N$ architecture output can only be multiplication of reference frequency, this architecture is not popular in low GHz RF communication. Instead, fractional-$N$ architecture is used because the output frequency can be a fraction of the reference frequency.[5,6] On the other hand, 60 GHz RF communications has a very wide channel bandwidth. Namely 7 GHz from 57 GHz to 64 GHz is available for communication. Therefore, the integer-$N$ architecture is suitable for the 60 GHz system.

## 4. CIRCUIT IMPLEMENTATION

The dual modulus prescaler consists of a dual modulus divider (divide-by-7 and 8), two counters (named as $P$ and $S$ counters) and an ECL-to-CMOS converter. In addition, a single input to differential output circuit is added to the prescaler input for testing purpose. Each circuit block is discussed in the following sub-section.

### 4.1. Dual Modulus Divider

The dual-modulus divider consists of two stages. The first stage is divide-by-3 and 4, and the second stage is divide-by-2. Figure 3 shows a simplified schematic of the dual-modulus divider. The circuit architecture is based on divider circuit in Reference,[7] except the proposed circuit operates at 3 times higher frequency.

Three D flip-flops, two OR gates and one NAND gate are used to implement the divider. All these circuits are built using emitter-coupled logic (ECL) circuit topology. ECL is used because it can handle high operating frequency at the cost of more power consumption. Figure 4, 5, and 6 show the ECL D flip-flop, ECL OR gate and ECL NAND gate.

The divider has two division ratios, 7 and 8. The division ratio is controlled by an input signal named `div_sel`, which is comes from S counter. If the `div_sel` is HIGH, the division ratio is 8, while if it is LOW the division ratio is 7.

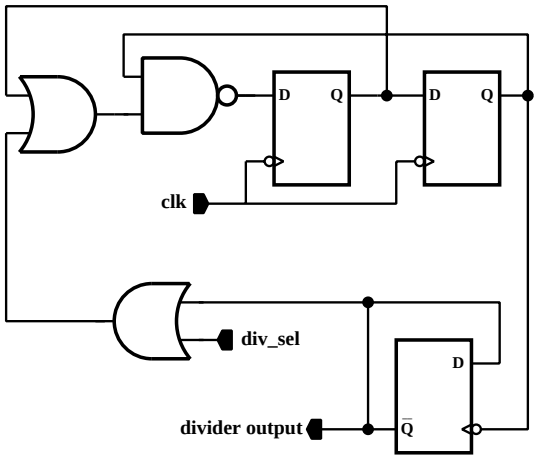


**Figure 3.** Dual-modulus divider. The top D flip-flops is a divide-by-3 or 4 circuit and the bottom D flip-flop is a divide-by-2 circuit. The `div_sel` signal determines the division ratio.

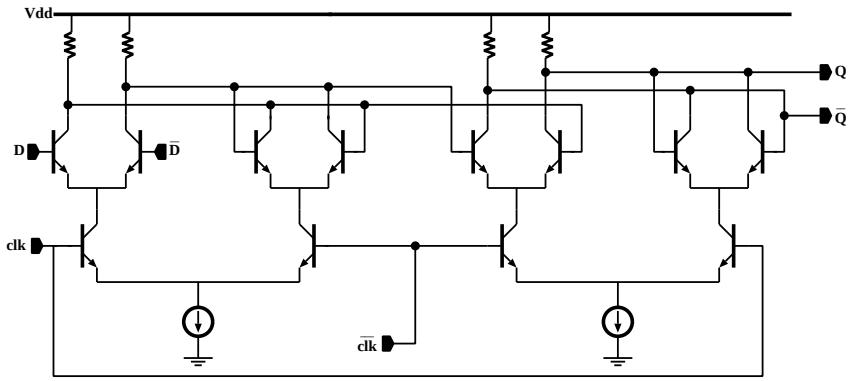


**Figure 4.** ECL D flip-flop. The D flip-flop is implemented using master-slave architecture.

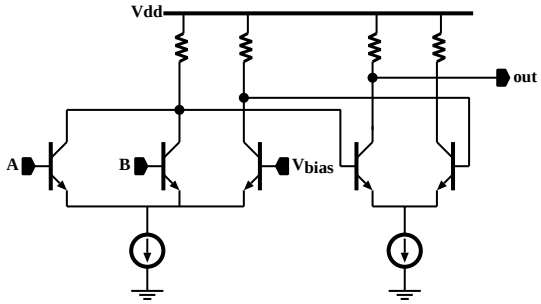


**Figure 5.** ECL OR gate.

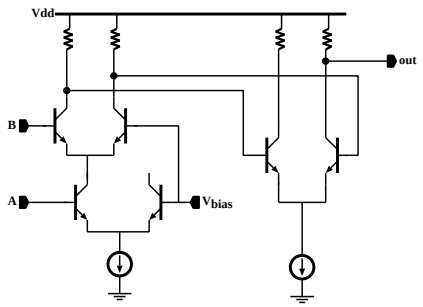


**Figure 6.** ECL NAND gate.

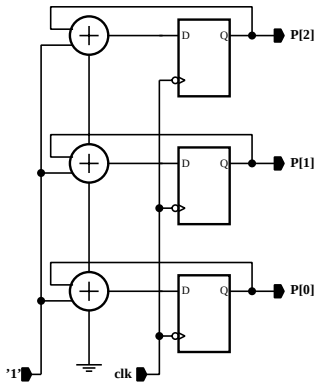


**Figure 7.** The $P$ Counter is a 3-bit synchronous binary down counter.

### 4.2. P Counter

The P counter is a 3-bit synchronous binary down counter. The counter is built from full adders and D flip-flops as shown in Figure 7.

The P counter is clocked by the dual-modulus divider output. The Most Significant Bit (MSB) of the counter is the output of the prescaler. This counter also provides a signal named load to the S counter. The `load` signal is HIGH only when all the P counter outputs are zeros.

### 4.3. S Counter

The S counter is same as the P counter except it has two extra input signals named load and digital input. Therefore, the counter has multiplexers in addition to full adders and D flip-flops. Figure 8 shows the S counter block diagram.

The clock signal comes from the dual-modulus divider output, and the `load` signal is from the P counter. The 3 bit digital input signal is user-defined and it determines the prescaler division ratio. The prescaler can handles six different digital inputs, from 000 to 101. This will give six different division ratios, 59, 60, 61, 62, 63 and 64. In order to get a correct division ratio, each digital input is added by 3. For example, if the digital input is 001, the $S$ value is 4. The S counter has an output signal named `div_sel`, which is feed to the dual-modulus divider, as explained in sub-section 4.1.

When the `load` signal is HIGH, the S counter loads the digital input to the output and starts count down from that binary input value. The S counter outputs maintain zeros until next load signal is HIGH. When all the S counter output are zeros, `div_sel` signal is LOW.

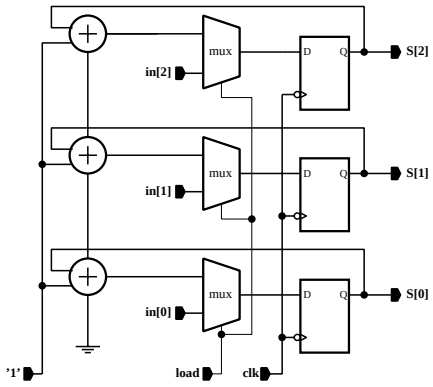


**Figure 8.** The S Counter is a 3-bit synchronous binary down counter with a load signal.

### 4.4. ECL-to-CMOS

An ECL-to-CMOS circuit is used to match the logic level between dual-modulus divider and the counters. Figure 9 shows the ECL-to-CMOS schematic.

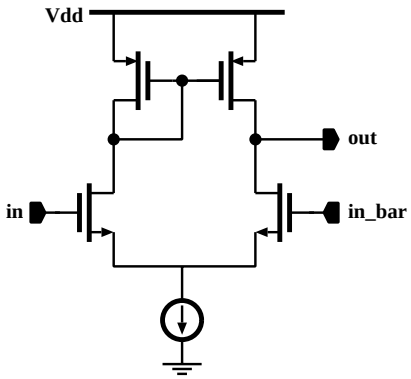


**Figure 9.** ECL-to-CMOS converter schematic.

As explained in previous sub-section, P and S counters are clocked by dual-modulus divider output. However, dual-modulus divider is an ECL circuit while the counters are CMOS circuits. Therefore, ECL-to-CMOS converter is required between the divider and counters. Unfortunately, the ECL-to-CMOS circuit introduce some delays. The delayed clock delays the counters output, including the `div_sel` signal from the S counter. As explained before, `div_sel` is fed back to the dual-modulus divider to determine the division ratio. As a result, the overall prescaler operating frequency is constrained by this delay issue. This delay is shown by the simulation results in Figure 10. From the simulation, the delay at negative edge is smaller compared to positive edge. As the D flip-flops in $P$ and $S$ counters are negative edge triggered, a further optimisation has been done to reduce this delay by proper transistor sizing.

## 5. RESULT

The prescaler is designed and simulated using the Cadence and JAZZ SBC18 design kit. It was fabricated on 0.18 $\mu$m SiGe BiCMOS technology. The prescaler is designed to operate up to 4 GHz, though the maximum requirement operating frequency is just 3.2 GHz. Figures 11 and 12 show the prescaler simulation results for 6 different digital input from 000 to 101, when using a 4 GHz input frequency. Each result contains three waveforms, which are the prescaler output, the dual-modulus divider output and the `div_sel` signal. The circuit consumes 70 mA from a 1.8 V supply voltage.

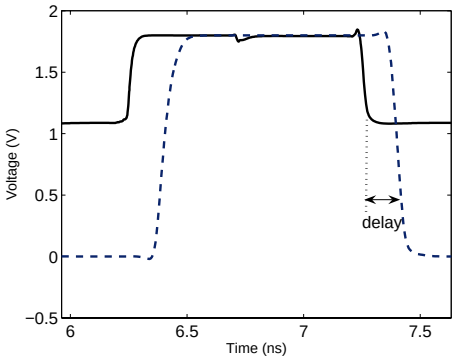


**Figure 10.** Delay caused by ECL-to-CMOS converter.

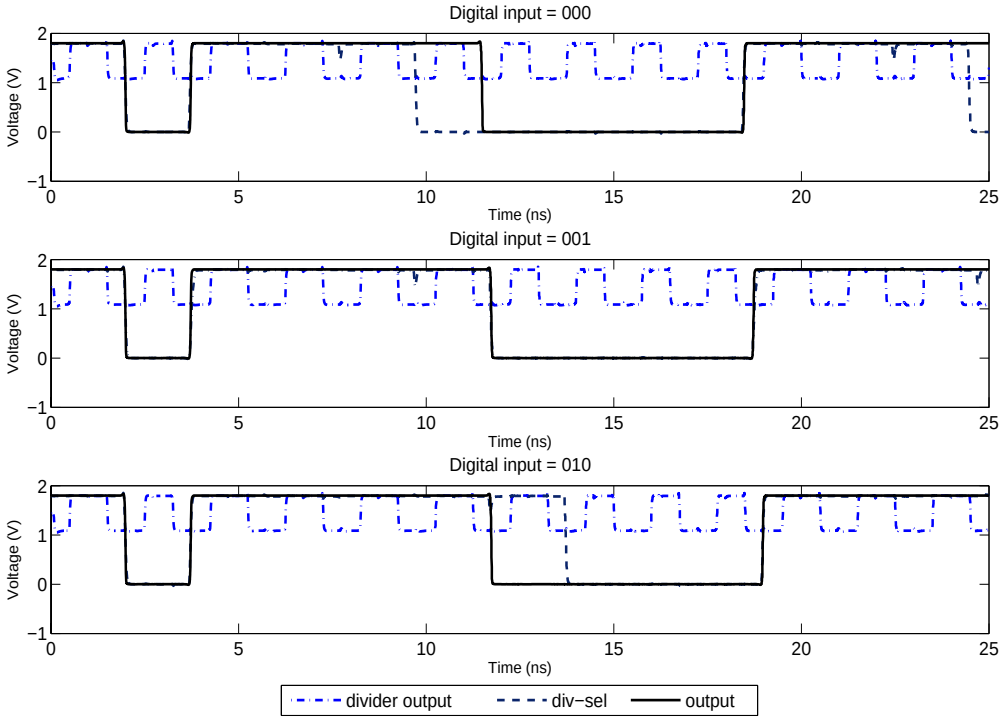


**Figure 11.** Prescaler result for digital input at 000, 001 and 010.

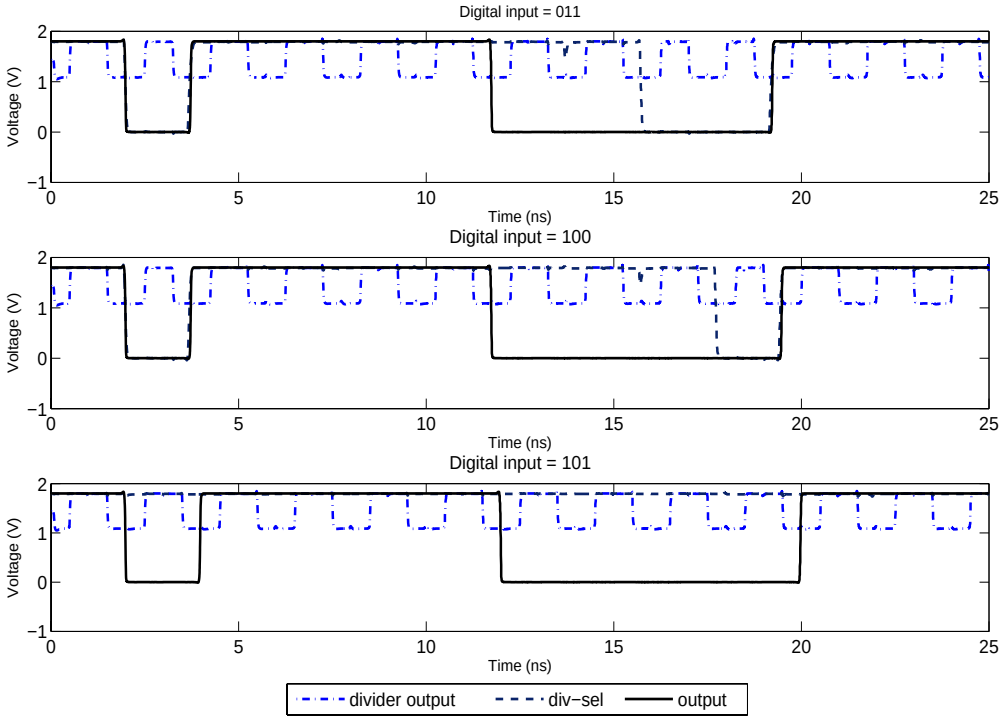


**Figure 12.** Prescaler result for digital input at 011, 100 and 101.

## 6. CONCLUSION

A frequency planning and a prescaler for a 60 GHz frequency synthesizer are presented. The prescaler employs an integer-$N$ architecture and is implemented by a dual-modulus divider, two counters, and an ECL-to-CMOS converter. It is designed to provide six different division ratio for six different channel frequency selection. The circuit handles a very high operating frequency, up to 4 GHz and consumes 69 mA from a 1.8 V supply voltage.

## 7. ACKNOWLEDGEMENTS

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