An Automated Approach for Evaluating Spatial Correlation in Mixed Signal Designs Using Synopsys HSpice®

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ABSTRACT

With current aggressive down scaling of critical dimensions (CD) in integrated circuits (IC) technologies, the impact of variations on the amount of power and performance variance of a system is growing. At present, in large scale IC designs one of the main concerns is the position dependant variations or simply spatial variation. Using different regions on a chip and defining a correlation matrix is one of the ways to handle spatially correlated variations. Unfortunately, using current versions of HSpice tool is not efficient to handle such variations as explained later.

In this paper we present an alternative design flow with focus on including the spatial variations analysis at the design phase. Using a combination of different file-types such as, layout information and hierarchical Spice code using the proposed approach lead to a more effective and efficient way of variability analysis with HSpice tool. Current version of HSpice can support only a Spice code with a single sub-circuit for spatial variations analysis [1] which is entirely on the opposite side of the hierarchical design concept. Therefore, we propose an alternative way to provide an automatic spatial variation compatible Spice code generator module to allow such modelling for a large design.

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1. Introduction

Due to technology scaling challenges faced by the designers are become more complex. Variability, leakage power dissipation, and thermal aspects are some of the big challenges in nanometre circuits and systems design. Today, circuit designers have to consider not only the trade-off between delay and power, but also the impact of process and environmental variations on the delay-energy and parametric yield trade-off. Consequently, delay of circuits, dynamic and static power consumption, and frequency of operation are no longer deterministic and must be modelled statistically [2]. Furthermore, circuit robustness is becoming a key aspect in nanometre scale VLSI, where variation ranges of many process and environment parameters will increase dramatically. At the same time, computer-aided design (CAD) developers are also challenged by this aggressive increase in the amount of variability.

There is no doubt that Synopsys HSpice is one of the well-known tools for circuit analysis and evaluation. It is also an up-to-date software considering variability issues. On the other hand, a spatial variation analysis requires much more efforts than the other types of variation like, global and local. At present, HSpice tool supports only a single sub-circuit with spatial variation block which is completely on the opposite side of the hierarchical design concept [2].

This paper proposes an automated approach for analysing spatially correlated parameters within a chip using Synopsys HSpice tool. There are three reasons that this proposal will help designers to have a more accurate prediction for parametric yield and design margins. Firstly, the variation-aware design is one of the most important aspects of IC design for the nanometre scale technologies [2]. Secondly, HSpice is well-known software and it is an applied tool for educational and industrial purposes. Thirdly, spatial correlation analysis becomes more important after decreasing the critical dimension (CD) of a device.

It is worth mentioning that this paper has focused on the automated flow approach to analysis spatially correlated parameters rather than an optimization or mitigation of spatial variation.

Section 2 briefly reviews the importance of spatial variation and its contribution towards performance over/under estimation. In Section 3, we discussed the proposed evaluation approach for spatial variation analysing. Section 4 presents a case of study that demonstrate the proposed design flow, while Section 5 presents conclusion and some future works.

2. Spatial variation review

Analysing an extracted Spice code from a large scale deign in terms of performance, power and other characteristics at the circuit level, especially for post-layout study, can almost be done using HSpice tool. Generally, HSpice is a standard tool in a foundry compatible design flow. HSpice has offered different solutions for new sets of challenges in nanometer scale IC design era. In particular, for variability analysis there are three different ways. 1) Variation block, 2) Variation parameter and 3) Variation model [1]. Variation block is an established method for global and local variability. For spatial correlation analysis, however, it is not an efficient way to analyse. A limitation of using only a single sub-circuit in the variability analysis flow including spatial variation needs to be improved.

Regardless of the variety of distributions being used by the variation block, which is still a challenge in variability modelling, the total variance in a circuit characteristics simply has three different components, global, local and spatial variation which is given by Eq. (1). This equation is a simple linear variance model for the total variance.

$$\sigma^2_{total} = \sigma^2_{global} + \sigma^2_{local} + \sigma^2_{spatial} \qquad (1)$$

Fig.1 explains the difference between local and global variations in IC design. The number of rows and columns in the matrix is equal to the number of devices and parameters, respectively. This means that the global variation affects all devices on a chip equally. Local variation, however, affects all devices in a chip differently [2].

$$\begin{pmatrix} V_{th0\_D0} & L_{eff\_D0} & \cdots & V_{fb\_D0} \\ V_{th0\_D1} & L_{eff\_D1} & \cdots & V_{fb\_D1} \\ & & \cdots & \\ V_{th0\_Dn} & L_{eff\_Dn} & \cdots & V_{fb\_Dn} \end{pmatrix}$$

Figure 1 – Matrix demonstration of global and local variations

The spatial correlation concept in IC design can be described as shown in Fig. 2. This demonstration is based on the quad-tree partitioning approach which is proposed in Ref. [2]. In this method a die is divided into many parts based on a partitioning approach that results in optimum number of parts. Regardless of the method complexity, it is one of the best ways to model the spatial correlation in a chip [2].

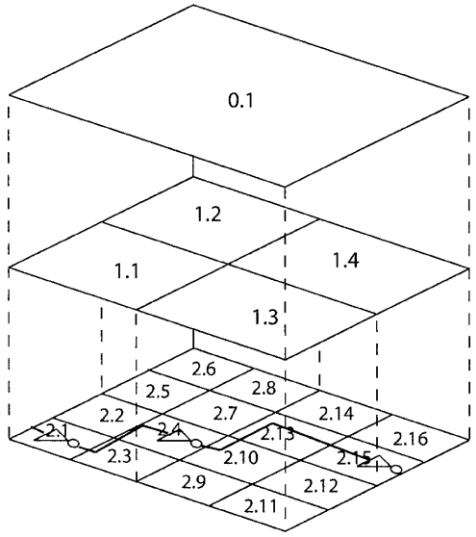

Figure 2 - Spatial correlation modelling with quad-tree partitioning method (After [2]).

Now the question is how important is the spatial correlation to the performance analysing of a design? The answer could be found in Fig. 3 [1]. As illustrated in the figure, if there is a significant spatial variation, thus it has to be taken into account. Statistical circuit analysis in the absence of

[1] CDF: Cumulative Distribution Function, PDF: Probability Distribution Function

spatial variation while it is significant causes a big error in predicted variance and actual variance of the system performance.

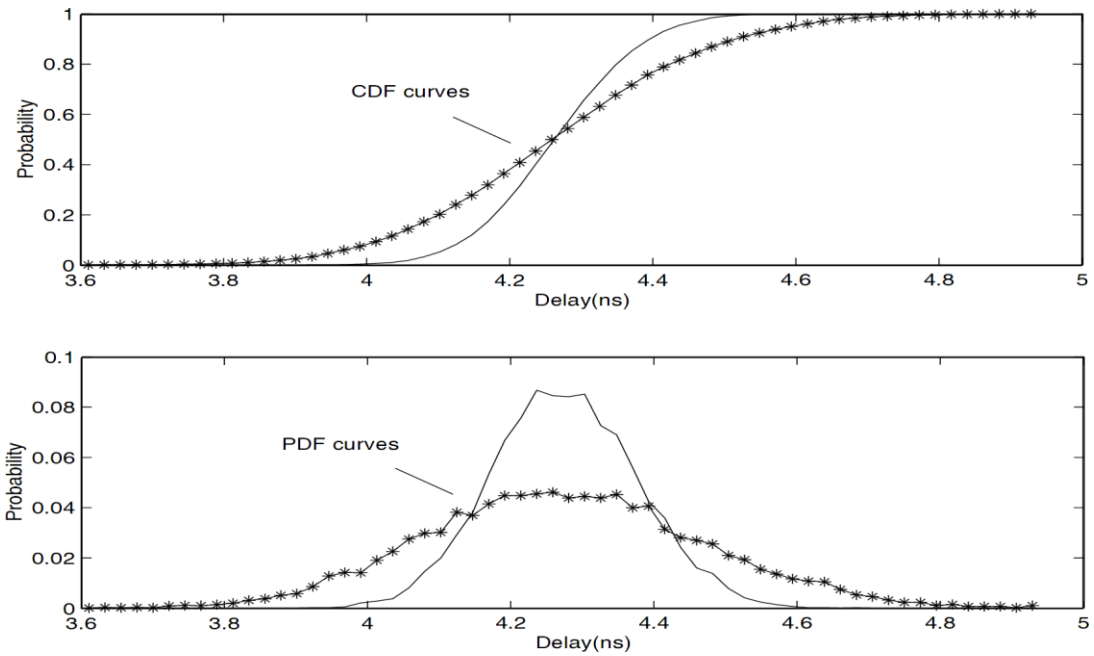

Figure 3 – Delay variation in the absence of spatial correlation (solid curve) and under spatial correlation (the curve with stars) (After [3])

HSpice software provides a variability block for spatial analysis in the design phase, but a limitation to use only a single sub-circuit. This limitation can cause many problems when a designer is dealing with a hierarchical design. In the next part an alternative design flow is proposed which provides a spatial correlation analysis compatible Spice code using information extracted from the design layout.

3. Proposed design flow

As discussed in the previous section, the proposed design flow has particularly focused on variability analysis. This proposed design flow is simply demonstrated in Fig. 4. Part 1 in Fig. 4 is a classic hierarchical Spice code which is used in the conventional design charactristic approach. Part 2 is a layout information file. This file is an ASCII extract file which consists of information about transistors names, terminals and positions. In this paper we used the Magic extract format (.ext files). In Part 3, proposed algorithm reads both of these files and generate a spatial correlation compatible HSpice netlist.

The Magic extract output file for a multiplexer is partially shown in Fig. 5. All the elements in the magic's output file are defined by a set of rectangles and coordinates. Each rectangle is defined by two coordinates, bottom-left (x_0,y_0) and top-right (x_1,y_1). For instance, in Fig. 5, the first "rect" is between (59, 1) and (60, 2).

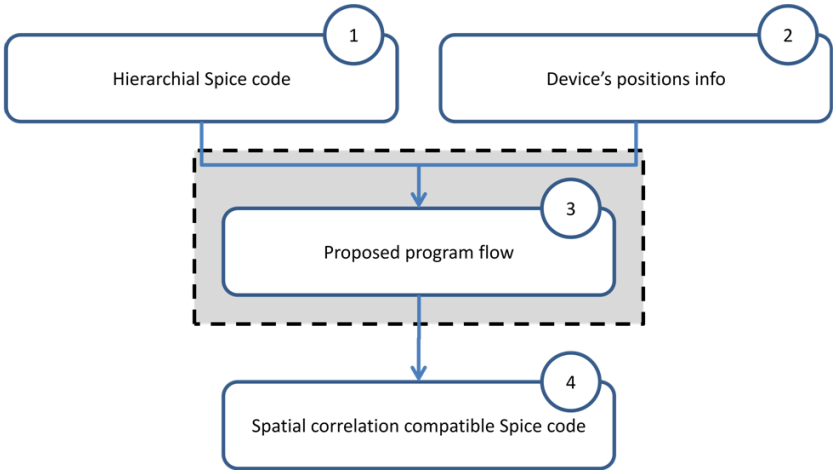

Figure 4 – Simple steps of the proposed flow

The main aim of our proposed flow is providing a spatial variation analysis compatible netlist, so device's positions are very important for us. The second most important is device's name. As illustrated in Fig. 6, assigning an X and Y coordinates is the integral part of the proposed algorithm. For this reason, there is a need to find the right device for assigning X and Y.

Type	*Loc*	*A P*	*Subs*	*Gate*	*Source*	*Drain*
fet nfet	59 1 60 2	8 12	GND!	Mid2 4 **N3**	Out 4 0	Vss#0 4 0
fet nfet	36 1 37 2	8 12	Float	Mid1 4 **N2**	Mid2 4 0	Vss#0 4 0
fet nfet	4 1 5 2	8 12	Vss#0	In 4 **N1**	Mid1 4 0	Vss#0 4 0
fet pfet	59 25 60 26	8 12	Vdd!	Mid2 4 **P3**	Vdd#0 4 0	Out 4 0
fet pfet	36 25 37 26	8 12	VBias	Mid1 4 **P2**	Vdd#0 4 0	Mid2 4 0
fet pfet	4 25 5 26	8 12	Vdd#0	In 4 **P1**	Vdd#0 4 0	Mid1 4 0

Figure 5 – Extracted netlist from Magic Layout (After [4])

Adding or inserting a spatial variation block is the next level of the program flow. As demonstrated in Fig. 6, if there is a variation block (m: "false") so the program only has to insert the spatial block, but, if there is no variations block (m: "true") so if m is "true", the program has to add a spatial variation and a Monte-Carlo sweep in the generated netlist.

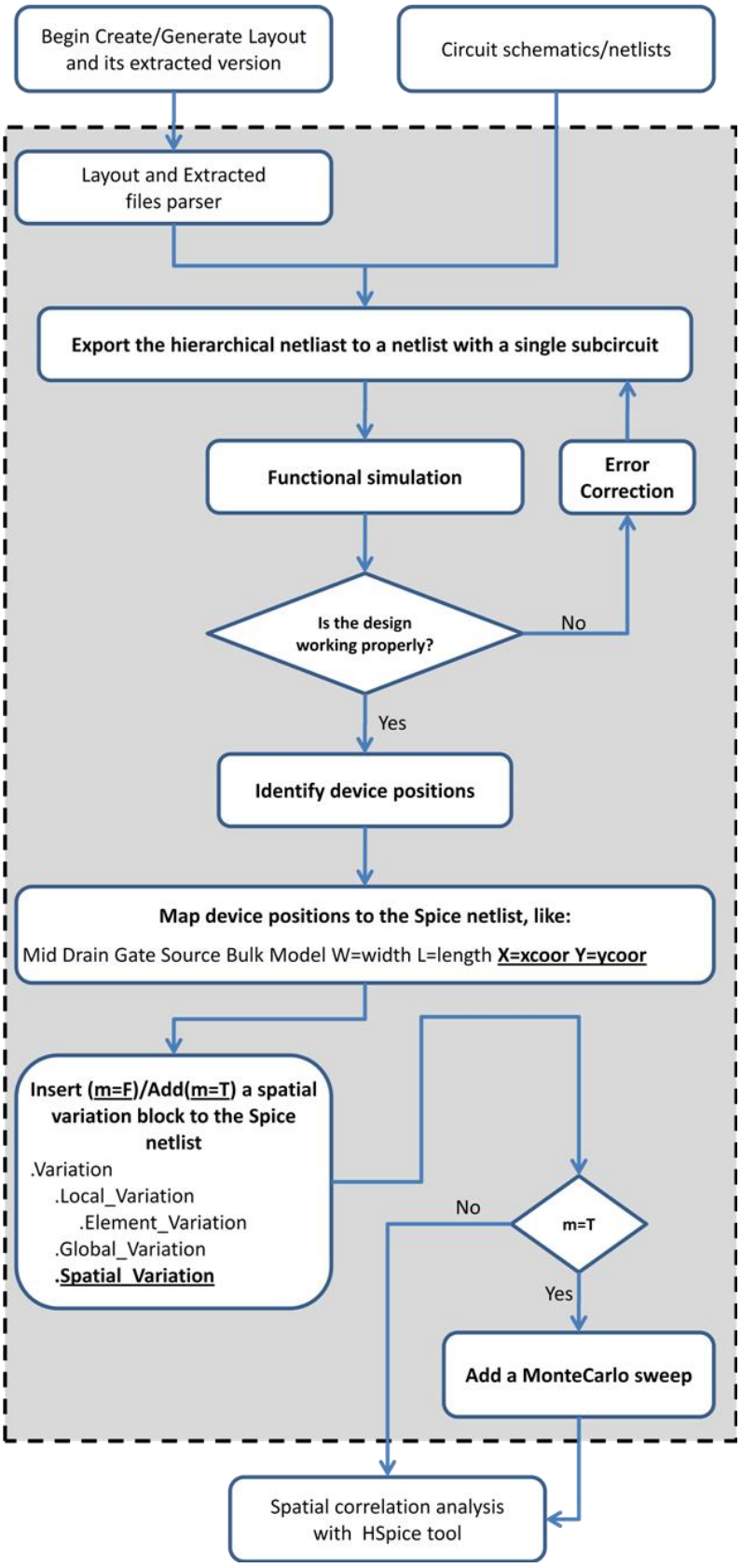

Figure 6 – The proposed flow to automate spatial correlation analysis using HSpice

The main loop of the program core for generating a HSpice spatial analysis compatible netlist is as follows:

```
Input (A): Circuit netlist with a single sub-circuit
Input (B): Circuit layout & extracted file
Output(C): A HSpice spatial correlation analysis compatible netlist

…

Initialize the number of devices with the number of fet transistors in the A
input file
while (number of iteration > number of devices)
      for each fet transistor in B
                  /*
                  Obtain (x0,y0) and (x1,y1),
                  where x0,x1,y0 and y1 all based on the lambda (layout) rules
                  */
            xcoor=Round((x0+x1)/2)
            ycoor=Round((y0+y1)/2)
            find the transistor in A
            parse the line and insert X=xcoor Y=ycoor with micrometer unit by
            the end of fet  definition
      end for
end while

…

Output C
```

The **A** input is not the original input netlist. It is a single sub-circuit netlist that the program generates from the main input netlist.

The importance of this approach becomes more significant when we realizes that most of the spatial variations analysing software are not widely available (like HSpice) and almost all of them are dedicated only for doing spatial analysis. On the other hand, HSpice has a significant advantage that designers can perform a wide range of analysing in digital, analog, mixed-signal and RF areas considering variability specifications.

4. Case study

In this section we applied the proposed method on a relatively simple circuit. The circuit is an 80-bits adder. The adder circuit contains 5365 MOSFET transistors. According to the proposed approach at the first step we made a plain Spice netlist from hierarchical Spice netlists. We also used the extracted file from Magic Layout. The following netlist shows 10 lines of plain Spice netlist surrounding (0,0) coordinate (W and L scale: 0.1µm).

…

```
m5312 x593/a_13_11 x591/b Vdd Vdd pch w=12 l=2
m5313 Gnd x591/b x593/a_43_4 Gnd nch w=6 l=2
m5314 Gnd x1060/out0 x1114/in0 Gnd nch w=3 l=2
m5315 x1114/in0 x1060/out0 x585/a_15_11 Vdd pch w=12 l=2
m5316 x585/a_15_11 x585/b Vdd Vdd pch w=12 l=2
m5317 x1114/in0 x585/b Gnd Gnd nch w=3 l=2
m5318 x1115/in0 x587/c x587/a_43_4 Gnd nch w=6 l=2
m5319 Vdd x587/c x1115/in0 Vdd pch w=12 l=2
m5320 x587/a_43_4 x1063/out0 Gnd Gnd nch w=6 l=2
m5321 x1115/in0 x1063/out0 x587/a_13_11 Vdd pch w=12 l=2
…
```

The following rectangle codes are also extracted from *.mag - layout - file. In this stage we have both *.mag and *.ext - extracted – files so we are able to assign a position to each transistor accurately. It is worth noting that the extracted file contains connectivity and coordinate information.

```
<< ntransistor >>
…
rect 42 14 48 16
rect 42 9 45 11
rect 42 1 48 3
rect 42 -4 45 -2
rect 42 -16 48 -14
…
<< ptransistor >>
…
rect 13 14 25 16
rect 13 9 25 11
rect 13 1 25 3
rect 13 -6 25 -4
rect 13 -16 25 -14
…
```

The output netlist is as follow:

```
…
m5312 x593/a_13_11 x591/b Vdd Vdd pch w=12 l=2 X=2u Y=2u
m5313 Gnd x591/b x593/a_43_4 Gnd nch w=6 l=2 X=5u Y=2u
m5314 Gnd x1060/out0 x1114/in0 Gnd nch w=3 l=2 X=4u Y=1u
m5315 x1114/in0 x1060/out0 x585/a_15_11 Vdd pch w=12 l=2 X=2u Y=1u
m5316 x585/a_15_11 x585/b Vdd Vdd pch w=12 l=2 X=2u Y=0
m5317 x1114/in0 x585/b Gnd Gnd nch w=3 l=2 X=5u Y=0
m5318 x1115/in0 x587/c x587/a_43_4 Gnd nch w=6 l=2 X=4u Y=-1u
m5319 Vdd x587/c x1115/in0 Vdd pch w=12 l=2 X=2u Y=-1u
```

m5320 x587/a_43_4 x1063/out0 Gnd Gnd nch w=6 l=2 **X=5u Y=-2u**
m5321 x1115/in0 x1063/out0 x587/a_13_11 Vdd pch w=12 l=2 **X=2u Y=-2u**
…

For the following simulations, TSMC-180 um process parameters were used. The mean and standard deviation simulation results for this adder delay time without considering the spatial correction modelling is shown in Table 1. If the simulation be repeated, for a critical path delay we have (To calculate the delay using HSpice we assumed trigger is a[0] – the first input bit – target cout[79] – the last carry out bit -):

Table 1. Simulation results of the 80 bit adder with and without spatial correlation analysis.

	***Without** spatial correlation analysis* (second)	***With** spatial correlation analysis* (second)
mean	10.4682n	10.4648n
sigma	7.0819p	11.1026p

It is worth mentioning that the number of simulation points is 50 which is not a good choice for an accurate result, but does demonstrate a practical example of the proposed approach and the impact of spatial correlation on the standard deviation of performance metrics.

5. Conclusions and Recommendations

This paper presents an alternative automated flow for evaluating spatial correlation across a design using Synopsys HSpice tool. The basic parts of the flow are a file with information about device positions, assigning the position to the right device in a hierarchical netlist and providing a flat Spice netlist with a single sub-circuit. This flow achieves the following three novel features: (1) it avoids the tedious and time-consuming spatial variation analysis with other commercial tools like Synopsys PrimeTime static timing analysis (STA) solution[2], (2) it helps designer to meet their specifications particularly for highly-constrained problems by providing an automated flow, and (3) it is the first major change after introducing the spatial variation support for HSpice in Version 2007.09. At present, HSpice becomes an integral tool in different VLSI design flows even for analysing a large circuit. Therefore, using the proposed approach even by using placement information instead of exact device positions improves HSpice accuracy and increase the ability of HSpice for variability analysis.

6. References

[1] HSpice® User Guide: Simulation and Analysis, Version C-2009.03, March 2009, p. 582.
[2] Srivastava, A. and Sylvester, D. and Blaauw, D., *Statistical analysis and optimization for VLSI: timing and power*, Springer, 2005.
[3] Chang, H. and Sapatnekar, S.S., "Statistical timing analysis considering spatial correlations using a single PERT-like traversal," *Proceedings of the IEEE/ACM*

[2] This is one of the features in Synopsys PrimeTime VX tool

International Conference on Computer-Aided Design, ICCAD, 2003, IEEE Computer Society Washington, DC, USA.

[4] Walter Scott, *Magic Tutorial #8*: Circuit Extraction, Special Studies Program, Lawrence Livermore National Laboratory, 1990.