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An Analog Implementation of Early Visual Processing in Insects

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Abstract

An analog VLSI implementation which mimics the early visual processing stages in insects is described. The system is composed of sixty parallel channels of integrated photodetectors and processing elements. It serves as the front end processor for a motion detection chip. The photodetection circuitry includes p-well junction diodes on a 2μm CMOS process and a logarithmic compression to increase the dynamic range of the system. The processing elements consist of an analog differentiator behind each photodetector. The differentiators are low frequency and have been designed using subthreshold design methods.

1 Introduction

Conventional attempts at image acquisition and processing using ordinary video cameras and computers have yielded only limited success in real-time applications. The problem is that the computational cost associated with conventional image processing algorithms prevents real-time machine vision implementations on anything but large-scale expensive digital computers. In recent years, the so-called "smart-sensors" paradigm, in which as much as possible of the signal processing is incorporated into the sensor in order to reduce the transmission bandwidth and subsequent stages of computation, has emerged as a possible competitor to more general-purpose digital vision machines [1,2].

Insects, compared to humans, possess a relatively simple visual system, yet they are capable of performing very complex tasks that are based on vision. The insect visual system has a highly parallel structure and is dominated by a retinoptic organisation. The visual ganglia in the optic lobes are organised into columns and strata. The first optic ganglion, *the lamina*, contains a large number of identical parallel channels. Each channel receives signals from a group of photoreceptors "looking" at the same point in the visual space, and projects outputs to the column lying directly beneath it in the second optic ganglion. For a detailed description of the lamina synaptic pathways see, for example [3].

In addition to sampling of the visual field, the photoreceptors in the retina perform adaptation using a gain control mechanism so that the visual system can function properly under varying lighting conditions. The role of the large monopolar cells, the main output cells of the lamina, is coding of contrast to help the visual system cope better with large variation in background intensity. It is these cells which provide inputs to the motion-detecting neurons of the second neuropil.

In order to obtain motion information both temporal and spatial contrasts are needed. The temporal contrast of an image pixel can easily be obtained in complex video systems using off-sensor-chip processing. In a single chip, however, this becomes a major problem because of the lack of easy access to low speed differentiation or differencing circuits, required for detecting moving objects. Reliable detection of spatial contrast is even more difficult because of mismatch between the devices in adjacent cells and circuits. Moreover, the wide range of intensity in ordinary environments requires a detector with a wide dynamic range to cope well with large intensity variations. Wide dynamic range photodetectors and low frequency analog differentiators have been designed and implemented as part of a motion detection chip.

2 Photoreceptor Circuit

Several kinds of photodetectors are available in a standard CMOS process: the junction diode of the source-drain diffusion, the well-substrate junction, and the parasitic bipolar transistor between the diffusion-well-substrate. The chosen 2μm CMOS process contains p-well on an n-epi layer. The p-well/n-epi junction was chosen for the photodetection, rather than the n^+/p-well junction, due to the greater depth of epi over well – leading to improved quantum efficiency (QE). The choice of an n-substrate process, over a p-substrate option, was not critical for photodetection as the minority carrier diffusion lengths, in both epi and well, are much greater than the epi depth. The choice of epi over a bulk process, is essential for image detection due to the improved Modulation Transfer Function (MTF), which implies a greater ability to detect higher spatial frequency detail. This is illustrated in Fig. 2, where although the diffusion curve

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for 550nm in bulk is acceptable, the MTF for 800nm is severely degraded in bulk compared to epi. Although the diffusion curves are obtained from the well known function of quantum efficiency, the expression for QE in epi was obtained from Ref. [4] which can be readily generalised for QE in a finite slab. The geometrical-only curve, in Fig. 2, is obtained from the usual sinc function expression and represents the ideal case in absence of diffusion effects – we speculate that this could be achieved in GaAs where the unipolar n^+/SI junction collects majority carriers, hence any diffusion terms vanish. Using the usual Plank's Law curve formulation we estimate the responsivity of our p-well/n-epi junction to be 53mA/W, whereas for the GaAs case we obtain 71mA/W. Therefore, in practice, for a scene illumination in the range 10^{-3} to 10^2 W/m^2, we expect a signal current from hundreds of femtoamps to tens of nanoamps, for our silicon element and slightly higher results for GaAs. For future work, GaAs may be promising for cases where demands are made on increasing the processing speed, whilst maintaining low power for mobile applications – as a by-product we would expect an improved MTF and responsivity.

The generated current for the CMOS photodetector structures can be in the range of several pico to several hundred nano amperes. A common circuit to convert this wide range current to a voltage is shown in Fig. 1 [1]. Due to the very low photocurrents, the MOS transistors operate in the subthreshold region, resulting in a logarithmic function. In our design we have used three of these transistors to compensate for the voltage drop of the next stage which is a source follower buffer. With the assumption that all transistors are equal in size and the substrate connections are all connected to the ground voltage, and also assuming that for all transistors the condition $V_{ds} >> kT/q$ is satisfied, the I-V relationship for the current to voltage converter with three MOS transistors can be expressed as:

$$I = \frac{W}{L} I_{D0} e^{\frac{qV}{kT} \frac{1}{n^3+n^2+n}}$$

where I is the input current, V is the output voltage, W and L are the width and length of the transistor, respectively, n is the subthreshold slope factor, and I_{D0} is a process dependent parameter.

3 Differentiator

Temporal and spatial differentiation are the basic functions in a motion detection system. To realise the spatial differentiation, in a single chip, usually the output voltages of two neighbouring photodetectors are applied to a simple differential amplifier.

Temporal differentiation poses problems in the implementation of a monolithic motion detector. The typical time constant required for differentiation of most of the

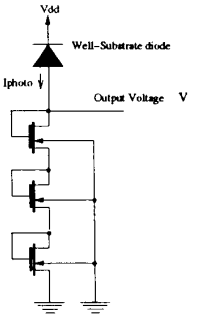

Figure 1: *The current to voltage converter and the photodiode used as the photoreceptor circuit*

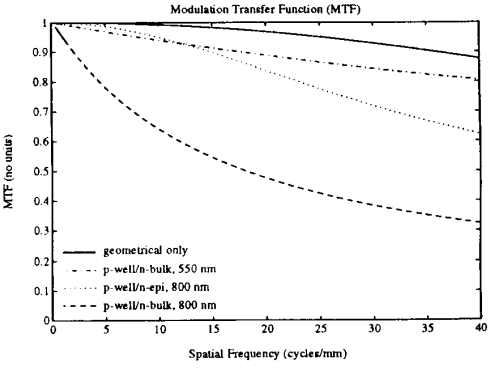

Figure 2: *Theoretical MTF versus spatial frequency. Diffusion-only curves are for specific optical wavelengths. Geometrical-only curve is for the actual 7/20 aperture to pitch ratio used.*

practical movements is in the order of $RC = 10$ms. The highest capacitance available in a VLSI chip is in the order of several picofarads. Therefore, the value of R should be about 10GΩ !

Discrete time differentiation methods, like sample-and-hold or switched-current have the problem of charge injection and more complicated circuitry [5]. Continuous methods, on the other hand, require special circuit design and the use of very high value resistances. The analog realisation of the differentiator can be based on both feedback and feed-forward methods. Feedback methods are preferable as they decrease the necessity for precise matching between the elements. Some of the configurations for implementing the differentiator are shown in Fig. 3.

While either of the circuits in Fig. 3-b and c may be used, the thresholding of the output in Fig. 3-c is more

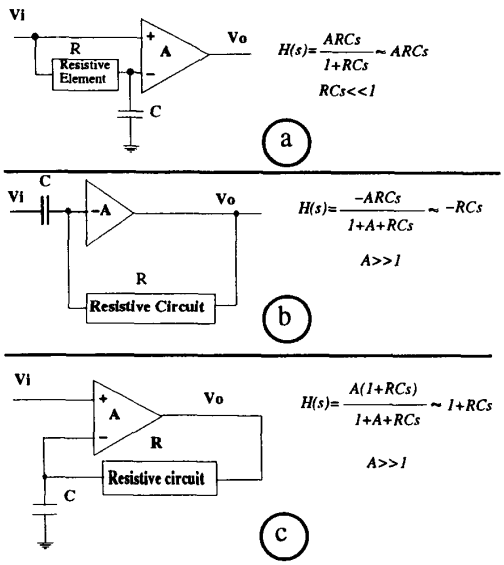

Figure 3: *Three configurations for implementing a simple differentiator: a- feed-forward differentiator with delay line (RC) and a diff-amp. b- feedback differentiator using an inverter as the gain element. c- feedback differentiator using an integrator (RC) in the loop.*

difficult, because of the dependence of the output steady-state voltage on the input current level. However, in circuit 3-b the output steady-state voltage is determined by the DC characteristics of the amplifier (an inverter). The biasing of the inverter based amplifier is automatically accomplished by the active resistor in the highest sensitivity region of the inverter characteristic curve. Also another amplifier (one more inverter exactly the same as the first one) can be used to further enhance the sensitivity of the differentiator. Moreover, thresholding can be done more easily.

The resistive element determines the lowest frequency of differentiation. The passive resistors available in standard processes have very low resistivity compared with our requirements. Active resistors, on the other hand, have limited dynamic range and need large area. Also to produce high value resistors, biasing currents in the order of several picoamperes should be used, introducing other problems like increased mismatch in current mirrors in subthreshold region.

There are several configurations for realising an active resistor. In Fig. 4 the circuit diagram of the an active resistor which is called HRES (Horizontal resistor [1]) is shown. The I-V relationship of this circuit can be expressed as:

$$I = I_{bias} \tanh \frac{qV}{nkT}$$

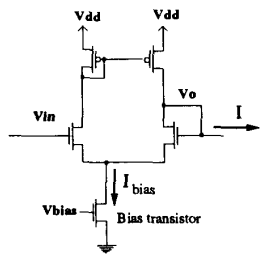

Figure 4: *Circuit diagram of the OTA based active resistor*

where I is the output current, I_{bias} is the biasing current, and V is the voltage across the resistor nodes. The transimpedance of this circuit is determined by the bias current and is $R = kT/qI_{bias}$ in the linear region. Using a bias current of 10pA, R will be about 5GΩ. The linear range of the input voltage is about several kT/q and the output current saturates at $\pm I_{bias}$. This not only causes a non-ideality in the transient operation of the circuit, but also results in a "delaying" problem. If the applied voltage across the resistor exceeds the linear region, the current delivered to the output of the resistor remains constant. If the resistor is connected to a capacitive node the charge or discharge time will be $t = C\Delta V/I_{bias}$. The result of this non-ideality is having larger delays for larger changes of input.

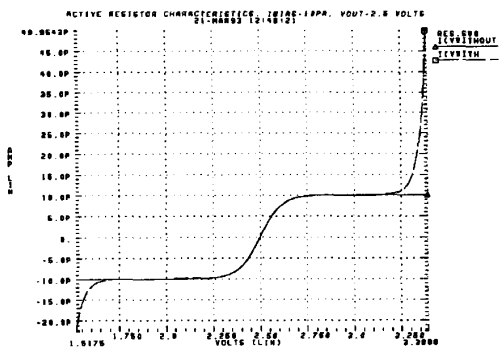

Figure 5: *The I-V characteristics of the active resistor with and without the limiting circuit.*

In order to prevent the saturation of the active resistor, which causes the delay problem, a limiting circuit can be used to inject a large amount of charge to the output of the active resistor. The amount of charge is determined by the characteristics of the limiting circuit. The simplest structures are two back-to-back MOS diodes (MOSTs with gate and source connected together). The characteristics of the active resistor with and without the limiting circuit are shown in Fig. 5. The maximum de-

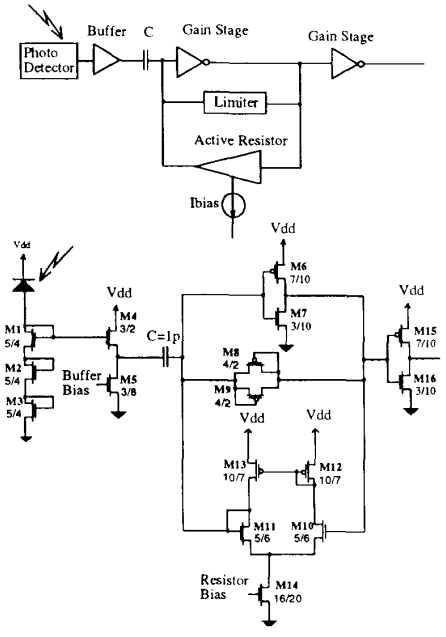

Figure 6: *The schematic of the whole differentiator circuit. The sizes of the transistors W/L are in microns. All the local substrates are connected to relevant supply voltage.*

lay of the circuit in response to large input steps, can be approximated by $t_{max} = CV_{on}/I_{bias}$, where V_{on} is the turn-on voltage of the limiter circuit.

In Fig. 6 the detailed circuit of Fig. 3-b used in the implementation is shown. The response of the circuit to a 10% change in intensity is shown in Fig. 7. This response matches very well to that of large monopolar cells of the fly. These cells reverse the sign of the stimulus contrast and act as a high pass filter or differentiator; their role is coding of contrast [6]. Using p-channel transistors as the limiting circuit the delay will be 3ms, for a bias current of 50pA and a capacitance of 1pF. In practice the bias current should be adjusted to have the maximum sensitivity for a certain application.

4 Template Model Realisation

The circuit presented in Fig. 3-b has been used in the front end of a vision chip based on the insect visual system. The chip architecture is based on the *template model* for motion detection proposed by Horridge [7,8]. In this model the change in temporal contrast is obtained and recorded as one of three states or levels: increase, decrease, and no-change. In the template model the only information used is the presence and direction of motion. The outputs of an array of the proposed circuit are processed in a template model processor. This processor is a special decoder which assigns a set of motion information, like direction and speed of motion, to a set of the changes of temporal contrasts at two neighbouring cells and at two consecutive times. In further layers of processing, other information like range, direction of motion, and time to collision, are extracted. A simplified architecture of the system is illustrated in Fig. 8.

Figure 7: *The response of the circuit to step input. From top to bottom the signals are: 1-The input that has changed by 10% 2-the output of the differentiator 3- the output of the circuit after thresholding.*

5 Physical Design

Sixty of these cells have been used in an array in the front end of a motion detector chip [9]. As parts of the chip are to be illuminated, the active circuits are protected by an opaque *Metal2* layer. The size and pitch of the photodiode in the array was determined by optical requirements of the system like horizontal alignment, geometry and optical characteristics of the lens and optical overlapping of the two neighbouring photodetectors, to be $50\mu m \times 7\mu m$ in area and $25\mu m$ in pitch. In order to reduce the mismatch of the operating points of the cells (mainly the current mirrors) large transistors ($16\mu m \times 20\mu m$) have been used for the biasing transistor in Fig 4. The capacitance has been realised by the poly1-oxide-poly2 linear capacitance structure. In Fig. 9 the layout of the analog processing element containing a photodetector and differentiator is shown. The chip accommodates digital processing parts with the analog array. In order to reduce the induced digital noise, the power supply lines of the analog and digital sections of the circuit have been separated. In Fig. 10 the photomicrograph of the front end processor in the insect vision chip, which contains 22000 transistors, is shown.

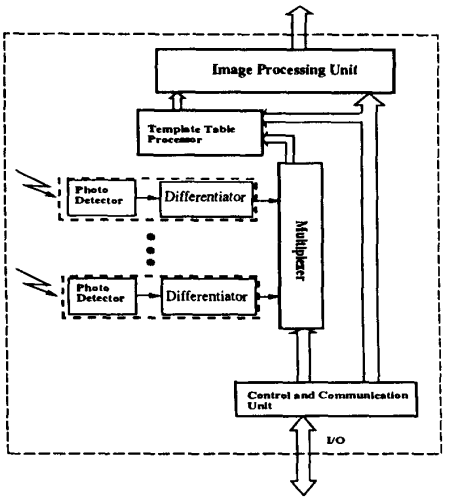

Figure 8: *The architecture of the motion detector based on the template model.*

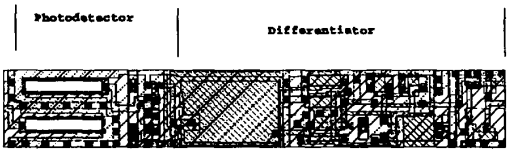

Figure 9: *The layout of the photodetector and differentiator circuits. The size of each cell is 50μm×7μm.*

6 Conclusion

The design of the front end of a motion detector incorporating the Horridge template model was described. Some of the design issues and problems like the step response delay and high value resistive elements were also discussed. Novel circuit design in the weak inversion region of operation has led to a new structure for low frequency differentiation, using simple analog building blocks. The designed circuits were inspired by the insect visual system. They were incorporated in a mixed analog/digital VLSI chip. The chip contains an array of sixty analog processing elements and a digital processor, accommodating more than 22000 transistors in an area of 4.5mm×4.6mm. It has been fabricated in a 2μm double-poly double-metal p-well CMOS process.

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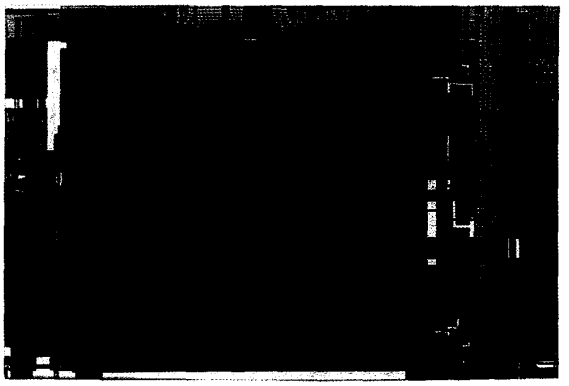

Figure 10: *The microphotograph of the array of the photodetector and differentiator in the motion detection chip.*

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