A Review of 3-D Packaging Technology

Said F. Al-sarawi, *Member, IEEE,* Derek Abbott, *Member, IEEE,* and Paul D. Franzon, *Member, IEEE*

Abstract— **This paper reviews the state-of-the-art in three-dimensional (3-D) packaging technology for very large scale integration (VLSI). A number of bare dice and multichip module (MCM) stacking technologies are emerging to meet the ever increasing demands for low power consumption, low weight and compact portable systems. Vertical interconnect techniques are reviewed in details. Technical issues such as silicon efficiency, complexity, thermal management, interconnection density, speed, power etc. are critical in the choice of 3-D stacking technology, depending on the target application, are briefly discussed.**

Index Terms— **Bare dice stacking, MCM stacking, 3-D MCM technology, 3-D packaging, vertical interconnection.**

I. Introduction

As the complexity of portable electronic systems increases, such as in the shift from the mobile phone toward the Interactive Mobile Multimedia Personal Communicator (IM^{3}PC) paradigm [1], greater demands are being placed on the production of low power, low weight and compact packaging technologies for VLSI integrated circuits. Likewise many aerospace and military applications are following this trend. In order to meet this demand, many new three-dimensional (3-D) packaging technologies are now emerging where either bare dice or MCM's are stacked along the z-axis, resulting in dramatic improvement in compactness. As this z-plane technology results in a much lower overall interconnection length, parasitic capacitance and thereby system power consumption can be reduced by as much as 30% [2].

Section II will discuss the advantages of 3-D packaging technology and its effect on system performance. Section III will provide a brief discussion of the different vertical interconnection methods used in 3-D packaging, while Section IV will address the limitations of the 3-D technology.

II. Advantages of 3-D Packaging Technology

The following subsections discuss briefly how 3-D packaging technology enhances system performance and provides performance factors that cannot be achieved using conventional packaging technologies.

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S. F. Al-Sarawi and D. Abbott are with the Centre for High Performance Integrated Technologies and Systems (CHiPTec), Department of Electrical and Electronic Engineering, The University of Adelaide, Adelaide 5005, South Australia (e-mail: alsarawi@eleceng.adelaide.edu.au; dabbott@eleceng.adelaide.edu.au).

P. D. Franzon is with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695 USA (e-mail: paulf@eos.ncsu.edu).

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A. Size and Weight

By replacing single chip packages with a 3-D device, substantial size and weight reductions are achieved. The magnitude of these reductions depends, in part, on the vertical interconnection density and accessibility, which will be discussed in Section II-G, thermal characteristics, and robustness required. It has been reported that 40 to 50 times reduction in size and weight is achievable using 3-D technology compared to conventional packaging. As an example, volume and weight comparisons between TI's 3-D bare dice packaging and discrete and planar packaging (MCM) are presented in Tables I–VII. It is evident from these tables that a five to six times reduction in volume is possible over MCM technology and a ten to 20 times reduction over discrete packaging technology. Moreover, a two to 13 times reduction in weight is also achievable compared to MCM technology and a three to 19 times reduction compared to discrete components. All of these reductions result from eliminating the overhead weight and size associated with conventional technologies. Furthermore, in the case of the Aladdin parallel processor [3], the reduction in size and volume against the Cray X-MP benchmark was by about 660 and 2700 times, respectively.

B. Silicon Efficiency

One of the main issues in packaging technology is the chip footprint, which is the printed circuit board area occupied by the chip [5] as defined in Fig. 1. In the MCM case, the footprint is reduced by 20–90% because of the use of bare dice. Three-dimensional packaging results in a even more efficient utilization of silicon real estate, which is referred to as "silicon efficiency." We can define silicon efficiency as the ratio of the total substrate area in a stack to the footprint area. Consequently 3-D technology exceeds a 100% silicon efficiency compared to other two-dimensional (2-D) packaging technologies.

C. Delay

Delay refers to the time required for a signal to travel between the functional circuit blocks in a system. In high speed systems, the total delay time is limited primarily by the time of flight, which is defined as the time taken for the signal to travel (fly) along the interconnect [6]. The time of flight, t, is directly proportional to the interconnect length. So reducing the delay requires reducing the interconnect length which is the case when using 3-D packaging, as shown in Fig. 2. The resultant reduction in interconnect length, results in a reduction of the interconnect associated parasitic capacitance and inductance, hence reducing signal propagation delays. For example, the signal delay as a result of using MCM's is reduced by about 300%. Furthermore, the delay would be less in case of 3-D

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TABLE I
3-D MASS MEMORY VOLUME AND WEIGHT COMPARISONS BETWEEN OTHER TECHNOLOGIES AND TEXAS 3-D TECHNOLOGY IN cm^3/Gbit [4]

	Type	Capacity	Discrete	2D	3D	Discrete /3D	2D /3D
Weight	SRAM	1 Mbit	1678	783	133	12.6	5.9
		4 Mbit	872	249	41	21.3	6.1
	DRAM	1 Mbit	1357	441	88	15.4	5.0
		4 Mbit	608	179	31	19.6	5.0
		16 Mbit	185	69	69	16.8	6.2
Volume	SRAM	1 Mbit	3538	2540	195	18.1	13.0
		4 Mbit	1588	862	145	10.9	5.9
	DRAM	1 Mbit	2313	1542	132	17.5	11.6
		4 Mbit	862	590	113	7.6	5.2
		16 Mbit	363	227	113	3.2	2.0

TABLE II
A LIST OF MOST OF THE COMPANIES AND INSTITUTIONS WORKING IN THE AREA OF 3-D PACKAGING [78]

Bare Die stacking		Packaged Die stacking	
Standard ICs	Custom ICs	Standard Package	Custom Package
Actel	IBM	Mitsubishi	CTS
Implex	Irvine Sensors	Thomson-CFS	Dense-Pac
Matsushita (MEI)	Fujitsu	Samsung Electronics	Grumman
Thomson-CFS	Hughes	Texas Instruments	Harris
Hitachi & Intel	Texas Instruments	nChip, Inc.	Hitachi
Valtronic, Inc.	Matsushita	NEC Corp.	Motorola
AT&T		Irvine Sensors	RTB Technology
		Cray Research, Inc.	Staktek
		Harris	Trymer

TABLE III
TABLE II CONTS

MCM stacking	Wafer stacking
Custom Modules	Custom Wafers
AT&T	Mass Memory Technology
Raytheon (E-Systems)	Hughes
General Electric	ATT
Hughes	NTT and Thomson-CSF
Matra Marconi Space	General Electric &
Matsushita (MACO)	USAF Philips Lab.
Motorola	Cubic Memory
Honeywell and Coors	
RCMT@Berlin Uni	
Lockheed	
Jet Propulsion Lab.	

technology because the electronic components are in close proximity to each other, as shown in Fig. 2.

D. Noise

Noise in general can be defined as unwanted disturbances superimposed upon a useful signal, which tend to obscure its information content. In high performance systems, noise management is a major design issue. Noise can limit the achievable system performance by degrading edge rates, increasing delays, and reducing noise margins and can cause false logic switching. The noise magnitude and frequency are closely tied to the packaging and interconnect scheme used. In a digital system four major sources of noise can be identified as:

1) reflection noise;
2) crosstalk noise;
3) simultaneous switching noise;
4) electromagnetic interference (EMI) [7].

The magnitude of all of these noise sources depends on the rise time of the signals passing through the interconnect. The faster the rise time, the worse the noise. The role of 3-D technology in reducing noise is in the reduction of interconnection length, and hence reduction of the associated parasitics which translate into performance improvements. On

TABLE IV
AN EVALUATION OF COMPANIES WHICH PROVIDE PERIPHERY INTERCONNECTION BETWEEN STACKED IC'S

Company	Application	Country	Interconnection Technique
Matsushita	Memories	Japan	Stacked TAB carrier (PCB)
Fujitsu	Memories	Japan	Stacked TAB carrier (leadframe)
Dense-Pac	Memories	USA	Solder dipped stacks to create vertical conductors on edge
Micron Technology	Memories	USA	Solder filled holes in chip carriers and spacers
Hitachi	Memories	Japan	Solder connections between plated through hole
Irvine Sensors	Memories/ASICs	USA	Thin film 'T-connects' and sputtered metal conductors
Thomson-CFS	Memories/ASICs	France	Direct laser write traces on epoxy cube face
Mitsubishi	Memories	Japan	PC boards soldered on two sides of TSOP packages
Texas Instruments	Memories/ASICs	USA	Array of TAB leads soldered to bumps on silicon substrate
Grumman Aerospace	ASICs	USA	A flip-chip bonded to faces of the stack
General Electric	ASICs	USA	Folded flex circuits
Harris	ASICs	USA	Folded flex circuits
MCC	ASICs	USA	Folded flex circuits
Matra Marconi	Memories	France	Wire bonded to an MCM substrate directly
Voltonic	ASICs	USA	Wire bonded to a substrate through an IC

TABLE V
AN EVALUATION OF COMPANIES WHICH PROVIDE AREA INTERCONNECTION BETWEEN STACKED IC'S

Company	Application	Country	Interconnection Technique
Fujitsu	ASIC	Japan	Flip-chip bonded Stacked Chips without spacers
University of Colorado & UCSD	Optoelectronic	USA	Flip-chip bonded Stacked Chips with spacers
Hughes	ASIC	USA	Microbridge springs and thermomigration vias

TABLE VI
AN EVALUATION OF COMPANIES WHICH PROVIDE PERIPHERY INTERCONNECTION BETWEEN STACKED MCM'S

Company	Application	Country	Interconnection Technique
Matsushita	Memories	USA	Solder leads on stacked MCMs
General Electric	ASIC	USA	HDI-thin film interconnect laminated to side of stack
Harris	Memories	USA	Blind castellation interconnection
CTS Microelectronics	Memories	USA	Blind castellation interconnection
Trymer	Guidance Systems	USA	Solder dipped stacks to create vertical conductors on edge

TABLE VII
AN EVALUATION OF COMPANIES WHICH PROVIDE AREA INTERCONNECTION BETWEEN STACKED MCM'S

Company	Application	Country	Interconnection Technique
Raytheon (E-Systems)	ASIC	USA	Fuzz buttons in plastic spacer and filled vias in substrate
Technical University of Berlin	ASIC	Germany	Elastomeric connectors with electrical feedthroughs
AT&T	ASIC / multi-processor array	USA	Compliant anisotropic conductive material
Hughes	ASIC / avionics	USA	Microbridge springs and thermomigration vias
Motorola	Not in Use	USA	Solder balls on top and bottom of substrate layers
Micron Technology	Memories	USA	Stacked silicon wafers with filled vias
Lockheed	ASIC / IR processors	USA	Stacked silicon wafers with filled vias

parasitics which translate into performance improvements. On

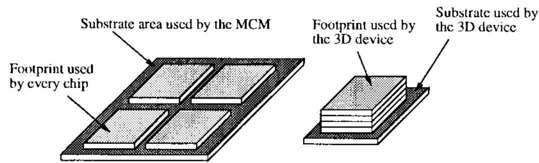

Fig. 1. A graphical illustration of the silicon efficiency between MCM's and 3-D technology.

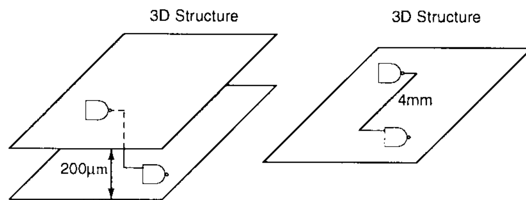

Fig. 2. A comparison between the wiring lengths in 2-D and 3-D structures [79].

the other hand, the noise could be problematic in a system if the used 3-D technique does not address the noise. For example, if the interconnections have not got a uniform impedance along the line or its impedance does not match the source and destination impedance, there is the potential for reflection noise. Furthermore, if the interconnects are not spaced enough there is also a potential for crosstalk noise. Simultaneous is reduced because of the shortened interconnects and consequent reduction of the associated parasitics, so producing less simultaneous noise for the same number of interconnections.

E. Power Consumption

In an electronic system the energy dissipated, E, due to the interconnect parasitic capacitance, C, is given by, $E = CV^2$, and therefore the power consumption is $P = fCV^2$, where V is the voltage swing across the C and f is the number of transitions per second. As the parasitic capacitance is proportional to the interconnection length, the total power consumption is reduced because of the reduced parasitics. For example, let us say that 10% of the system power consumption is dissipated in the interconnects when mounted on a PWB. If the product was implemented using MCM technology, the power consumption will be reduced by a factor of five. Hence, the product would consume 8% less power than the PWB-base product [8]. Furthermore, when such a product is implemented using 3-D technology the saving will be much more because of the reduced interconnect length and the associated parasitics.

F. Speed

The power saving achieved using 3-D technology can allow the 3-D device to run at a faster rate of transitions per second (frequency) with no increase in power consumption. In addition, the reduction in parasitics (capacitances and inductances), size and noise of a 3-D device, allow for higher transitions per second which would increase the overall system performance. For example, the Aladdin parallel processor, achieved 35 000 and 10 800 in MIPS and FLOPS per unit volume improvement over the Cray X-MP as a result of integration using 3-D MCM technology [3].

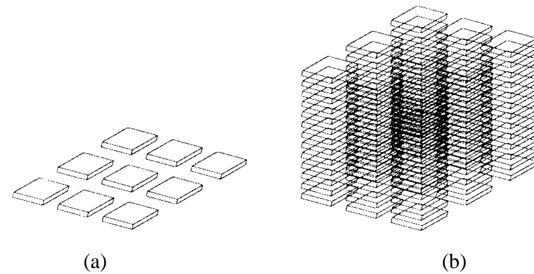

Fig. 3. A comparison between 2-D and 3-D packaging interms of the accessability and useablity of interconnection.

G. Interconnect Usability and Accessibility

The use of a 3-D packaging configuration provides access to 116 neighbors within an equal interconnect length to a centre element in the stack, in contrast to eight neighbors to the centre element in the case of 2-D packaging technology, while assuming a typical die thickness of 0.6 mm [9], [10] as illustrated in Fig. 3. Hence, reduction of the interconnect length in the stack results in reduction of propagation delay between chips. Furthermore, the available vertical interconnection results in maximum utilization of the available interconnects in contrast to traditional packaging technologies where such utilization is limited by physical structures such as vias or holes or by previously routed interconnects (Fig. 4). The accessibility in case of 3-D packaging technology depends on the type of vertical interconnection employed as it is proportional to the available vertical interconnect density—which is defined as the number of signal layers per average wire pitch [11], [12]. So, area interconnection provides the most accessibility and usability in contrast to peripheral interconnections, where the usability and accessibility are limited by the periphery length of the stacked element.

H. Bandwidth

Interconnect bandwidth, especially memory bandwidth, is often the performance limiter in many computing and communications systems. Thus low latency (delay) and wide buses are very desirable. For example, in the well known Intel Pentium Pro, the CPU and Level 2 cache are packaged together in the same multi-cavity Pin Grid Array to obtain a large memory bandwidth. The exciting possibility is whether 3-D packaging technologies can be used to integrate a CPU and memory chips while avoiding the cost of the multicavity Pin Grid Array.

III. Vertical Interconnections in 3-D Electronics

Vertical Interconnections [13], [14] refer to the interconnections needed to route power, ground, and signals to the layers within the 3-D Module. The following subsections will describe briefly the different types of vertical interconnections.

A. Periphery Interconnection Between Stacked ICs

The following subsections will list interconnection techniques used to interconnect stacked chips using the stack periphery.

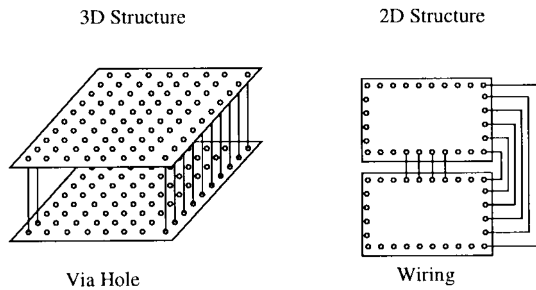

Fig. 4. A comparison between 3-D and 2-D structures in terms of the possible number of interconnections assuming one routing layer for the 2-D structure [79].

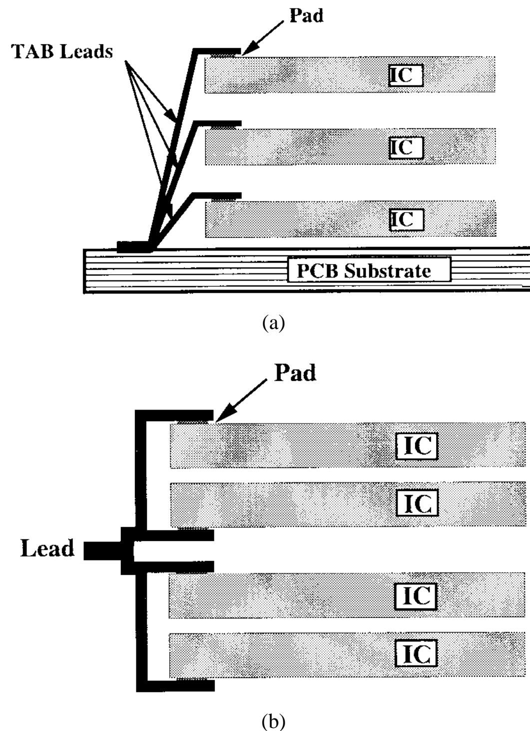

Fig. 5. Two variants of the stacked tape carrier vertical interconnect: (a) stacked TAB on PCB and (b) stacked TAB on leadframe.

1) Stacked Tape Carrier: Stacked tape carrier is a method for interconnecting IC's using TAB technology. This method could be divided further into stacked TAB on PCB and stacked TAB on leadframe as illustrated by the schematic diagram shown in Fig. 5. The TAB on PCB method is used by Intel Japan [15] and Matsushita Electric Industrial Company [16], [17], [18]. In Matsushita's case, they used this approach for designing high density memory cards. The second method is used by Fujitsu in designing DRAM chips [19], [20].

2) Solder Edge Conductors: Solder edge conductor bonding is a process where vertical interconnections between IC's are performed by soldering edge conductors. There are four variants of this method as follows.

a) *Solder dipped stacks to create vertical conductors on edge:* In this approach, the leads of the stacked IC's that are to be connected, are brought into contact using a static molten solder bath and simultaneously soldered. A schematic diagram on how such interconnections are performed is shown in Fig. 6(a). This method is used by Dense-Pac for designing high density memory modules [21], [22], [23].

b) *Solder-filled holes in chip carriers and spacers:* In this approach the vias are filled with a conductive material to interconnect the stacked IC using carriers and spacers as shown in Fig. 6(b). This method is used by Micron Technology in designing DRAM and SRAM chips [24]. A similar technique was developed and patented by Hughes Electronics [25].

c) *Solder connections between plated through-hole:* In this approach the IC leads are brought by TAB then interconnected using a small PCB called a PCB frame, which has vias through it. The vertical interconnections are achieved using these vias and by stacking these frames using a solder joint bonding technique as shown in Fig. 6(d). Hitachi has developed this method and used it in the design of high density DRAM's [26].

d) *Edge array solder balls:* In this approach, solder balls are placed along the edge of the chip and the chip is edge mounted on the substrate using solder reflow. For example, Hughes achieved this by dicing through the solder ball [27]. MCNC has achieved this by shaping the solder ball so that it "overhangs" the chip edge [28]. MCNC is also capable of rerouting the pads to the edge of the chip as shown by the photograph of an early prototype in Fig. 7.

3) Thin Film Conductors on Face-of-a-Cube: A thin film is a layer of conductive material either sputtered or evaporated onto a substrate in a vacuum to form conductors. 'Thin film conductors on face-of-a-cube' is a method where vertical interconnections are performed on the cube face. There are two variants of this method as follows.

a) *Thin film "T-connects" and sputtered metal conductors:* This method was jointly developed by Irvine Sensors and IBM. In this method, after the I/O signals are rerouted to one edge of the chip, a thin film metal layer is patterned on the surface of the stacked chips. Then, two processes, called lift-off photolithography and sputter-deposition, are performed on the face of the stack to form pads and buslines, creating what is called "T-connections" [29] as shown in Fig. 8.

b) *Direct laser write traces on epoxy cube face:* In this method, the interconnect pattern on the sides of the cube is generated by laser trimming. This pattern is designed to intersect with the IC's wires cross section on the face of the cube [30], [31] as shown in Fig. 9. This method is used by Thomson-CFS DOI for high density memories [30], microcameras [32], [33], medical applications and smart munitions [34], [31].

4) An Interconnection Substrate Soldered to the Cube Face: In this method a separate substrate is soldered to the face of the cube as will be explained by the following variants of the method.

a) *Array of TAB leads soldered to bumps on silicon substrate:* This method was developed and used by Texas Instruments in the design of very high density memories [35], [36], [37]. The vertical interconnections are

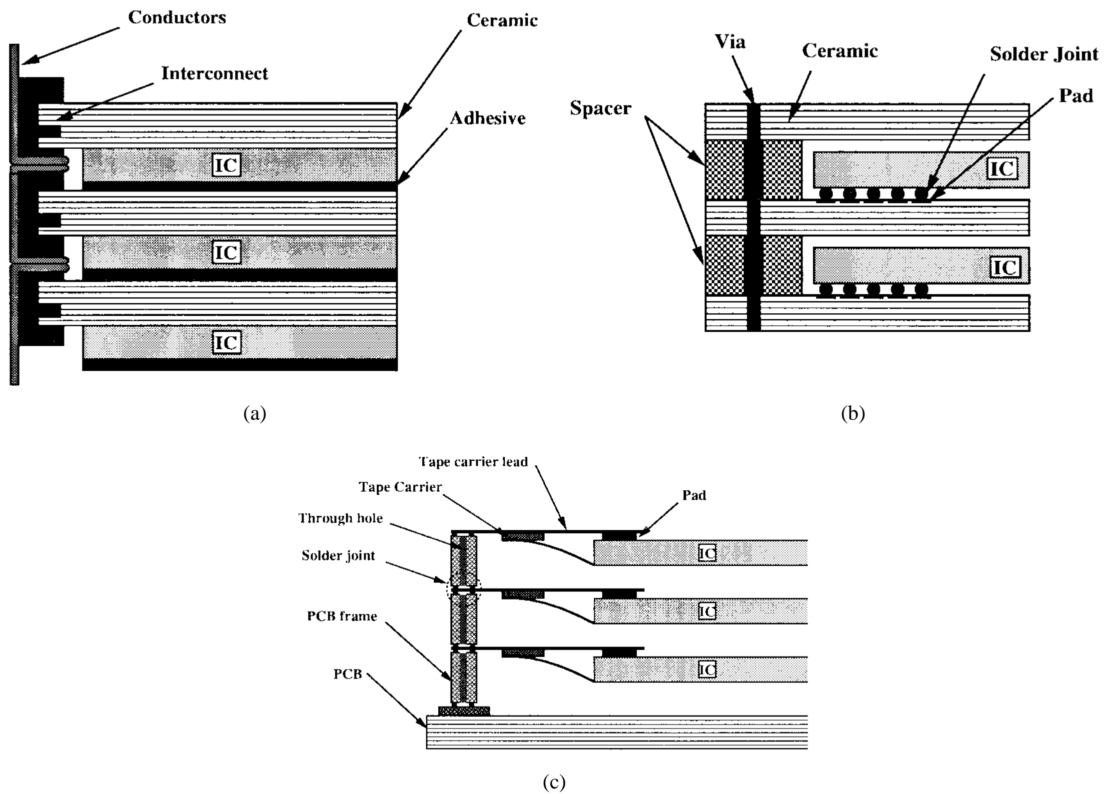

Fig. 6. Three variants of the solder edge conductors vertical interconnections: (a) solder edge contacts, (b) solder filled via, and (c) stacked PCB leadframes.

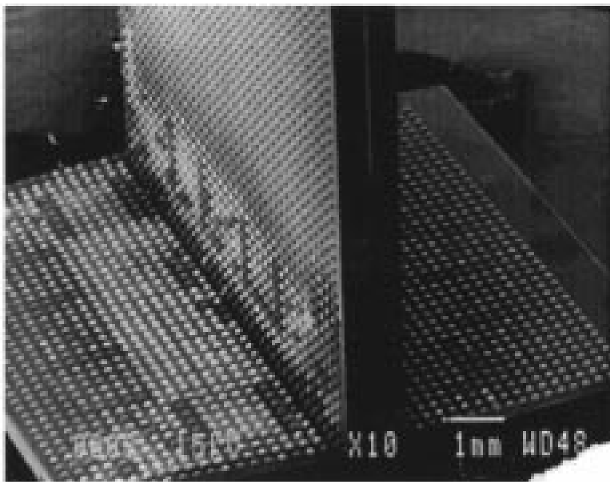

Fig. 7. A photograph of an edge array with solder balls fabricated at MCNC.

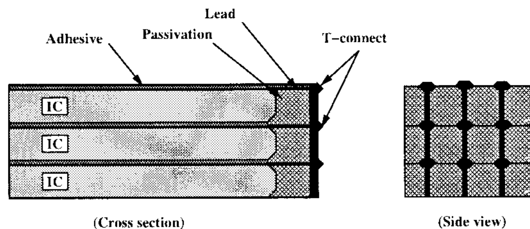

Fig. 8. Thin film metal "T-connects" for vertical interconnections.

achieved by rerouting the memory chip I/Os for TAB bonding. Then, a group of four to 16 of these chips is laminated to form the 3-D stack. These stacks are

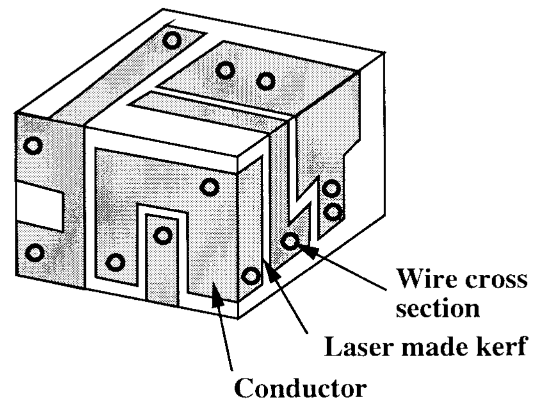

Fig. 9. Direct laser writing process for vertical interconnections.

placed on a silicon substrate and aligned such that the TAB leads on the bottom of the stack contact the solder bumped pads on the substrate as shown in Fig. 10.

b) *A flip-chip bonded to faces of the stack:* In this method, before MCM's are stacked their interconnection leads are brought to the side to a metallic pad. Then an IC is bonded to these metallic pads using flip-chip technology as shown in Fig. 11. This approach was used by Grumman Aerospace corporation to develop surveillance technology for military applications [38], [39].

c) *PC boards soldered on two sides of TSOP packages.* In this approach, two PCB's are soldered on two sides of stacked TSOP packages to perform the vertical interconnections. Then, the PCB leads are configured to form a dual in line package (DIP) as shown in Fig. 12. This

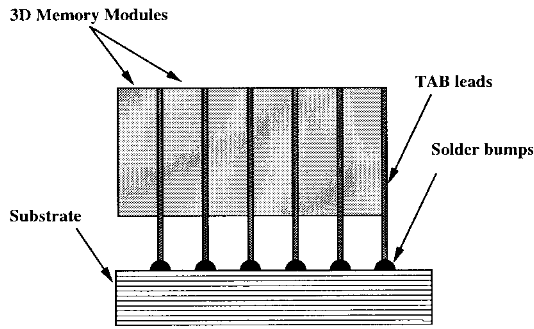

Fig. 10. Texas Instruments array TAB leads soldered to bumps on a silicon substrate.

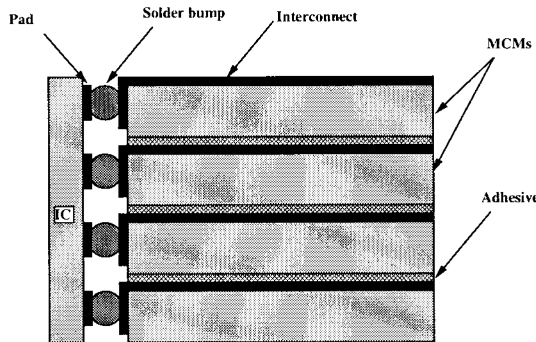

Fig. 11. Vertical interconnection method where a chip is flip bonded to the side of the stacked MCM's.

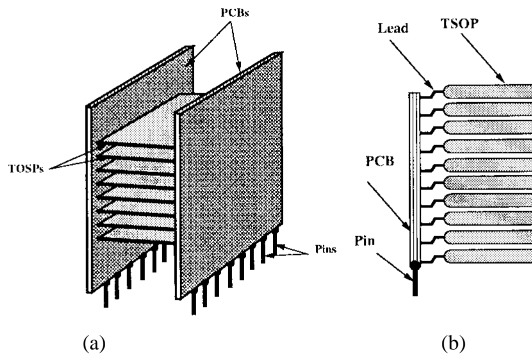

Fig. 12. (a) Schematic diagram of a PCB solder to TSOP's and (b) a cross sectional view of the upper schematic.

method is used by Mitsubishi in designing high density memories [40].

5) Folded Flex Circuits: In the folded flex circuits, bare dice are mounted and interconnected on a flex type material, then folded to form a 3-D stack [41] as shown in Fig. 13. This method is reported by General Electric, Harris, and MicroModule Systems.

6) Wire Bonded Stacked Chips: The "wire bonded stacked chips" method uses a wire bonding technique for the vertical interconnections. There are two variants for this approach:

a) *Wire bonded to an MCM substrate directly:* In this approach, stacked chips are wire bonded to a planar MCM substrate using wire bonding technology as shown in Fig. 14. This approach was used by Matra Marconi Space for a high density solid state recorder [42] and by nChip in the design of high density memory modules [43].

b) *Wire bonded to a substrate through an IC:* In this approach, there is a mother and a daughter chip. The mother chip will act as a substrate for the daughter chip, where interconnections from the daughter chip go to pads on the surface of the mother chip substrate as shown in Fig. 15. Voltonic USA has used this technology in some medical applications [44].

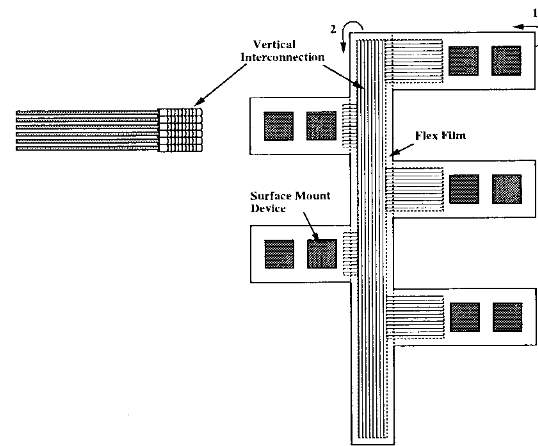

Fig. 13. Schematic diagram showing how IC's are stacked and interconnected using a flex type material.

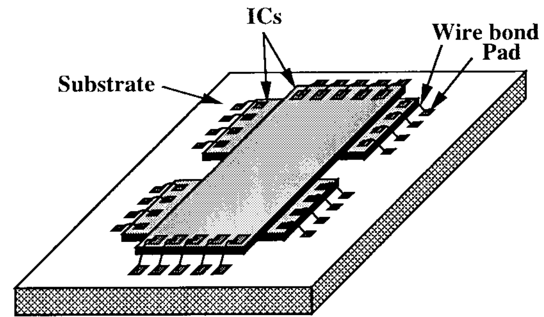

Fig. 14. Vertical interconnection approach using wire bonding techniques.

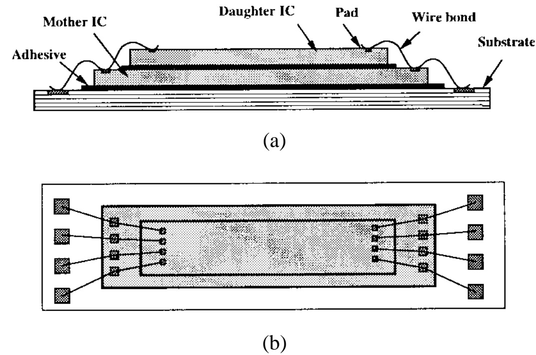

Fig. 15. (a) Schematic diagram of two chips stacked and interconnected using wire bonding and (b) a top view of the upper schematic diagram.

B. Area Interconnection Between Stacked ICs

An area interconnection is a method where vertical interconnections are not bonded to the periphery of the stacked elements, as will be illustrated by the following variant of this method.

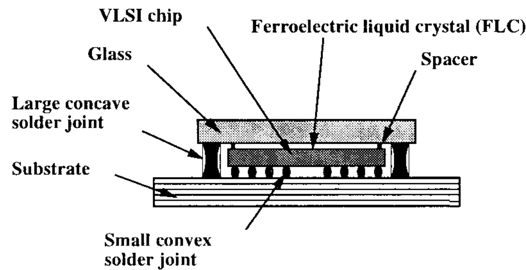

Fig. 16. Schematic diagram of two chips stacked using flip-chip technology.

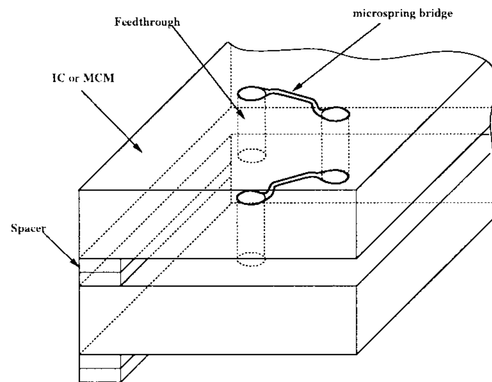

Fig. 17. Schematic diagram of Hughes microspring vertical interconnect method.

1) Flip-Chip Bonded Stacked Chips Without Spacers: In this approach the stacked IC's are flipped and interconnected to either a substrate or another chip using the solder joint technology. This technique was used by many companies, some of these companies are IBM company in the design of ultra-high-density components [45], Fujitsu for stacking a GaAs chip on a CMOS chip technology [46] and Matsushita which developed a new "micro-bump bonding method" [47] and used by Semiconductor Research Center, Osaka, Japan, for thermal heads and an LED printer head [48].

2) Flip-Chip Bonded Stacked Chips With Spacers: This approach is similar to the above approach except that spacers are used to control the distance between the stacked chips. This technique was developed and used by University of Colorado, Boulder, and University of California, San Diego, to fix a glass plate containing a ferroelectric liquid crystal on the top of the VLSI chip [49], [50] as shown in Fig. 16.

3) Microbridge Springs and Thermomigration Vias: Microbridge springs method involves the use of microsprings to achieve the vertical interconnections between stacked IC's, as shown in Fig. 17. This method was developed and used by Hughes in the design of 3-D parallel computers for real time data and image processing and avionics for F-14, F-15, F/A-18, AV-8B, and B-2 aircrafts [51]. The same technique can be used for MCM's and is also relevant to the methods presented in Section III-D1.

C. Periphery Interconnection Between Stacked MCMs

This is a method where vertical interconnections between stacked MCM's are realized on the stack's periphery. There are three main variants of this method as follows.

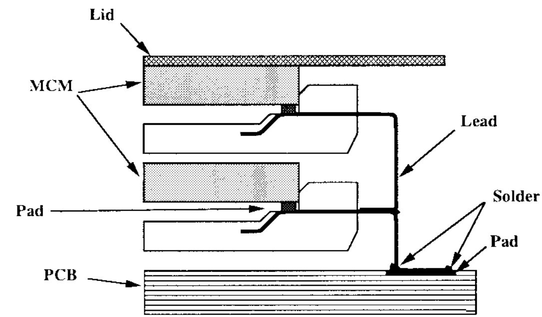

Fig. 18. A soldered leads on stacked MCM's vertical interconnection method, which is a variant of the solder edge conductors method discussed in Section III-A2.

1) Solder Edge Conductors: This is similar to the solder edge conductor for IC's, discussed in Section III-A2. However, in this case the vertical interconnections are performed between MCM's rather than IC's. There are two variants of this method.

a) *Solder dipped stacks to create vertical conductors on edge:* This technique is similar to the solder dipped stacks to create the 'vertical conductors on edge' technique discussed in Section III-A2 with the exception that MCM's are used to form the stack. This technique was used by Trymer in the development of a guidance system for hypervelocity projectiles [52], [53].

b) *Solder leads on stacked MCMs:* After each MCM is packaged separately they are stacked with the leads formed to allow stacking as shown in Fig. 18, then soldered for permanent mounting. Matsushita Electronic Components has used this method in the design of high density SRAM's and DRAM's by using 2–8 layer stack. This method is referred to as 'Stacked QFP-format MCMs' because the leads on the bottom board are formed as a quad-flat pack package [54].

2) Thin Film Conductors on Face-of-a-Cube:

a) *HDI-thin film interconnect laminated to side of stack:* The vertical interconnects are realized along the sides of the stack using the same high density interconnect (HDI) process used in the substrate. The sides are laminated then patterned using a chemical process called "electroplated photoresist." A schematic diagram of this method is shown in Fig. 19. This technique was developed and used by General Electric in the design of high density memories and other application specific integrated circuits (ASIC's) [55], [56].

b) *Direct laser write traces on epoxy cube face:* This method of interconnection is similar to the one discussed in Section III-A3 except that MCM's are used in the stack instead of IC's. Thomson-CFS is the company who developed this technology for both MCM and IC stacking and called it "MCM-V."

3) Blind Castellation Interconnection: In this approach a semicircular or crown-shaped metallised surface (Castellation) is used for making vertical interconnections between the stacked MCM's as shown in Fig. 20. This method was used by

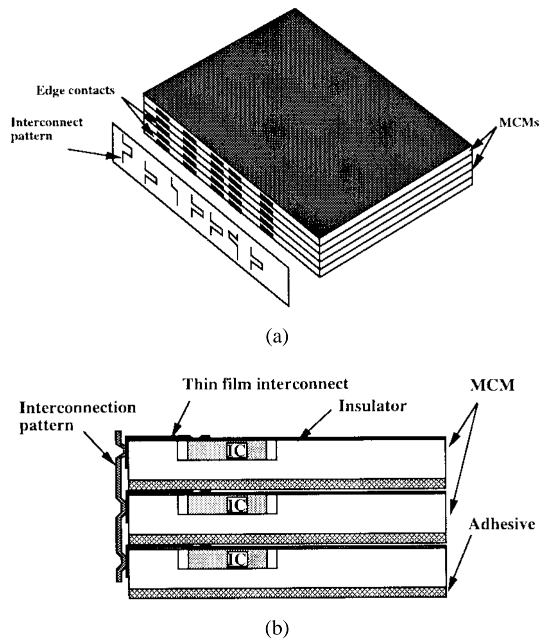

Fig. 19. (a) GE method for stacking MCM's with edges interconnected on the sides of the cube; (b) cross-sectional view of (a).

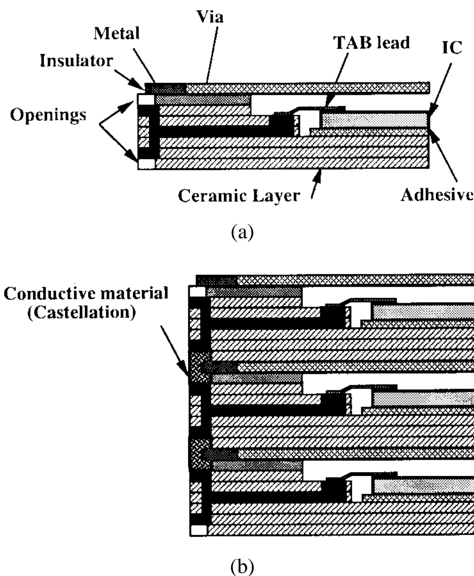

Fig. 20. (a) Schematic diagram of an MCM with the blind castellation method and (b) a schematic diagram of three MCM's stacked using the blind castellation method.

Harris and CTS Microelectronics in the design of high density memory modules [57], [58], [59].

4) Wire Bonded Stacked MCMs: This approach is similar to the wire bonded stacked chips technique discussed in Section III-A6, except MCM-Ds are used in the stack. This approach was developed and used by CENG for designing a 1 Gb mass memory module [60].

5) Elastomeric Connectors: This approach uses elastromeric connectors[1] to vertically interconnect stacked MCM's. Such approach is currently employed by the Jet Propulsion Laboratory in the implementation of a Space-Cube—a multiprocessor architecture using 3-D MCM [61].

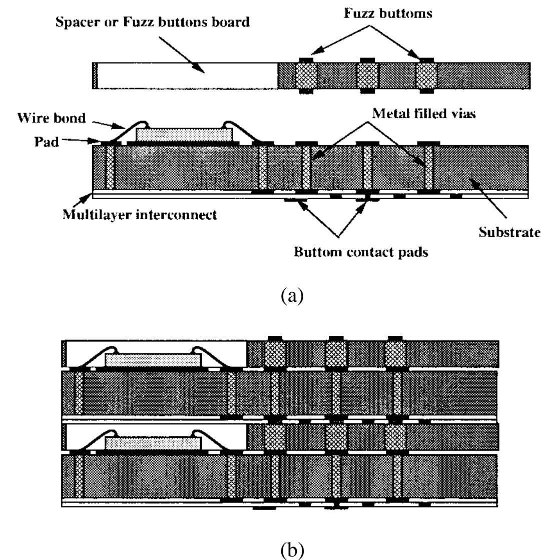

Fig. 21. (a) Schematic diagram for an arrays of contacts between MCM's with through-hole via and (b) two MCM's are stacked by applying a mating force.

D. Area Interconnection Between Stacked MCMs

This is a method where the interconnections between stacked MCM's are not bonded to the stack periphery. Such methods provide higher interconnection density between stacked elements. The following are variants of such vertical interconnections:

1) Arrays of Contacts Between MCM's With Through Hole Vias: In this method, an array of contacts are used to provide the vertical interconnections between stacked MCM's. There are six variants of this method as follows.

a) *Fuzz buttons in plastic spacer and filled vias in substrate:* In this method MCM's are stacked with an intermediate layer called the spacer or fuzz buttons board [62]. This layer has a precision plastic spacer to provide clearance for chip and bond, and fuzz buttons to provide interconnection by applying a mating force on the stacked MCM's as shown in Fig. 21. Fuzz buttons are physically made of fine gold "wire wool" and the integrity of a contact made by the contact of two of these wool pads is surprisingly good. This method is developed by E-Systems

   and used by E-Systems and Norton Diamond Film for stacking MCM's with diamond substrates [9], [63], [64] and also used by Irvine Sensors in a low cost compact DSP [65].

b) *Elastomeric connectors with electrical feedthroughs:* The vertical interconnections in this method are implemented by a combination of "electrical feedthroughs" and elastomeric connectors. The "electrical feedthroughs" are premanufactured elements[2] that are mounted into a laser structured substrate by

[1] An elastomer is a plastic material that at room temperature can be stretched repeatedly to at least twice its original length and, upon release of the stress, will return with force to its approximate original length.

[2] These elements are small silicon strips taken from a processed wafer, carrying straight, parallel conductor lines inside a polymer dielectric on both sides, then cut into strips orthogonal to the metal fibers.

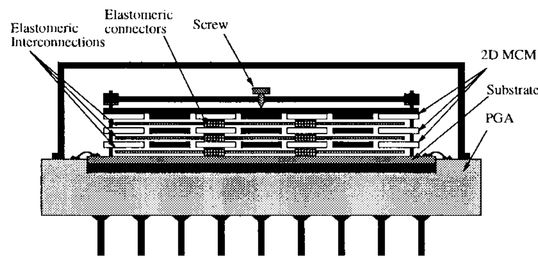

Fig. 22. Schematic diagram of TUB stacking technology showing the uses of elastomeric connections for vertical interconnections [14].

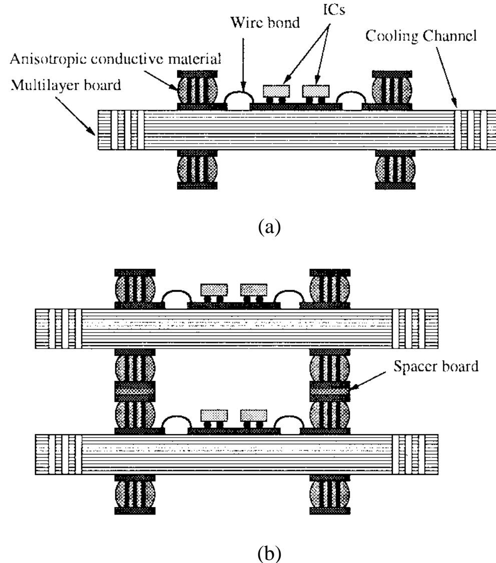

Fig. 23. (a) Schematic diagram of a vertical interconnection approach using an anisotropic conductive material and (b) shows two MCM's stacked using this method.

an embedding technique. A schematic diagram of this method is shown in Fig. 22. This method was developed by the Research Center of Microperipheric Technologies at the Technical University of Berlin [15], [14]. In addition, Texas Instrument has developed a variant of this method in the design of a high performance parallel computer called the "Aladdin Parallel Processor" [3].

c) *Compliant anisotropic conductive material:* This method uses an anisotropic conductive material that is electrically conductive through its thickness, but nonconductive in its length and width. A spacer is used to provide additional interconnections, clearance for wirebond loop height, and cooling channel height as shown in Fig. 23. This method was developed and used by AT&T in the design of a 1 GFLOP multiprocessor array using 3-D MCM technology [66].

d) *Microbridge springs and thermomigration vias:* Refer to Section III-B3 for the technique description.

e) *Solder balls array on top and bottom of substrate layers:* This method involves using a solder balls array on the top and bottom of a substrate to provide the vertical interconnect. The bottom balls are used to interconnect the stacked MCM's to a PCB by applying pressure on the stack, while the top solder joints are used to provide interconnection between the stacked MCM's as shown in Fig. 24 [67], [68]. This method has been patented by Motorola but has not been used in production.

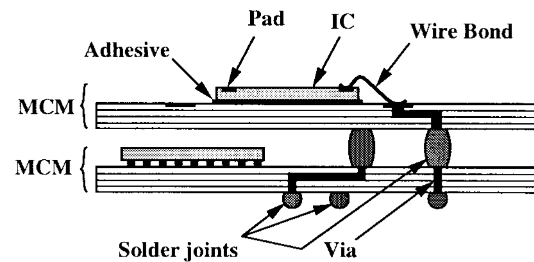

Fig. 24. Stacked MCM's using solder balls arrays on top and button of substrate layers.

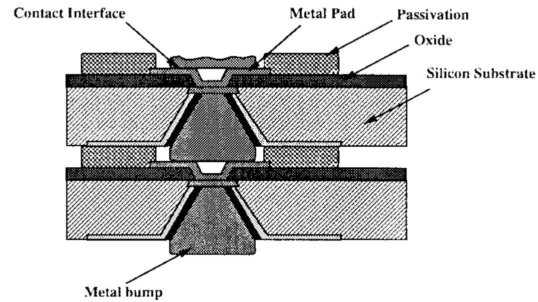

Fig. 25. Two wafers stacked using filled vias method.

f) *Stacked silicon wafers with filled vias:* In this method, vertical interconnections are formed using vias etched through the entire wafer and then filled with metal. The bottom side of the filled via contacts the top surface of a metal pad on the adjoining wafer as shown in Fig. 25. The filled vias are connected by applying pressure on the stack. This method was developed and used by Micron Technology for high density data storage using stacked nondiced wafers. Another wafer stacking approach was used by Lockheed Missiles and Space Company in the design of infrared signal processors [69], [70]. However, in the Lockheed approach the stacking is achieved by flip-wafer and achieving the interconnection using solder joints.

IV. LIMITATIONS OF 3-D PACKAGING TECHNOLOGY

The 3-D technology offers advantages for all types of electronic assemblies, including those for computer, military, automotive and telecommunication applications. However, there are trade-offs which need to be taken into account when using 3-D technology in system design. These trade-offs are briefly outlined in the following subsections.

A. Thermal Management

As the demand increases to build high performance systems, trends in electronic package design have moved toward larger chips, higher number of I/O ports, increased circuit density, and improved reliability. Greater circuit density means increased power density (W/cm^2). The power density has

increased exponentially over the past 15 years and it appears that it will continue to do so in the near future. As is the case with devices fabricated using 3-D technology, the power density is high, so thermal management should be considered carefully. The thermal management in 3-D technology has been addressed at two levels. The first is at the system design level by trying to evenly distribute the thermal energy across the 3-D device surface [71]. The second is at the packaging level. This is achieved through one or a combination of the following approaches. Firstly, by using low thermal resistance substrates such as diamond [64], [72] or chemical vapor deposition (CVD) diamond [73]. Secondly, by using forced air or liquid coolant to reduce the 3-D device temperature [74], [75]. Thirdly, by using a thermally conductive adhesive and implementing thermal vias [76] between the stacked elements to extract the heat from inside the stack to its surface. Even though, these methods are effective, it is believed thermal management will be more challenging with increased circuits densification.

B. Design Complexity

Advances in interconnection technology have played a key role in allowing continued improvement in integrated circuit density, performance, and cost. Over the last 20 years, circuit density has increased by a factor of approximately 10^4. According to Gordon Moore, CEO of Intel, integrated circuits will roughly double in density every device generation. One generation lasts about 18 months, resulting in a straight-line on a log scale [77]. As a result, feature size and resolution of geometries used in production follow the same trend with feature size reductions of about 20% per component generation. At the same time, increased functional integration has lead to larger chip sizes, which has required materials development for increased wafer size and equipment development for handling larger wafers.

A large number of systems have been implemented using the 2-D form, and have demonstrated that such complexity can be managed. However, a fewer number of systems and devices have been implemented using 3-D technology, proving nevertheless that such devices or systems are manageable, although complex. The increase in complexity can be managed by designing and developing software to cope with the increasing system complexity.

C. Cost

With the emergence of any new technology, there is an expected high cost involved in using it. As it is the case with the 3-D technology, the cost involved at present is high, due to the lack of infrastructure and the reluctance of manufacturers to change to new technologies for reasons associated with risk factors. Moreover, such cost is a function of the device complexity and the requirements. The following factors affect recurrent cost of stacking:

1) stack height and complexity;
2) number of processing steps per stack (e.g. for bare dice stacking present manufactures quote anything from 5–50 steps!);
3) test methodology used on each dice before stacking;
4) whether each die is burnt-in or not (IDDQ leakage current testing is often a cheaper alternative);
5) post silicon processing (e.g. pad reroute, wafer thinning, through substrate vias etc. are extremely expensive.);
6) the number of known good die (KGD) required per stack level. (This can vary anywhere from three to 20 depending on the 3-D manufacturer. If wafer thinning is employed, two wafers per stack level may be requested by the 3-D manufacturer—this leads to exorbitant cost.)

Furthermore, the nonreturnable engineering (NRE) cost is also very high, making it even harder to use 3-D technologies. Factors that strongly affect NRE include:

1) extent of tests carried out on a pilot batch of dummy stacks (e.g. thermal testing, stress gauge testing, electrical testing etc.);
2) number of dummy stacks required (usually varies between 20–50);
3) level of involvement of the 3-D manufacturer starting from system level design of the individual bare die (different 3-D manufactures have vastly varying capabilities in their ability for thermal and cross talk simulations, for example).

D. Time to Delivery

"Time-to-Delivery" is the time needed to fabricate a product. As expected the 'time to delivery' is function of the system complexity and requirements. In case of 3-D packaging technology, this time can be more than the time taken by any other 2-D packaging technologies. An inquiry to some manufacturers who provide 3-D packaging, revealed that the "time-to-delivery" is six to ten months, depending on the size and complexity of the 3-D device—this is two to four times longer than the time needed for MCM-D technology.

E. Design Software

Design software is one of the problems facing 3-D technology. Most manufacturers use their own design tool kits, which give the designers the ability to implement their design in accordance with the vendor's manufacturing requirements, while allowing the designers to focus on the design without getting involved with manufacturing and interfacing details. However, most of these design kits are not fully integrated or implemented in software that is easily accessible. Hence, for some of the manufacturers there is a need to port their design rules into available software or alternatively the customer may buy their own software. In the first case, there is a time and risk involved, while in the second the cost involved is the main issue, adding to the cost of 3-D device fabrication.

V. DISCUSSION

Three-dimensional packaging technology enhances most aspects of electronic systems such as size, weight, speed, yield and reduces power consumption. Moreover, due to the systematic elimination of faulty IC's during the assembly process of a 3-D device, the yield, reliability and robustness of the end

device will be high compared to a discrete implementation of such a device. Currently, 3-D packaging is limited by a number of factors. Some of these limitations such as thermal management are a result of densification, others are due to technological limitations, such as via diameter, line width, via pitch, and line spacing. It is expected that the effect of such limitations will decrease with the advances in packaging technology.

The main issues in 3-D packaging are the quality, the density of vertical interconnects, electrical characteristics, mechanical characteristics, thermal characteristics, availability of design tool kits, reliability, testability, rework, NRE cost, packaging cost, availability of known good die (KGD) and fabrication time. These factors determine the selection of a 3-D packaging technology. Moreover, as in most case these factors are interrelated, a measure of these issues in relation to the targeted application have to be identified. One way of doing so is to list all the accessible 3-D packaging technologies, then address the previous issues for each technology and grade them out of 100. The technology which scores the highest grade is the most suitable to use. Another important issue that has risen as part of this study is the accessibility to manufacturers who provide 3-D technology. Even though many companies are active in 3-D research and technology, few offer standard 3-D products and even fewer provide access to their packaging technology.

As seen from the above discussion, there are four distinct methods of stacking electronic circuits. Tables II and III provide a summary of most of the companies working in the area of 3-D packaging, classified according to the type of elements to be stacked. Some of these companies are not mentioned elsewhere in this paper, however, they are listed for completeness. Moreover, Tables VI to VII summarize the companies working in the area of 3-D packaging with their technology applications, countries, and the vertical interconnection methods used in their packaging techniques.

VI. Conclusion

Significant savings in power consumption, weight and physical volume can be achieved by adopting the 3-D packaging approach. A number of emergent bare dice and MCM stacking approaches have been reviewed. The choice of 3-D technology depends largely on the application. For stacking memory IC's, where the power dissipation is low and all the IC's are of matched size, "pancake" bare die stacking produces the most efficient results.

For the special case of *area* rather than *peripheral* connections (i.e., a regular array connected to a processor on a pixel-by-pixel basis), "loaf" rather than "pancake" bare dice stacking is preferable. The reason for this is that loaf stacking avoids the need for through-substrate-vias and hence saves silicon space and cost.

Bare die stacking techniques that require little or no silicon post processing and have the fewest number of 3-D fabrication process steps are the most attractive. The number of steps required for bare die stacking varies dramatically from vendor to vendor from the order of five to 50 steps!

In summary, bare die technology is most suitable when dealing with repetitive stacking of identical IC's. When dealing with a range of IC's of different sizes, the MCM stacking approach tends to be the most efficient in terms of cost and complexity. The most efficient, in terms of physical volume, appears to be the technique where thin MCM flex boards are stacked and then potted in epoxy. This technique also is advantageous for large volume production, where reel-to-reel flexboard can be utilized, many units can be potted in parallel and the resulting strip can then be sliced up. In cases where military/aerospace standards disallow organic materials (such as epoxy), particular attention for robustness and heat-sinking is required, then the various ceramic MCM stacking techniques can be employed. In this case the fuzz button approach appears to be the most widely used, due to its ability for high density vertical interconnect (about a factor of three better than surface mount connectors).

Finally, 3-D stacking techniques place upon the system designer more demands in terms of thermal and crosstalk modeling—also design for testability and a carefully structured test procedure are crucial. Vendors that thoroughly address simulation and test issues, and that focus on reducing the number of fabrication steps of their stacking technology will meet the demands of the system designer.

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Said F. Al-sarawi (M'92) received the general certificate in marine radio communication and the B.Eng. degree (with honors) in marine electronics and communication from the Arab Maritime Transport Academy (AMTA), in 1987 and 1990, respectively, the M.S. degree in low power microelectronics from the Department of Electrical and Electronic Engineering, University of Adelaide, South Australia, in 1991, and is currently pursuing the Ph.D. degree.

His research interests include design techniques for micro-power circuits in VLSI technology using standard CMOS technology, analog design techniques using neuron-MOS (νMOS) transistors, radio frequency electronic identification systems, ASIC design, neural networks, mixed digital-analog design, systems integration using MCM's, and 3-D packaging technologies.

Derek Abbott (M'85) received the B.Sc. degree (with honors) in physics from Loughborough University of Technology, U.K. and the Ph.D. degree (with distinction) in electrical and electronic engineering from the University of Adelaide, Australia.

He worked for nine years at the GEC Hirst Research Centre, London, U.K., on infrared and visible image sensors—requiring discipline in VLSI design, optoelectronics, device physics, semiconductor noise, fabrication, and testing. He has worked with both novel and standard technologies, including nMOS, CMOS, CCD, SOS, GaAs, and vacuum microelectronics. Since emigrating to Australia, he worked for Austek Microsystems, Technology Park, South Australia, and where he has been with the University of Adelaide since 1987, is a Senior Lecturer with the Department of Electrical and Electronic Engineering. He has been an Invited Speaker at a number of international institutions and has appeared on international radio and television. He is a founder member and deputy director of the Centre for High Performance Integrated Systems and Technologies (CHiPTec), Adelaide, instituted in 1987. He has been consultant to various U.K. and Australian defense and industry organizations. His current research interests are in the areas of VLSI, GaAs, photodetectors, smart sensors, imaging devices, device physics, and noise. He has been an Invited Speaker at the University of Geneva; EPFL, Lausanne; CSEM, Neuchatel; University of Las Palmas, Spain; Motorola, Tempe; Massachusetts Institute of Technology, Cambridge; Los Alamos National Laboratories, NM; Seoul National University, Korea; Chonnam National University, Korea; Tokyo Metropolitan University; Cambridge University, U.K.; UNED, Madrid, and the Technion, Israel. He was an Invited Keynote Speaker at the SPIE Photonics East conference in Philadelphia, PA, 1995, was an Invited Speaker at UPoN'96, Szeged, Hungary, and is an Invited Speaker at Micro'97, Adelaide. He is currently co-authoring a text for Cambridge University Press.

Dr. Abbott is a member of the International Scientific Advisory Committee, UPoN, the Technical Program Committees for SPIE Photonics East and the IEEE GaAs IC Symposium, and the Executive Organizing Committee, SPIE Smart Materials, Structures, and MEMS conference. He is the Conference Director for UPoN'99, to be hosted in Adelaide, Australia.

Paul D. Franzon (M'89) is an Associate Professor in the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh. He has over eight years experience in electronic systems design and design methodology research and development. During that time, in addition to his current position, he worked at AT&T Bell Laboratories, Holmdel, NJ, at the Australian Defense Science and Technology Organization, as a Founding Member of a successful Australian technology start-up company, and as a Consultant to industry, including technical advisory board positions. His current research interests include design sciences/methodology for high speed packaging and interconnect, for high speed and low power chip design, and the application of microelectromechanical machines to electronic systems. In the past, he has worked on problems and projects in wafer-scale integration, IC yield modeling, VLSI chip design, and communications systems design. He has published over 70 articles and reports. He is also the co-editor and author on a book about multichip module technologies, published in October, 1992. His teaching interests focuses on microelectronic systems building including package and interconnect design, circuit design, processor design, and the gaining of hands-on systems experience for students.

Dr. Franzon received an NSF Young Investigator's Award in 1993. He is a member of ACM and ISHM and serves as Chairman of the Education Committee, National IEEE-CHMT Society. In 1997, he was the General Chair at the IEEE MultiChip Module Conference.