Deblurring algorithm: It is very difficult to extend deblurring procedures directly to a vector space; this is why a componentwise ARMA deblurring method has been adopted to compensate for the smoothing.

The aim of the deblurring step is to estimate the point spread function (PSF) of the unknown degrading system. The image is described through a nonsymmetric half plane (NSHP) model[2]

$$s(m, n) = \sum_{(k, l) \in C} c(k, l)s(m - k, n - l) + w(m, n) \quad (3)$$

where $C = \{(1 \leq k \leq M, \quad 0 \leq l < M) \cup (-M \leq k \leq 0, 1 \leq l \leq M)\}$ and $w(m, n)$ is a zero mean white Gaussian noise with variance σ_w^2. The observed image is a distorted version of $s(m, n)$. If we model the distortion as an FIR noncausal system, the resulting image will be

$$r(m, n) = \sum_{(i, j) \in C'} h(i, j)s(m - i, n - j) + v(m, n) \quad (4)$$

where $C' = \{-H \leq i \leq H, \ -H \leq j \leq H\}$ and $v(m, n)$ is additive noise. If we assume that the additive noise is negligible, by substituting eqn. 3 into eqn. 4 we obtain

$$r(m, n) = \sum_{(k, l) \in C} c(k, l)r(m - k, n - l) + \sum_{(i, j) \in C'} h(i, j)w(m - i, n - j) \quad (5)$$

The observed image may then be modelled by an ARMA model, where the AR part is based on the image model parameters and the MA part is based on the blur parameters. The parameters and the order of the ARMA model must be determined. A least squares estimate of the parameters is achieved by searching the minimum of the quantity $\Sigma w^2(m, n)$. When the function $H(\omega_1, \omega_2)$ is decomposed into a four quadrant factorisation[2,3] the previous minimum can be achieved by means of a recursive procedure. This is possible if $H(\omega_1, \omega_2) \geq 0$ (e.g. a Gaussian blurring function). Once the parameters of the MA part have been determined, the deblurring step is completed by using such parameters in inverse filtering the observed image.

Experimental results: To evaluate the algorithm previously described (a vector median filter followed by an ARMA deblurring technique), some experiments have been performed by using art images. When dealing with artwork images it is mandatory to filter the acquisition noise without blurring the image themselves and without generating new colours; hence the proposed processing chain is particularly suitable.

Fig. 4 *Original image*

Fig. 4 shows the original image before noise filtering. By applying a 3 × 3 vector median filter the result shown in the upper left part of fig. 5 is obtained. Evidently some noise is removed and some blur is generated. By componentwise applying the ARMA deblurring algorithm outlined previously, the result shown in the upper right part of fig. 5 is obtained, where the blur effect is almost completely eliminated. Similar results have been obtained by using a 5 × 5 vector median filter (lower part of Fig. 5).

Conclusions: A technique which allows the filtering of noise in colour images with a significant reduction of the image blur has been described. Such a result has been achieved by chaining a vector median filter and an ARMA deblurring technique. Vector median filters allow good results in terms of spike noise suppression and ensure colour closed operations.

Fig. 5 *Vector median filtered images before (left) and after (right) deblurring*

The deblurring part of the algorithm can be applied to the luminance component of the image if colour closed operations are required. In this Letter the blurring function has been assumed to be positive and symmetric to achieve four quadrant factorisation. When this hypothesis does not hold, only an approximation to the correct PSF can be obtained and this reduces the final quality of the deblurred image.

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PHOTOVOLTAIC GATE BIASING EDGE EFFECT IN GaAs MESFETs

Indexing terms: Gallium arsenide, Field-effect transistors, Semiconductor devices and materials

A new effect in planar GaAs MESFETs, whereby a sharp increase in optical gain at the transistor edges occurs, is reported for the first time. This gain effect only appears when a large resistor is inserted in series with the gate, to produce the conditions for photovoltaic gate biasing. The mechanism for increased gain at the edges is suggested to be due to carrier photogeneration in the substrate that is subsequently collected by the gate. Application in the area of X-Y addressable transistor array imagers is proposed.

The photoresponse of the GaAs MESFET has received much attention due to the potential application of the GaAs MESFET in high speed optoelectronic communications, OEICs and optical tuning of microwave devices. Various optical gain mechanisms have been reported, including photovoltaic gate biasing. This effect occurs when the gate photocurrent flows through an external series gate resistor R_g, thus increasing the gate voltage and hence drain current. To produce a significant increase in drain current, a large R_g

introduces a large RC time constant which typically causes the response to roll off in the 10–100 MHz range. Consequently, as most researchers have concentrated on high speed applications, photovoltaic gate biasing has been regarded as being of limited merit[1] and has not received full attention.

Photovoltaic gate biasing is, however of interest in a low frequency GaAs X-Y addressable transistor array for solid-state imaging. The pixels in such an imager can be configured to optimise the edge gain mechanism, thereby increasing the sensitivity of the device. With careful development, a GaAs imager using a conventional planar MESFET technology may potentially offer increased radiation hardness, reduced dark current and the convenience of integration with high speed GaAs image processing cells.

We report a new finding that the optical gain sharply increases where the gate crosses the transistor edge. This only occurs with a series gate resistor inserted, to produce the conditions for photovoltaic gate biasing. This finding suggests that carriers generated in the substrate, beyond the transistor boundary, are able to be collected by the gate depletion region. This edge effect is observed in a planar GaAs MESFET and is quite different to the edge gain effect observed in mesa GaAs MESFET structures.[2,3]

We proposed a generalised model for the photoresponse of a GaAs MESFET in a recent paper,[4] which considered a photovoltaic (PV) effect in the gate depletion region, a photoconductive (PC) effect in the channel and two main substrate effects (trapping by defect centres and substrate/channel depletion region collection). To explain the observed effects, in the present case, we are able to invoke the gate depletion region and substrate/channel depletion region parts of the model.

Experiment: The planar MESFETs used have a fingered structure with five gates, $L = 0{\cdot}8\,\mu m$ and overall $W = 400\,\mu m$. The channel (depth $d = 0{\cdot}1\,\mu m$ and doping $N_d = 1{\cdot}2 \times 10^{17}\,cm^{-3}$) is situated on a semi-insulating (SI) GaAs: EL2 substrate, with no buffer layer. The source gate and drain-gate separations are both $1{\cdot}3\,\mu m$.

The device was mounted on a computerised X-Y platform and illuminated by a $2\,\mu m$ diameter CW laser spot with a wavelength of 678 nm. The laser power incident on the device was measured to be $1{\cdot}4\,\mu W$. The X-Y platform was controlled to move the device through a 2-D raster sequence and the drain current was automatically logged so that a 3-D plot of the transistor response was generated.

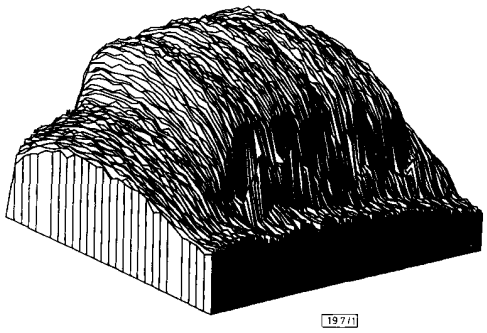

Fig. 1 *MESFET drain current response to 2-D laser scan*
Maximum current = 3·7 mA; no gate resistor

Results: Example 3-D plots of transistor drain current response to laser illumination are shown in Figs. 1 and 2. For comparison, the case for no series gate resistor is shown in Fig. 1. Peak drain current is in the central region of the transistor, and the drain current rolls off towards the periphery of the transistor, as expected from classical theory. However, with a 10 MΩ resistor in series with the gate, Fig. 2 shows dramatic drain current peaks at the positions where gate metal crosses the transistor edge. The five peaks along an edge correspond to the five gates. There are two sets of five peaks, as the gates overlap the transistor at both ends, of course.

These plots were repeated for a number of devices and it was observed that the peak heights did not vary substantially within each set of five. However, there were some cases when a set of peaks at one end of the transistor were as much as four times the height of the set at the opposite end. This effect could not be correlated with any visible transistor layer misalignment.

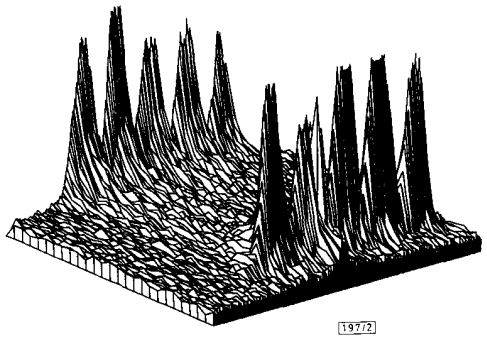

Fig. 2 *MESFET drain current response to 2-D laser scan*
Maximum current = 29 mA; 10 MΩ gate resistor

Note that although the gates are opaque, the peaks actually correspond to a position where the laser spot is exactly centred on the gate (Fig. 3). This is because the spot diameter is larger than the gate length and thus a central position maximises the amount of light to the gate edges, where the depletion region extends outwards, from under the gate, and is exposed. Also, holes diffusing in the channel that are generated close to the gate edges can be collected by the gate depletion region. Even though the diffusion length of holes in the channel is $1{\cdot}8\,\mu m$, holes that are far from the gate are more likely to be collected by the channel/substrate depletion region because the channel depth $d \ll 1.8\,\mu m$; therefore there is a very narrow capture angle for gate collection.

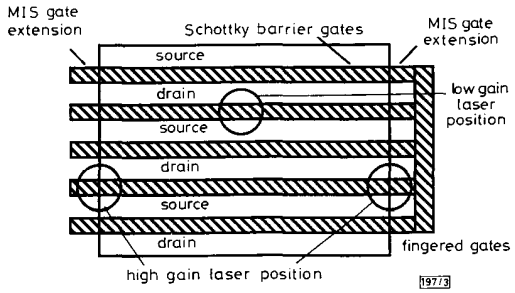

Fig. 3 *Laser spot positions for high and low gain drain current response*

Discussion: We established that the peak drain current could be accounted for by an increase in gate photocurrent, as measured by an electrometer. Fig. 4 shows gate photocurrent

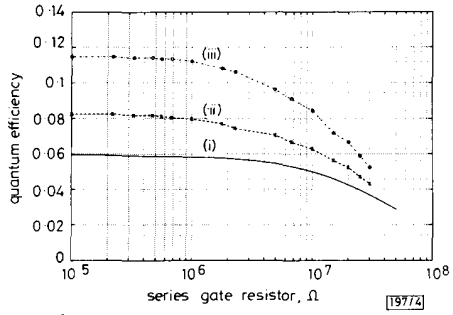

Fig. 4 *Quantum efficiency against gate resistor*
(i) internal quantum efficiency ($T = 1$) from first order theory
(ii) measured (low gain)
(iii) measured (high gain)

against R_g, when the laser spot is centrally placed on the gate, for a position at the transistor edge (high gain) and towards the middle of the transistor (low gain). The theoretical curve is found by following the front illumination case of Seib,[5] to evaluate the quantum efficiency η. However, in a GaAs MESFET, the boundary conditions change and the equations are now solved with hole concentration $p = 0$ at the substrate/channel interface ($y = d$), instead of at $y = \infty$. This results in

$$\eta = T(\lambda)A_0\{1 - \exp(-\alpha W_d) - A + B - C\} \quad (1)$$

where

$$A = \frac{\alpha^2 L_0^2 \exp(-\alpha W_d)}{1 - \alpha^2 L_0^2}$$

$$B = \frac{A}{\alpha L_0} \frac{1 - \exp\left\{-(d - W_d)\left(\alpha + \frac{1}{L_0}\right)\right\}}{1 - \exp\left\{\frac{-2(d - W_d)}{L_0}\right\}}$$

$$C = \frac{A}{\alpha L_0} \frac{1 - \exp\left\{-(d - W_d)\left(\alpha - \frac{1}{L_0}\right)\right\}}{1 - \exp\left\{\frac{2(d - W_d)}{L_0}\right\}}$$

L_0 is the hole diffusion length in the channel and α is the absorption coefficient at the wavelength of interest. If we assume that the depletion region extension from under the gate is W_d and approximate that light is only captured in these regions, as a first order estimate, then the dimensionless geometry factor $A_0 = 2 \times 1{\cdot}83 \times W_d/\pi$. The depletion region width W_d is given by the standard relation for a Schottky barrier

$$W_d = \left[\frac{2\varepsilon_0 \varepsilon_r}{qN_d}\left|V_{bi} - V_g - \frac{kT}{q}\right|\right]^{1/2} \quad (2)$$

where, the built in voltage, $V_{bi} = 0{\cdot}85$ V. If the external bias applied to R_g is $-0{\cdot}8$ V, then the gate voltage $V_g = -0{\cdot}8 + I_g R_g$. By knowing the incident laser power P_0, the gate photocurrent is obtained from

$$I_g = \left(\frac{q\lambda}{hc}\right)\eta P_0 \quad (3)$$

The theoretical curve for η in Fig. 4 is obtained via an iterative solution of the above equations with the transmission coefficient set at $T = 1$, for simplicity. This is lower than the measured curve because our first order approximation has neglected sideways diffusion of holes into the gate. However, a full three dimensional solution to the diffusion equation will be presented in a future paper.

The high gain curve in Fig. 4 can only be explained if there are holes generated in the substrate, outside the transistor, being collected by the gate. Therefore we postulate the existence of a depletion region in the substrate that has connecting electric field lines with the edge of the gate depletion region. This new depletion region is assumed to be formed under the MIS structure, where the gate extends over Si_3N_4, outside the transistor. If the effect of surface states under the MIS gate is ignored, we estimate that the depletion region would need to be about 2 μm deep and extend out under the gate by a maximum of 0·2 μm to account for the high gain curve in Fig. 4.

In conclusion, we have reported a new optical edge gain effect in planar GaAs MESFETs, useful in low frequency applications, such as in an X-Y array imager. Photocollection under the MIS gate extension, outside the transistor, is suggested to explain the gain effect. Future models for the photoresponse in planar GaAs MESFETs, that attempt to generalise all operating conditions, must take into account this new effect.

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FAST CLOCK SYNCHRONISER USING INITIAL PHASE PRESETTING DPLL (IPP-DPLL) FOR BURST SIGNAL RECEPTION

Indexing terms: Circuit design, Digital communication systems

A fast clock synchroniser that quickly adjusts the initial phase of the DPLL output clock to the input signal (receiver detector output) at the beginning of acquisition is proposed for burst QDPSK signal reception. The synchroniser performance is given in terms of nondetection rate (NDR) of the unique word following the clock synchronisation preamble. Measured results clearly indicate that the proposed synchroniser achieves faster synchronisation than the conventional binary quantised DPLL clock synchroniser.

Introduction: Burst control signals are transmitted whenever a mobile accesses its base station. The burst frame is composed of the clock synchronisation preamble, unique word and data part. During the preamble period, the recovered clock must be synchronised to the input signal for sampling and symbol decision. A conventional clock synchroniser uses a binary quantised DPLL.[1] This can provide a very stable output clock, however its acquisition time is long and thus a long preamble is needed. The frame use efficiency can be increased if the preamble length is as short as possible. Fast synchronisation can be achieved with a conventional DPLL at the cost of increased output clock jitter which degrades burst signal reception performance. This Letter proposes a new clock synchroniser that quickly adjusts the initial phase of the DPLL output clock to the input signal at the beginning of acquisition, and measured performance is reported for QDPSK burst signal reception in mobile radio channels.

Principle of operation: Fig. 1 shows the block diagram of the initial phase presetting DPLL (IPP-DPLL) clock synchro-