measured Q values of three inductors are shown in Fig. 2. At 5 GHz, the inductor of 2.21 nH has limited its Q for self-resonance, and the inductor of 0.46 nH has a lower Q for its small inductance. The inductor of 0.86 nH has the highest Q at 5 GHz.

An oscillation frequency is determined by

$$f = \frac{1}{2\pi\sqrt{L(C_{VD} + C_P)}}$$

where L is the inductance of the inductor, C_{VD} is the capacitance of the varactor diode and C_P is the parasitic capacitance of the differential pair M1–M2, buffers and inductors. For a low-noise characteristic, C_P cannot be reduced too much; a lower L and higher C_{VD} are preferred for extending the tuning frequency, and it is contrary to the requirement for the low phase-noise characteristic.

In this work, the inductance of 0.86 nH was adopted for the low phase-noise characteristic, and the C_P was reduced for a sufficient frequency-tuning range, i.e. C_P is reduced to the same value as the C_{VD} to adopt not too large MOSFETs for the differential pair and buffer circuit.

Measured results: The 4.6 GHz VCO was fabricated using 0.25 μm CMOS technology. Fig. 3 shows a die photograph of the VCO. The chip size, including the area of the pads, is 1200 × 700 μm. All measured results were obtained using the on-wafer probing technique. The power supply voltage was 2 V, the current consumption was 8.6 mA, and the current consumption without the output buffer circuits was 4.7 mA. Fig. 4 shows the measured frequency-tuning characteristic and output power of the VCO. The frequency-tuning range is 4.40 to 4.63 GHz, and the output power is >−7.7 dBm with the control voltage 1 to 2 V. The measured frequency-tuning range is sufficient for the target specification of 200 MHz. Fig. 5 shows the measured phase-noise characteristic, and −118.1 dBc/Hz is obtained at 1 MHz offset and −138.7 dBc/Hz at 10 MHz offset. This phase noise is superior to previously reported phase noise in the 5 GHz band [2–4]. All measured results met out target specifications.

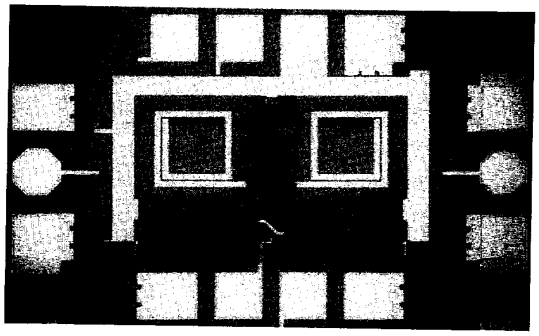

Fig. 3 *Die photograph of VCO*

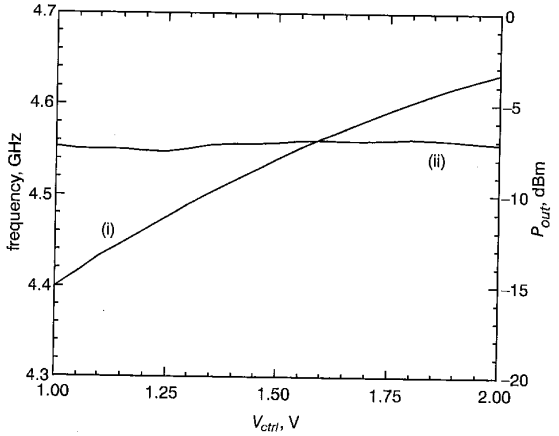

Fig. 4 *Measured frequency-tuning range and output power of VCO*
(i) oscillation frequency
(ii) output power

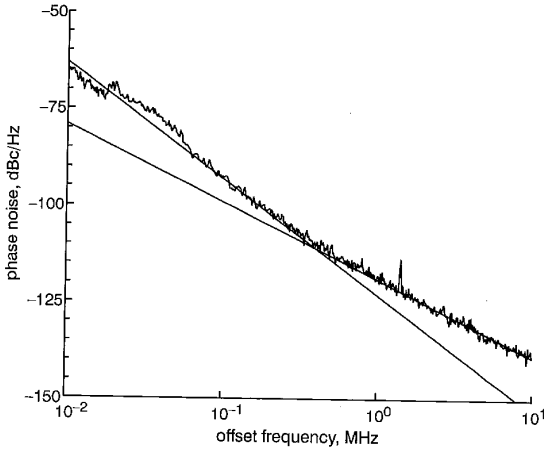

Fig. 5 *Measured phase-noise characteristic of VCO*

Conclusions: The circuit design and measured results of the 4.6 GHz VCO using 0.25 μm CMOS technology have been presented. A measured frequency-tuning range of 230 MHz and phase noise of −118.1 dBc/Hz at 1 MHz offset and −138.7 dBc/Hz at 10 MHz offset were obtained for careful circuit design based on the trade-off between frequency-tuning range and phase noise.

4 February 2002
Electronics Letters Online No: 20020444
DOI: 10.1049/el:20020444

R. Fujimoto, R. Tachibana, H. Yoshida and S. Otaka (*Corporate Research & Development Center, Toshiba Corporation, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan*)

E-mail: ryuichi.fujimoto@toshiba.co.jp

K. Kojima (*System LSI Research & Development Center, Toshiba Corporation, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan*)

References

1 LEESON, D.B.: 'A simple model of feedback oscillator noise spectrum', *Proc. IEEE*, 1966, **54**, (2)
2 KINGET, P.: 'A fully integrated 2.7 V 0.35 μm CMOS VCO for 5 GHz wireless application'. IEEE ISSCC98, San Francisco, CA, USA, February 1998, pp. 226–227
3 HUNG, C.-M.: 'Fully integrated 5.35-GHz CMOS VCOs and prescalers', *IEEE Trans. Microw. Theory Tech.*, 2001, **49**, (1), pp. 17–22
4 COPELAND, M.A.: '5-GHz SiGe HBT monolithic radio transceiver with tunable filtering', *IEEE Trans. Microw. Theory Tech.*, 2000, **48**, (2), pp. 170–181

Compact parallel (*m,n*) counters based on self-timed threshold logic

P. Celinski, J.F. López, S. Al-Sarawi and D. Abbott

A new, highly compact implementation of general parallel counters (i.e. population counters) with logic depth 2, based on self-timed threshold logic, is presented. The novel feature of the design is the sharing among all threshold gates of a single capacitive network for computing the weighted sum of all input bits. The significance of the result is the reduction by almost 50% in the required number of capacitors. Interconnect routing cost is also reduced, resulting in significantly decreased total area.

Introduction: As the demand for higher performance very large scale integration processors with increased sophistication grows, continuing research is focused on improving the performance, area efficiency, and functionality of the arithmetic and other units contained therein.

Threshold logic (TL) was introduced over four decades ago, and over the years has promised much in terms of reduced logic depth and gate count compared to conventional logic-gate-based design. However, lack of efficient realisations has meant that TL has, over the years, had little impact on VLSI systems. Efficient TL gate realisations have been developed (see [1, 2]) and more recently (see [3]), and a number of applications based on TL gates have demonstrated its ability to achieve high operating speed and significantly reduced area. In this Letter we present a novel, highly compact, low power implementation of CMOS parallel counters based on self-timed threshold logic.

Self-timed threshold logic (STTL): A threshold logic gate is functionally similar to a hard limiting neuron. The gate takes n binary inputs $x_1, x_2, \ldots, x_n$ and produces a single binary output y based on a linear weighted sum of the binary inputs followed by a thresholding operation. The Boolean function computed by such a gate is called a threshold function and it is specified by the gate threshold T and the weights $w_1, w_2, \ldots, w_n$, where w_i is the weight corresponding to the ith input variable x_i. The output y is 1 if $\sum_{i=1}^{n} w_i x_i \geq T$, and 0 otherwise.

Fig. 1 shows the proposed circuit structure for implementing self-timed threshold logic. The main element is the cross-coupled NMOS transistor pair (M3, M4) which generates the output Q and its complement Q_b after buffering by the two inverters. The gate operates in two phases. Precharge and evaluate are specified by the dual enable signals E and its complement E_b. The inputs x_i are capacitively coupled onto the floating gate ϕ of M10, and the threshold is set by the gate voltage T of M11. The potential ϕ is given by $\phi = \sum_{i=1}^{n} C_i x_i / C_{tot}$, where C_{tot} is the sum of all capacitances, including parasitics, at the floating node. Weight values are thus realised by setting capacitors C_i to appropriate values. In CMOS, these capacitors are typically implemented between the polysilicon 1 and polysilicon 2 layers.

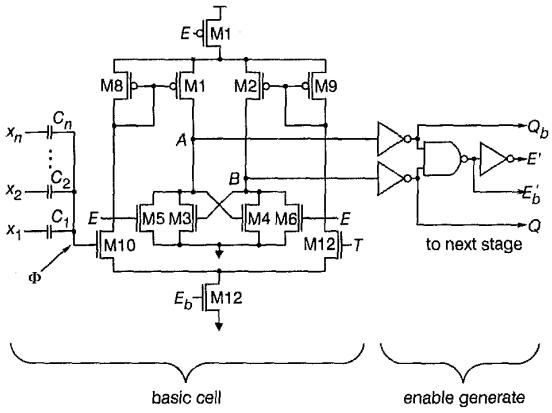

Fig. 1 *Proposed self-timed threshold logic gate*

The enable signals, E and E_b, control the precharge and activation of the sense circuit. When E is high the voltages at nodes A and B are discharged to ground. When E is low and E_b is high, the outputs are disconnected from ground and the differential pair, formed by M10 and M11, draws different currents from the supply via M8 and M9. The currents in M8 and M9 are mirrored by M1 and M2, respectively, and the gates of M3 and M4 (nodes A and B) begin to charge at different rates. As the charging rates are different and the capacitances at those two nodes are the same (ensured by identical sizing of the two buffer inverters connected to nodes A and B), a voltage difference begins to develop between nodes A and B. When this difference is sufficiently large, either M3 or M4 turns on fully, but not both. The outputs Q and Q_b are evaluated and passed to the next stage. In this way, the circuit structure effectively determines whether the weighted sum of the inputs, ϕ, is greater or less than the threshold, T, thus realising a thresholding operation. The enable signals and the data passed to the next stage are generated by the circuit labelled 'enable generate'. The inverters connected to nodes A and B are buffers. The NAND gate generates the signal E'_b and the remaining inverter its inverse E'. When the first gate is in precharge phase, the second and all subsequent gates are also in the precharge phase. After the outputs of the first stage are evaluated all subsequent outputs also evaluate in succession. Thus, outputs of each gate propagate through the chain in a self-timed fashion.

Proposed modified Minnick counter design: An (m,n) counter is a combinatorial network which generates a binary coded output vector of length n which corresponds to the number of logic 1's in the m-bit input vector. Counters are important in various applications, the most common of which is the reduction of the partial product tree in parallel multipliers.

Higher-order counters, such as (7,3) or (15,4), have traditionally been implemented using trees of (3,2) counters (full adders) because of the disadvantages of a direct implementation. However, counters consisting of such full adder trees have a relatively high delay and grow rapidly with input vector size in terms of the required number of full adders. The Minnick counter [4] based on TL offers a good trade-off in terms of area and delay. For these reasons we have chosen the Minnick counter as the basis for our modified implementation. The (7,3) counter will be used as an illustrative example, but the technique presented here can be equally applied to higher-order counters.

The (7,3) Minnick counter consists of five threshold gates arranged in two layers, three in the first layer and two in the second layer. The circuit diagram showing the proposed design is shown in Fig. 2. Usually the implementation of this counter using one of the recently proposed capacitive TL gates would require the network of seven capacitors connected to the seven inputs to be duplicated at each of the gates in the circuit. Therefore, significant area would be associated with routing the seven interconnect lines to each of the five gates, and with duplicating the seven capacitors at each gate. These drawbacks have an even greater impact on total area for higher-order counters. The innovation proposed here is to implement the capacitive network which calculates the analogue value of the sum of the counter input bits only once, and this value becomes one input of the sense amplifier in each STTL gate. In the second layer gates, the other sense amplifier input is connected to the capacitive networks which implement the negative weights of the layer 1 to layer 2 interconnections. Such an arrangement is made possible by the differential nature of the STTL gate. Output y_2 is available after one gate delay and the remaining outputs after two gate delays. All outputs can be made to evaluate simultaneously by adding one additional STTL gate which would act as a delay element for y_2. This gate is shown with dashed lines in Fig. 2.

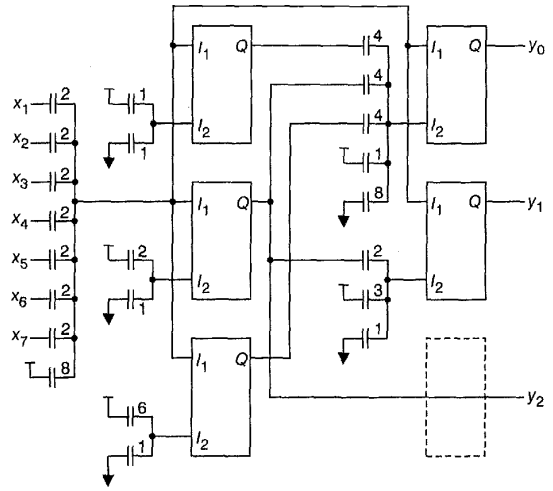

Fig. 2 *Circuit diagram of proposed STTL modified Minnick (7,3) counter*

The numbers next to the capacitors in Fig. 2 indicate the multiple of the unit capacitor. Enable signals E and E_b are not shown, to improve clarity. The two gates in the second layer are enabled after the outputs from the first layer are evaluated. Capacitors shown connected to *Gnd* and V_{dd} adjust the effective threshold of each STTL gate. The inputs denoted by I_1 and I_2 in Fig. 2 correspond to the ϕ and T inputs, respectively, shown in Fig. 1.

Results and conclusions: The (7,3) counter circuit shown in Fig. 2 was simulated with HSPICE using industrial 0.25 μm process parameters at a supply voltage of 2 V. The value of the unit capacitor was chosen to be 5 fF. The enable signal frequency for the first layer gates was 300 MHz and the power dissipation was measured to be 870 μW.

The simulation waveforms are shown in Fig. 3. The waveform I_1 represents the input to each STTL gate and increases as the number of 1's in the input vector, $(x_1, \ldots, x_7)$, is increased from none to seven. It can be seen that when the first layer enable signal, E, goes low, the outputs y_2, y_1 and y_0 evaluate correctly for all values of the input vector.

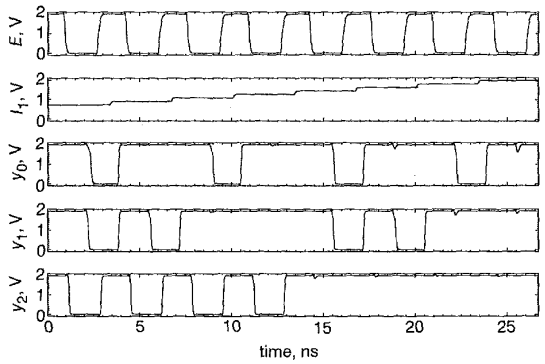

Fig. 3 *Simulation results of STTL modified Minnick (7,3) counter*

The counter delay is <1.4 ns, measured from the falling edge of the enable signal to y_0 or y_1. Compared to conventional designs of the Minnick (7,3) counter, the required number of capacitors has been reduced from 39 to 22.

6 February 2002
Electronics Letters Online No: 20020438
DOI: 10.1049/el:20020438

P. Celinski, S. Al-Sarawi and D. Abbott (*Department of Electrical and Electronic Engineering, Centre for High Performance Integrated Technologies and Systems (CHiPTec), Adelaide University, Adelaide, SA 5005, Australia*)

E-mail: celinski@eleceng.adelaide.edu.au

J.F. López (*Research Institute for Applied Microelectronics, Universidad de Las Palmas de G.C., 35017, Spain*)

References

1 AVEDILLO, M.J., QUINTANA, J.M., RUEDA, A., and JIMÉNEZ, E.: 'Low-power CMOS threshold-logic gate', *Electron. Lett.*, 1995, **31**, (25), pp. 2157–2159
2 ÖZDEMIR, H., KEPKEP, A., PAMIR, B., LEBLEBICI, Y., and CILINIROĞLU, U.: 'A capacitive threshold-logic gate', *IEEE J. Solid-State Circuits*, 1996, **31**, (8), pp. 1141–1149
3 CELINSKI, P., LÓPEZ, J.F., AL-SARAWI, S., and ABBOTT, D.: 'Low power, high speed, charge recycling CMOS threshold logic gate', *Electron. Lett.*, 2001, **37**, (17), pp. 1067–1069
4 MINNICK, R.C.: 'Linear-input logic', *IRE Trans. Electron. Comput.*, 1961, **EC-10**, pp. 6–16

1260 nm InGaAs vertical-cavity lasers

C. Asplund, P. Sundgren, S. Mogg, M. Hammar, U. Christiansson, V. Oscarsson, C. Runnstrm, E. Odling and J. Malmquist

The fabrication and performance of highly strained double-quantum well InGaAs/GaAs vertical-cavity lasers with record-long emission wavelength of 1260 nm at room temperature is reported. Depending on device diameter, the minimum threshold current is in the low mA-regime while the maximum output power exceeds 1 mW. The devices work continuous-wave over a wide temperature range of at least 10–120°C.

Introduction: Long-wavelength (1.30–1.55 μm) vertical-cavity lasers (VCLs) are much requested as potential low-cost sources for fibre-optical communication systems. However, despite extensive research and development efforts during the past decade, the commercial breakthrough of such VCLs has still to be achieved. A major problem in their realisation is the lack of a lattice-matched materials system providing both high-index-contrast distributed Bragg reflectors (DBRs) and high-gain quantum-wells (QWs). While excellent DBRs can be built up in the AlGaAs/GaAs system, long-wavelength QWs are only well established in the InP system. High-performance 1.3 μm VCLs have been realised using wafer-bonding between InP-based active materials and AlGaAs/GaAs DBRs [1]. However, this is a rather complex fabrication procedure that has not proven to meet the requirements of low-cost production. A more recent approach has been the application of 1.3 μm GaInNAs quantum wells lattice-matched to GaAs [2–4], but this materials system is very difficult to master and it is presently unclear whether it will lead to a viable technology. Parallel with this development it has been realised that using well-tuned growth conditions it is possible to fabricate InGaAs QWs on GaAs substrate with photoluminescence (PL) emission wavelength around 1200 nm [5]. Using such QWs, 1.22 μm VCLs with excellent characteristics have been demonstrated [6, 7]. While this wavelength is too short for typical singlemode applications, there appears to be room for improvements from further optimised QWs and/or device tuning, and it is of interest to find the limits of this technology. It should be noted that the wavelength requirements as dictated by specific applications and related standards are usually shorter than the 1310 nm corresponding to minimum dispersion in standard fibres. For instance, for 10 gigabit Ethernet or Telecom-SONET OC-192 the lower end of the wavelength window is set to 1260 nm [8, 9], basically corresponding to the cutoff wavelength of standard singlemode fibres. This wavelength should thus be considered as an important first target for device optimisation.

In the present work we have investigated the possibility of extending the emission wavelength of InGaAs VCLs using extensive gain-cavity detuning. For InGaAs double QWs (DQWs) with PL emission peak around 1190 nm the cavity resonance is varied between 1190 and 1260 nm. Lasing is obtained in the whole of this wavelength interval, showing threshold currents in the low mA-regime and mW output power even for an emission wavelength of 1260 nm. We consider these results very encouraging since they demonstrate a possible route towards 1.3 μm VCL technology based on mature and standard materials systems, quite similar to those used in the successful development of shorter-wavelength VCLs widely employed in short-distance multimode applications.

Experiment: The VCL structure was grown by metal organic vapour-phase epitaxy (MOVPE) and consists of an Si-doped 25.5-period bottom DBR, a one-lambda GaAs cavity region comprising two InGaAs QWs separated by a GaAs barrier layer of 20 nm, and a Zn-doped 26-period top DBR. The top DBR includes a 40 nm AlAs oxidation layer for current and mode confinement. The QWs were grown at 530°C using TEGa, TMIn and TBAs as precursors, while the 15 nm linearly graded $Al_{0.88}Ga_{0.12}As$/GaAs DBRs were grown at 680°C using TMGa, TMAl, AsH_3, DEZn and SiH_4. The doping concentration is kept low in both DBRs to minimise the effects of optical loss [10]. The well width is 8.1 nm for an In content of 39% resulting in a PL emission wavelength around 1190 nm with a full-width at half maximum below 27 meV. Owing to a radially non-uniform growth rate across the wafer we obtain a variation in the offset between PL and cavity mode as shown in Fig. 1. Mesas of different sizes between 35 and 43 μm were etched through the top DBR and a steam-oxidation process was employed to form apertures with diameters between 4 and 12 μm. Finally n- (AuBe) and p- (AuGe) contacts were formed and the top-emitting structure was planarised with benzocyclobutene (BCB).

Results and discussion: Fig. 2 shows continuous-wave (CW) light against current (LI) characteristics for 9 μm devices at different positions on the wafer, corresponding to different emission wavelengths as indicated. The threshold current increases with increasing wavelength and PL-cavity offset, but the maximum output power is still as high as 0.8 mW for a wavelength of 1260 nm. As shown in Fig. 3, the threshold current decreases monotonously with decreasing device diameter to 3.1 mA for a 5 μm aperture. The devices work CW to at least 120°C, the maximum temperature of our heat stage. Owing to the large negative gain-cavity offset the threshold current decreases with increasing temperature with a minimum around 85°C, reaching 1.6 mA for a 6 μm device (see Fig. 3). The emission wavelength increases with increasing temperature and was measured to 1269 nm at 120°C, corresponding to a wavelength shift of 0.087 nm/K.