# Low power serial-parallel dynamic shift register

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Serial-to-parallel shift registers have a wide range of applications. These registers are commonly found in communication systems and interfaces between electronic peripherals. Presented is a unique low power area efficient 128 bit serial-to-parallel shift register design that contains only four transistors per stage. The new register uses the capacitive bootstrapping technique to overcome the threshold voltage drop of MOSFETs. This logic family is named non-ratioed bootstrap logic (NRBL). Target applications are dense smart sensor arrays and image sensors.

*Introduction:* The shift register is perhaps the most common structure for enabling the movement of a data bit in VLSI systems [1]. Shift registers have many applications ranging from producing time delay by using serial-in serial-out shift registers, or converting serial data to parallel data using a serial-in parallel-out shift register. Serial-in parallel-out shift registers are commonly used in image sensors to control the analogue multiplexer, which transmits data from the photodiode pixel to the A/D converter then processed into an image.

There has been recent interest in using capacitors to reduce the size of VLSI circuits [2]. In this Letter we present a different capacitive approach to produce a very compact serial-parallel shift register. For the first time in the open literature, we demonstrate functionality with four transistors per stage and no DC power rails. There are a number of applications where both low power and compactness are required. These include dense optical smart sensors [3] and gate control of solid-state quantum computers [4]. A special feature of this shift register is that the output amplitude can be externally controlled by adjusting the height of the two-phase non-overlapping clock, this feature being important for these target applications.

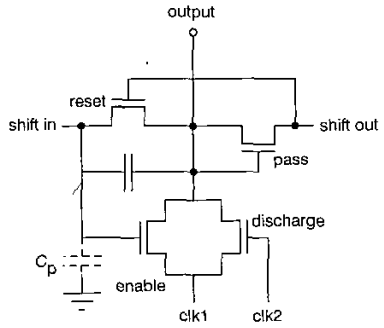


**Fig. 1** *One stage of shift register*

As shown in Fig. 1, each stage of the low power serial-to-parallel dynamic shift register discussed in this Letter consists of four non-ratioed minimum sized $n$-channel transistors and can be implemented in any standard CMOS process. A bootstrapping capacitor is used to overcome the threshold voltage drop of the $n$-channel pass transistor. The register has no DC power supply and is driven entirely by the two-phase clock, leading to low power dissipation. The clocks should be non-overlapping and if this requirement is not met, the register will not perform correctly [5]. Non-overlapping clocks are advantageous as fixed pattern noise (fpn) since capacitive clock feedthrough can be more easily controlled [6]. Power consumption and dissipation is an important parameter in modern VLSI design, as electronic devices increasingly become portable [7]. Power consumption therefore needs to be minimised, keeping the battery size practical for portable electronic devices.

*Structure of shift register:* Each stage of the shift register is non-inverting and consists of four transistors with an extra transistor at the input and output of the shift register as shown in Fig. 2. The added transistor at the input stage is required to clock the serial input pulse. The added transistor at the output stage is required to discharge the last bootstrap capacitor.

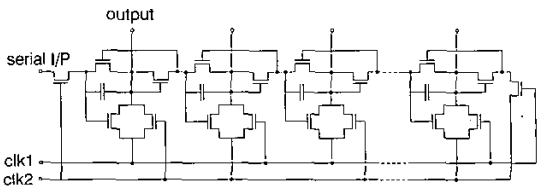


**Fig. 2** *Multiple stages of NRBL shift register*

*Operation of shift register:* With reference to Fig. 1, the operation of the circuit is as follows. The drain of each enable transistor is pulsed every clock period. The ouput of each shift element remains low until a high is enabled by the previous stage or the serial $I/P$. The ouput is charged up by the clock pulse when a high appears at the gate of the enable transistor. The output pulse does not drop by the threshold voltage $V_t$, of the $n$-transistor owing to the bootstrap action of the capacitor $C_b$. $C_b$, pulls up the enable transistor by $V_{boot}$, holding it at $V_{clk}+V_{boot}$,

$$V_{boot}=\frac{C_p}{C_b+C_p}V_{clk}$$

where $C_p$ is the parasitic capacitance to ground at the input. As the output is charged up to $V_{clk}$, $V_{clk}-V_t$ appears at the gate of the reset transistor and the following enable transistor via the pass transistor. As clk 1 starts going low the ouput drops accordingly. When the output is $2V_t$ below $V_{clk}$, the reset transistor turns on and resets the bootstrap capacitor. This causes the enable transistor to turn off when the output is at this level. When the next clock phase comes on (clk 2) the discharge transistor turns on and completes the discharge of the output. The bootstrap capacitor of the next stage is not charged as the gate of the pass transistor is now at a lower potential than its source. The same cycle repeats for the subsequent stages of the shift register. Note that the connection of the two clocks alternate between each stage of the shift register. A summary of the functions of each transistor are as follows:

*Enable transistor*: Connects clock to output when enabled by the previous stage.
*Reset transistor*: Resets the bootstrap capacitor.
*Pass transistor*: (i) passes initial current to charge up bootstrap capacitor of next stage, (ii) when output discharges, it turns off so that the bootstrap capacitor of the next stage does not discharge, (iii) provides a threshold voltage drop so that the reset transistor is kept hard off until the output potential drops.

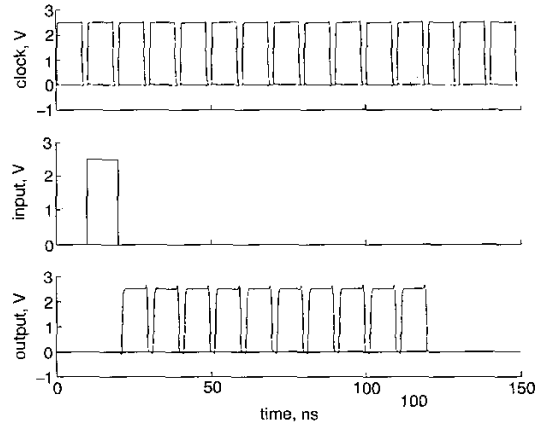


**Fig. 3** *Simulation results of NRBL shift register*

*Simulation and results:* Simulation of the dynamic shift register was performed with HSPICE using an industrial 0.25 μm CMOS process at 2.5 V clock voltage. The value of the bootstrap capacitance is determined by the value of $V_{boot}$ required and was chosen to be 15.46 fF. The shift register was simulated with a load inverter with size equivalent to 128 minimum size load transistors. Fig. 3 shows the operation of the shift register, with two non-overlapping clocks at 50 MHz. When the input pulse is clocked at the serial $I/P$, the output

pulses of each stage are as shown in Fig. 3. To make the simulations more creditable, a distributed clock tree is used to drive the stages of shift register. Table 1 shows comparison of different shift register.

**Table 1:** Comparison of different shift register cells

| | NRBL shift register | Dynamic shift register [1] | Shibata's shift register |
|---|---|---|---|
| Maximum speed (MHz) | 50 | 50 | 100 |
| Transistor/Stage | 4 | 6 | D-FF(~15) |
| Number of power supplies | 0 | 1 | 1 |
| Power dissipation per stage (mW) | 0.27 | 0.50 | 1.50 |

*Power dissipation:* The power dissipation of the dynamic shift register is minimal as only one stage is on at a time. The total power dissipation is therefore mainly due to the charging and discharging of the capacitance that each stage drives, $C_L$. This is equal to $C_L V_{clk}^2 f$, where $f$ is the clock frequency. Fig. 4 shows simulated results of power dissipation against varying voltage of operation, with load of 128 minimum transistors and with no load.

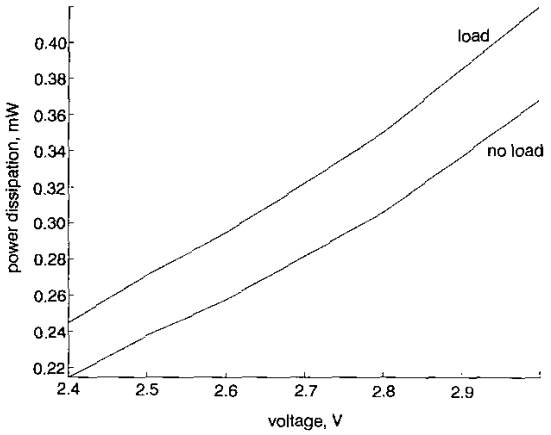


**Fig. 4** *Power dissipation against clock voltage*

*Conclusion:* A four-transistor per stage serial to parallel dynamic shift register has been designed and simulated with HSPICE using a 2.5 V, 0.25 μm CMOS process. It has been shown to drive a fan out of 128 with a very low power dissipation.

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## An open-loop clock deskewing circuit for high-speed synchronous DRAM

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An open-loop clock deskewing circuit (CDC) for high-speed synchronous DRAM is described. Unlike the conventional circuits, the CDC does not require an additional measure delay line, thus power consumption is reduced. The delay is measured directly from the main delay line and both the input and output ports of the delay line are movable. The CDC provides a deskewed clock within two clock cycles.

*Introduction:* The increasing data bandwidth of synchronous DRAM necessitates the use of a clock deskewing circuit to minimise the timing uncertainty. Several deskewing circuit techniques have been proposed to date, which can be classified as either open-loop or closed-loop. Open-loop deskewing circuits such as synchronous mirror delay (SMD) and hierarchical synchronous delay line (HSDL) have the advantage of much shorter locking time than closed-loop circuits [1, 2]. For example, SMD provides a deskewed internal clock in two clock cycles whereas several hundreds of clock cycles are taken in closed-loop CDCs. In conventional open-loop CDC, however, the power consumption is large because of the additional delay line required to measure the delay of the main delay line. Moreover, the accuracy of clock deskewing is determined by the matching between the main delay line and the measure delay line. In this Letter, an open-loop CDC is described where the delay is measured directly from the main delay line and therefore an additional measure delay line is not required.

*Open-loop CDC without measure delay line:* The architecture of the open-loop CDC without a measure delay line is shown in Fig. 1, the timing diagram of which is shown in Fig. 2. In these Figures, $\Delta t$ is the dummy delay to compensate for the delays of the clock input buffer and the data output buffer and DM is a delay measurer detecting the phase difference between *clkin* and *clkdly*. The output pulse width of DM is proportional to the phase difference between *clkin* and *clkdly*, i.e. the output of DM which is HIGH for '$T-\Delta t$'. The basic purpose of the CDC is to provide the output clock, *clkout*, delayed by '$T-\Delta t$' from *clkin*.

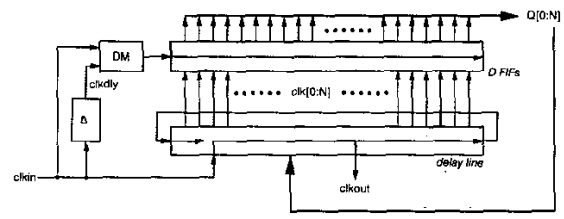


**Fig. 1** *Open-loop CDC without measure delay line*

Unlike conventional open-loop CDCs, both the input and output ports of the delay line are movable, as shown in Fig. 3. The output of DM which is HIGH for '$T-\Delta t$' is sampled by the array of $D-F/F$s which are clocked by the multiphase clocks $clk[0{:}N]$ generated from the delay line. The number of HIGHs in $Q[0{:}N]$ corresponds to the