GEC RESEARCH LABORATORIES
HIRST RESEARCH CENTRE
WEMBLEY MIDDLESEX HA9 7PP

SSD/188
D Z Abbott
January 1984

DESIGN DETAILS OF THE MA726 SILICON SCANNER FOR A 'HYBRID' SOLID-STATE IMAGE SENSOR

Abstract

This memo describes the principal design features of the MA726 nMOS 128 x 128 X-Y addressable array being produced on behalf of EEV for use as a signal read-out device as part of an experimental 'hybrid' image sensor.

Circulation

Abstract Only:

Sir Robert Clayton
Dr C Hilsum
Dr B J Isherwood
Dr I R Young
Dr D G Scotter
Dr L J Stagg
Dr R J Offen
Mr A Prince
Mr R L Rouse
Mr P A Crowther
Mr D L Lewis
Miss C Pettican

Mr G D Speake
Dr J C Williams
Mr D W Byatt
Dr J H Blythe
Mr J R Mark
Mr L W Gill — MRC, Gt Baddow
Mr O F Joseph
Mr J H Streeter
Mr R Greygoose
Mr G R Jordan
Mr D King
Mr P H Wisbey
Mr R A Wood

Full Copy:

Mr D H Roberts
Mr D E Hooper
Dr D V McCaughan
Mr D E H Smith
Mr J S Whitelegge
Dr C E C Wood
Dr S P Doherty
Dr L W Kennedy
Mr P Burton
Mr D J Burt
Mr R Lambert
Mrs S L Partridge
Dr T W Beck

1 Introduction

Development of solid-state image sensors at HRC is currently based on the technology of CCD frame transfer arrays. Whilst these devices can provide excellent white light sensitivity, the response is too low for colour TV as light at the blue end of the spectrum is absorbed in the polysilicon electrodes. Of the numerous approaches possible to overcome this difficulty, one of the more attractive [1] is a 'hybrid' sensor which uses a photoconductive layer deposited on a silicon scanner chip to physically separate the functions of photogeneration and signal read-out, as shown schematically in Figure 1. Since the whole area of the array is now overlaid with a high quantum efficiency photoconductor, improved sensitivity can result.

This memo describes an initial 128 x 128 element scanner chip, type number MA726, that has been designed for fabrication of experimental hybrid sensors at EEV. An X-Y addressable diode array has been chosen for this, as has been shown in Figure 1, although a CCD approach is also possible. The main reason for the choice is not one of inherent technical superiority but rather the chance to gain additional information as to whether the X-Y type of array can give a yield higher than CCD. This could arise from an essentially less complicated fabrication and the fact that point defects in the silicon are less likely to cause whole columns to be faulted. Against this, however, the devices are likely to have significantly higher noise. The main contribution being fixed pattern noise (FPN) caused by clock feedthrough onto the video output. However, off-chip FPN reduction techniques can be employed to increase the S/N to a viable level [2,5].

A further consideration in this choice of X-Y array is that the basic 128 x 128 element scanner (ie without the photoconductor) is itself photosensitive and may be useful as a simple-to-operate low-resolution sensor for access via a microprocessor in applications such as robotics. The basic scanner has a superior blue response to CCD, but against this is its reduced photosensitive area.

The basic operation of this sensor is discussed in Section 2 and image sensing with the incorporated photoconductive layer will be considered in Section 3.

2 Basic operation of an X-Y addressed array as an image sensor

Figure 2 shows the basic design of an X-Y addressed imaging array. Each element consists of a p-n photodiode and associated MOS switch, shown in detail in Figure 3a. Also included on-chip are MOS shift registers which act as horizontal and vertical scan generators. In operation, an optical image is focussed on to the array and photons incident on each photodiode generate electron-hole pairs in the underlying silicon (Figure 3a). As each photodiode is reverse-biased, electrons are swept up by the field in the depletion region and accumulate on the diode's self-capacitance. Holes are swept away and recombine in the bulk. If a sufficient amount of charge is collected to cause a photodiode to go into forward bias, electrons are injected into the substrate and may drift towards neighbouring diodes causing 'blooming'.

(i) The spectral response of the array can be tailored by careful choice of photoconductor material (eg a-Si:H, PbO etc).

(ii) Sensitivity is increased as a greater photosensitive area is presented to incident light.

(iii) Anti-blooming can be implemented by adjusting V_b such that the collected charge cancels the field, local to the photoconductor region under intense illumination, just before the blooming point occurs. Any further electron-hole pairs produced in this region, will simply recombine without significant lateral diffusion taking place.

An additional technique is to pulse V_b negative, for a short duration during the blanking period, so as to purposely dump photocharge into the substrate for recombination [6]. However, it is not clear whether significant blooming control would result in our case or not. A definite improvement in blooming characteristics could be obtained by shielding exposed regions of silicon (in our case, the horizontal polysilicon lines) by means of an opaque grid under the photoconductor. This method has been reported with a measure of success in [6].

4 Description and design of the MA726 X-Y array

The MA726 was designed in a simple 6 μm nMOS LOCOS process to be compatible with requirements of low cost and high yield. The overall chip size is 6.5 mm square and the array elements were designed to a 40 μm pitch (see Figure 4).

The basic X-Y array requires only 6 photolith stages in fabrication (Appendix 1) and then can function as an imager for test purposes. In order to hybridise the silicon array and photoconductive layer, a further 2 photolith stages are required to place top level metal contacts on the diodes. The photomasks required for each stage are described in Appendix 1. A special substrate contact mask (layer 6) is included so that the field oxide can be selectively etched in order to make good ground contact to the underlying P^+ channel stop. The substrate contact ring is indicated in Figure 5 displaying the general chip layout (shown only in Metal I for clarity). As can be seen, the main array connects to external electronics via 16 bonding pads, many of which can be made common in practice. The various circuit elements indicated in the diagram are discussed in detail in the following subsections.

4.1 Addressable photodiode structure

The addressable photodiode is simply a MOS transistor with a large source region (20 x 30 μm^2) exposed to light. The drain region is connected to a metal column line (Figure 4) which also shields it from incoming light. The gate is connected to a horizontal address line which is pulsed high in order to transfer collected photocharge from source to drain for read-out. With reference to Figure 6 three particular features of the photodiode are discussed:

Taking the area of the diode as 20 x 30 μm^2 and the area of the p-well as 10 x 16 μm^2, C_O is calculated to be ~0.1 pF. Assuming V_V = +5 V and assuming standard TV rates, τ = 0.5 μs giving I_S ~400 nA. This is about the same level of signal current present in existing CCD imagers at HRC.

(iii) P+/epi layer

The P^+ underlying the epi layer serves 2 main purposes

(a) Photocharges generated in the P^+ substrate by deep penetrating long wavelength radiation have a short diffusion length and so are prevented from degrading the spatial resolution of the array.

(b) If the diodes go into forward bias a portion of the blooming charges will be absorbed in the P^+ layer.

4.2 Dynamic nMOS shift registers

The shift registers used for scanning the array in the horizontal and vertical directions are both of the same design on a 40 μm pitch. The basic shift register is of the 2-phase low power dynamic design with non-inverting stages. Each stage contains 5 MOS transistors, one of which acts as a bootstrap capacitor to overcome the common problem of threshold drops.

Important features of circuit operation, layout and performance are now highlighted:

(I) Circuit operation

With reference to Figure 7, the circuit operation is as follows. The drain of an 'enable' transistor is pulsed every (say) ϕ_1 clock period. The output of each 'shift' element remains low until a high is enabled by the previous stage. When a high appears at the gate of an 'enable' transistor, the output is charged up by the clock pulse. This pulse does not get cut off at a threshold voltage under +10 V due to the action of the bootstrap capacitor, C_B. C_B pulls up the gate of the 'enable' transistor by ΔV, holding it at 10 + ΔV volts, where

$$\Delta V = \left(\frac{C_B}{C_B + C_p} \right) V_\phi$$

and C_p = stray capacitance to ground at input of each stage

V_ϕ = clock pulse amplitude (+10 V)

As the output is charged up to a full +10 V, (10-V_T) appears at the gates of the 'reset' and the following 'enable' transistors via the 'pass' transistor. When $\phi 1$ starts going low the output drops. When the output is $2V_T$ below 10 V, the 'reset' transistor turns on and neutralises the charge on the plates of the bootstrap capacitor. This causes the 'enable' to turn off when the output is at this level. When the next phase comes on ($\phi 2$) the 'discharge' transistor turns on and completes the discharge of the output. [As the gate of the 'pass' transistor is now at a lower potential than its source, the bootstrap capacitor of the next stage is not discharged]. The same cycle repeats for the next stage and so on. The functions of each of

(III) Performance

The layout was arranged so as to minimise C_p giving 0.05 pF. Against this value, a C_B of 0.6 pF was chosen as giving satisfactory bootstrap action. In view of these capacitances, and the load capacitance (C_L) that each stage drives, a measure of performance is obtained by calculating the maximum frequency of operation, f_{max}. Taking the 'enable' transistor as operating in saturation, the following differential equation is set up

$$\beta \left[(\eta - 1)\ V_S + (V_o - V_T) \right]^2 = (C_L + C_p\ \eta)\ dV_S/dt$$

where V_S = source voltage (connected to O/P)

$\eta = C_B/C_B + C_p)$

$V_o = (V_G - V_S)$ @ $t = 0$

Solving this equation, f_{max} can be calculated from the time for the output to rise up to V_ϕ = 10 V and is given by

$$f_{max} = \frac{\beta\ (V_o - V_T)}{2\ (C_L + C_p\ \eta)\ V_\phi} \cdot \left[(V_o - V_T) - (1 - \eta)\ V_\phi \right]$$

The value of the parameters can be taken as, V_o = +8 V

η = 0.92

β = 70 $\mu A/V^2$

$C_L = C_B + C_p + 2\ Cg$ = 0.75 pF (for vertical register)

$C_L = C_B + C_p + Cg$ + cap. of gate line = 7.5 pF (for horizontal register)

f_{max} ~100 MHz fast vertical register

f_{max} ~3 MHz slow horizontal register

These figures indicate that the scanner chip should operate at frequencies above normal TV rates with the given design values of C_p and C_B. SPICE simulations indicated correct operation at normal TV rates.

The power dissipated by the shift registers is due to the charging and discharging of the capacitance that each stage drives. As only one stage is active at any time, the total power dissipation is simply $C_L V_\phi^2 f$. For standard TV rates the fast register dissipates ~75 μW and the slow register dissipates ~6 μW. These figures are favourably two to four orders of magnitude lower than those of ratio-type shift registers that are known to give rise to thermal heating problems in large arrays.

4.3 Column-to-video line multiplexer

The multiplexer (Figure 2) comprises a row of transistor switches, that connect the column lines, in turn, to the video line. The switching sequence is controlled by the vertical shift register that is connected in parallel with the multiplexer. In design, the layout of the individual

where η is the fraction of signal charge read out in t seconds. Taking C_C = 5 pF and R_j ~500 Ω, η = 99%, C_V = 50 pF as severest estimates gives t = 100 ns. This implies that all the column lines can be read out in less than a standard line time.

4.4 Output

Two output options are provided on-chip:

(a) A bonding pad connection direct to the video line, for an external virtual earth amplifier.

(b) A source follower with reset transistor connected to the video line.

The source follower should be designed to have a large gate capacitance so as to minimise voltage noise at the output. However, this capacitance adds to that of the video line resulting in increased kTC noise. Therefore, a compromise is met by choosing a gate capacitance equal to that of the video line. Within this constraint a large aspect ratio (W/L) was chosen for a high g_m and low Johnson noise; namely W = 600 μm and L = 6 μm. Metal contacts are made along the whole width of source and drain so as to eliminate series resistance.

4.5 Protection circuitry

The gate protection consists of a current limiting resistor in series with a diode and spark gaps (Figure 9). The operation of each element is described as follows.

(a) Diode

The purpose of the diode is to form a conduction path to substrate when incorrect voltages appear at the input. For negative voltages it goes into forward bias and for positive voltages above V_{BD} ~ +20 V it goes into zener breakdown. Substrate contacts are placed close to the diode (Figure 9) to reduce the internal series resistance, R_D.

(b) Resistor, R_S

The resistor, ideally, has no voltage across it under normal conditions and drops nearly all the voltage under conditions of diode conduction. Thus, the diode does not get damaged. R_S must be sufficiently massive so as not to vapourise, itself,and sufficiently small so as not to slow down the input waveform.

(c) Spark gaps

If a large voltage appears at the input, the spark gap points concentrating the field cause the air in between to ionise and provide a conducting path to substrate. Spark gaps are provided both in Metal I and Metal II. A 45° sawtooth geometry is documented [22] as being optimum for absorbing the impulsive electrical energy and giving a breakdown of ~200 V when unpassivated. ½ μm flats have been put on the tips to aid pattern generation.

standard TV rates, thus proving the design. A further batch (no 2569) is presently being fabricated with a modified implant schedule (Appendix 3) to give the correct value of threshold voltage. Two control wafers without the deep p-well implant have been included in this batch for purposes of comparison.

When samples of the second batch (no 2569) are received, they will be tested as image sensors in their own right before hybridisation with a photoconductive layer. Both yield figures and values of signal-to-noise ratio will be determined in order to assess the viability of the device. If unacceptable figures are obtained, then the option of designing a CCD interline transfer array, for hybridisation, remains open. However, all being well, development of the X-Y addressed array could include further investigation into noise reduction techniques, anti-blooming shielding and increased array size with interlaced elements.

References

Arrays

(1) Terui, Y et al
A Solid-State Colour Image Sensor Using
ZnSe-ZnCdTe Heterojunction Thin-Film Photoconductor
Proc SSCC, (1980)

(2) Ravich, L E
Electronic Imaging Round Table
Electronic Imaging, May (1983)

(3) Ravich, L E
Electronic Imaging Round Table, Part II
Electronic Imaging, August (1983)

(4) Koike, N et al
MOS Area Sensor : Part I
IEEE Trans ED, Vol ED-27, No 8, (1980)

(5) Ohba, S et al
MOS Area Sensor : Part II
IEEE Trans ED, Vol ED-27, No 8, (1980)

(6) Chikamura, T et al
Blooming Characteristics Of A Solid-State
Imager Overlaid With A Photoconductor
IEEE Trans ED, Vol ED-29, No 12, (1982)

(7) Burt, D J
P8600 : Epitaxial Substrate Version
HRC Memo SSD/82, July (1982)

(8) Barbe, D F
Charge-Coupled Devices
Springer-Verlag, New York, (1980)

(9) Terui, Y et al
A CCD Imaging Device Having A PLOSS Structure
IEDM, (1981)

(10) Van der Spiegel, J
Discrete And Integrated Photosensitive Devices
Solid-State Sensors and Transducers,
Katholieke Univ Leuven, Belgium, (1982)

(11) Tsukada et al, T
Solid-State Colour Imager Using An a-Si:H
Photoconductive Film
IEDM, (1981)

(12) Plummer, J and Meindl, J
MOS Electronics For A Portable Reading
Aid For The Blind
IEEE J of Solid State Circ, April (1972)

Protection circuits

(22) Cohen, S and Caswell G
An Improved Protection Circuit For
CMOS/SOS Arrays
IEEE Trans ED, Vol ED-25, No 8, (1978)

(23) Lezlinger, M
Gate Protection Of MIS Devices
IEEE Trans ED, April (1971)

(24) Hickernell, F and Crawford, J
Voltage Breakdown Characteristics
Of Closed Aluminium Arc Gap Structures
On Oxidised Silicon
IEEE Proc Rel Phys, (1977)

(25) Linholm, L and Plachy, R
Electrostatic Gate Protection
Using An Arc Gap Device
Proc IEEE 11th Annual Rel Phys Symp, (1973)

(26) Agatsuma, T and Ishii, S
An Analysis Of Equivalent Circuit With
Gate Protection In MOS Devices
IEEE Trans ED, Vol ED-25, No 4, (1978)

(27) Jackets, A E et al
Gate Protection Devices For
MOS Integrated Circuits
HRC Memo No 1018/SC/26R7, (1969)

(28) Jarvis, D B et al
Gate Protection Devices for
MOS Integrated Circuits
HRC Memo No 956/SC/22R7, (1968)

(29) Christian, S R
Testing The Input Protection
Circuit Of the MA361
HRC Memo No SOS/4, (1979)

Appendix 1

Imaging X-Y addressable array

Device : MA726

Size is 6.5 mm square (including 1/2 scribe channel)

Smallest dimension is 6 μm

1/2 scribe lane width is 150 μm + extra 25 μm for overlapping during step-and-repeat

Pitch of array 40 μm

Process : nMOS

3" wafer diameter

Negative resist

Contact printing

Pattern generation : Electromask 2000

Electromask metric

Grand total of 175116 exposures

Tape density of 800 BPI (bits per inch)

Taping border is on one separate level

Masks : Optically generated

For contact printing

To produce 80 chips per wafer

Step-and-repeat distance 6.5 mm or 256 thou (1 thou =25.4 μm)

9 masks in a set

4" by 4" by 0.060" stepped submasters

4" by 4" by 0.060" anti reflective chrome working plates

3 sets of working plates acquired

Layer :		Enclosed area appears :	Field :
1	Active area	Clear	Darkfield
2	Implant (Option 1, well)	Opaque	Lightfield
3	Implant (Option 2, blanket)	Opaque	Lightfield
4	Polysilicon	Clear	Darkfield
5	Contact holes	Opaque	Lightfield
6	Substrate contact	Opaque	Lightfield
7	Metal I	Clear	Darkfield
8	Via holes	Opaque	Lightfield
9	Metal II	Clear	Darkfield

Appendix 2

Pin out - 24 pin dil

1	SUB	Substrate
2	PROT IN	Protection test circuit
3	$\phi H2$	Horizontal clock phase-2
4	$\phi H1$	Horizontal clock phase-1
5	S_{Hi}	Horizontal shift register input
6	NC	NC
7	NC	NC
8	TG)	20 x 12 μm^2 test transistor (no implant)
9	TS)	
10	TD)	
11	V_{DD})	Reset transistor
12	ϕR)	
13	V_{DD})	Output transistor
14	O/P)	
15	VIDEO	
16	V_{DD})	Vertical shift register output
17	S_{Vo})	
18	NC	NC
19	$\phi V2$	Vertical clock phase-2
20	$\phi V1$	Vertical clock phase-1
21	S_{Vi}	Vertical shift register input
22	V_{DD})	Horizontal shift register output
23	S_{Ho})	
24	PROT OUT	Protection test circuit

Appendix 3

Principal process parameters

Gate oxide thickness ~700Å

Field oxide thickness ~5000Å

P-type epi resistivity 20-40 Ωcm

thickness 20-25 μm

doping 5 x 10^{14} ions cm^{-3}

P^+-type substrate doping ~10^{18} ions cm^{-3}

S/D implant 5 x 10^{15} cm^{-2} @ 80 keV

Deep p-well implant 1 x 10^{12} cm^{-2} @ 160 keV

	Batch 2558	Batch 2569				
Wafer Nos	All	1-5	6-10	11-15	16-20	21-22
Overall V_T p-implant @ 30 keV [10^{11} cm^{-2}]	1.3	4.5	4.5	7	7	7
P^+-channel stop @ 60 keV [10^{14} cm^{-2}]	5	1	2	1	2	2

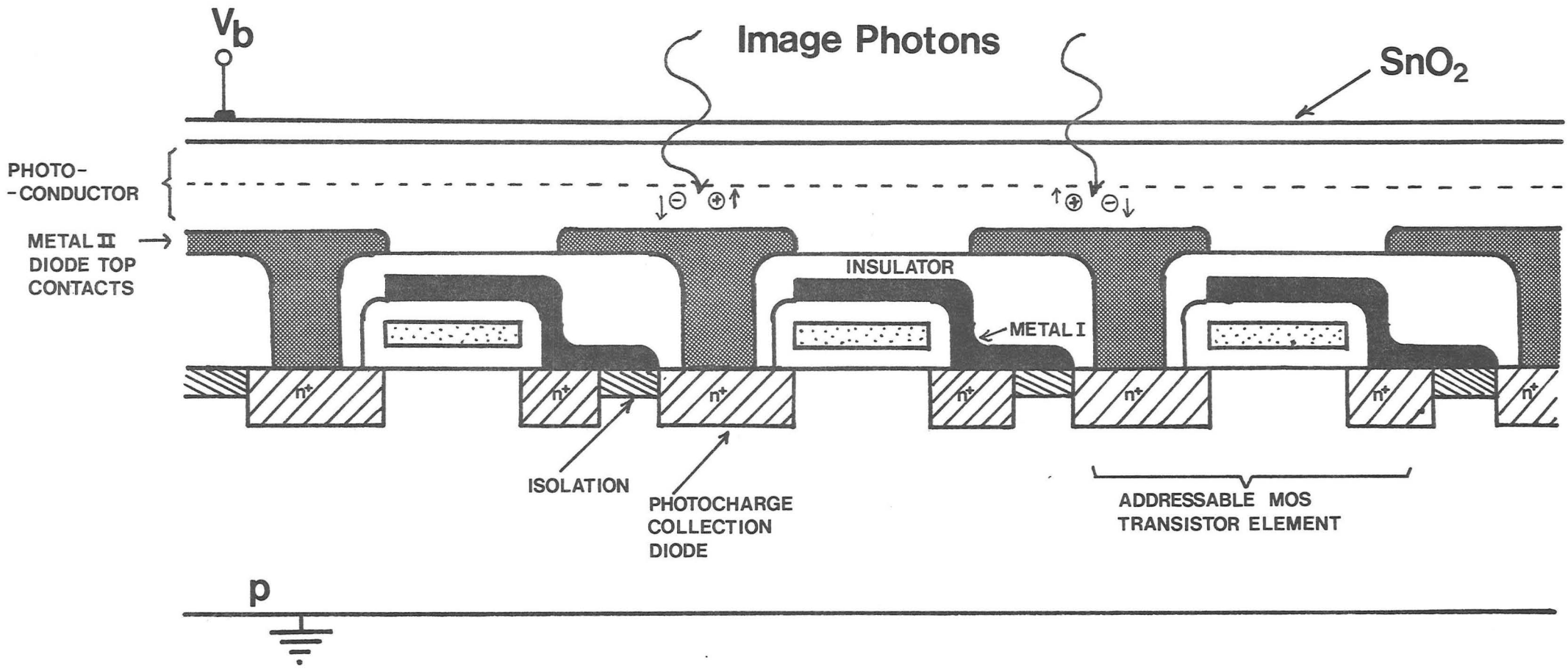


Fig.1 Hybrid X-Y Addressed Array Image Sensor.

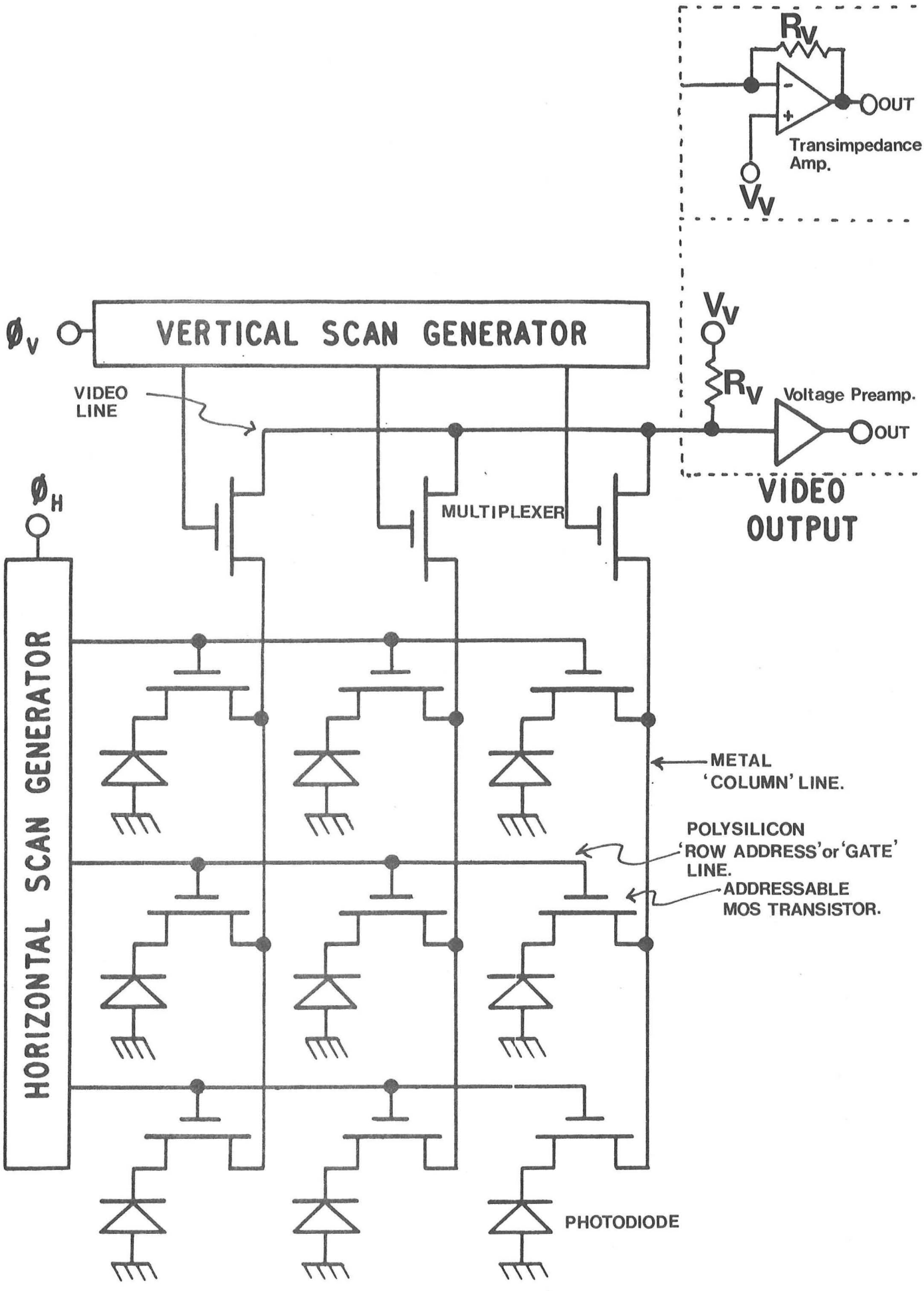


Fig. 2 Basic X-Y Array.

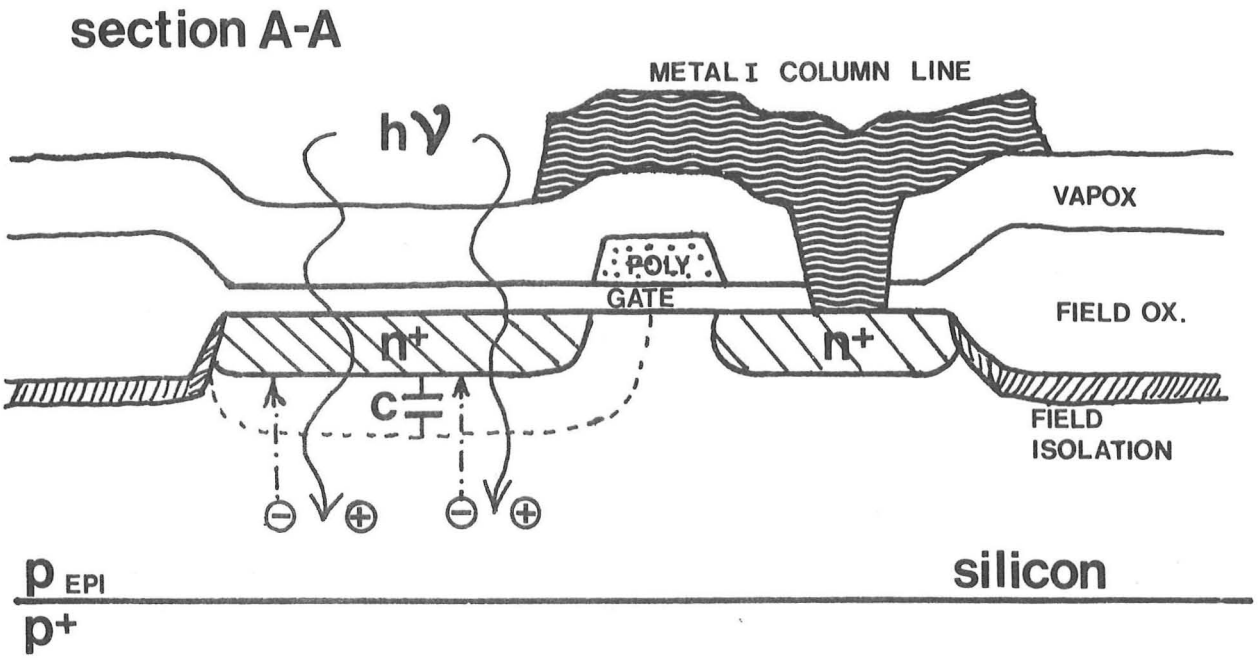


Fig.3a Section Through Pixel Showing Photocollection.

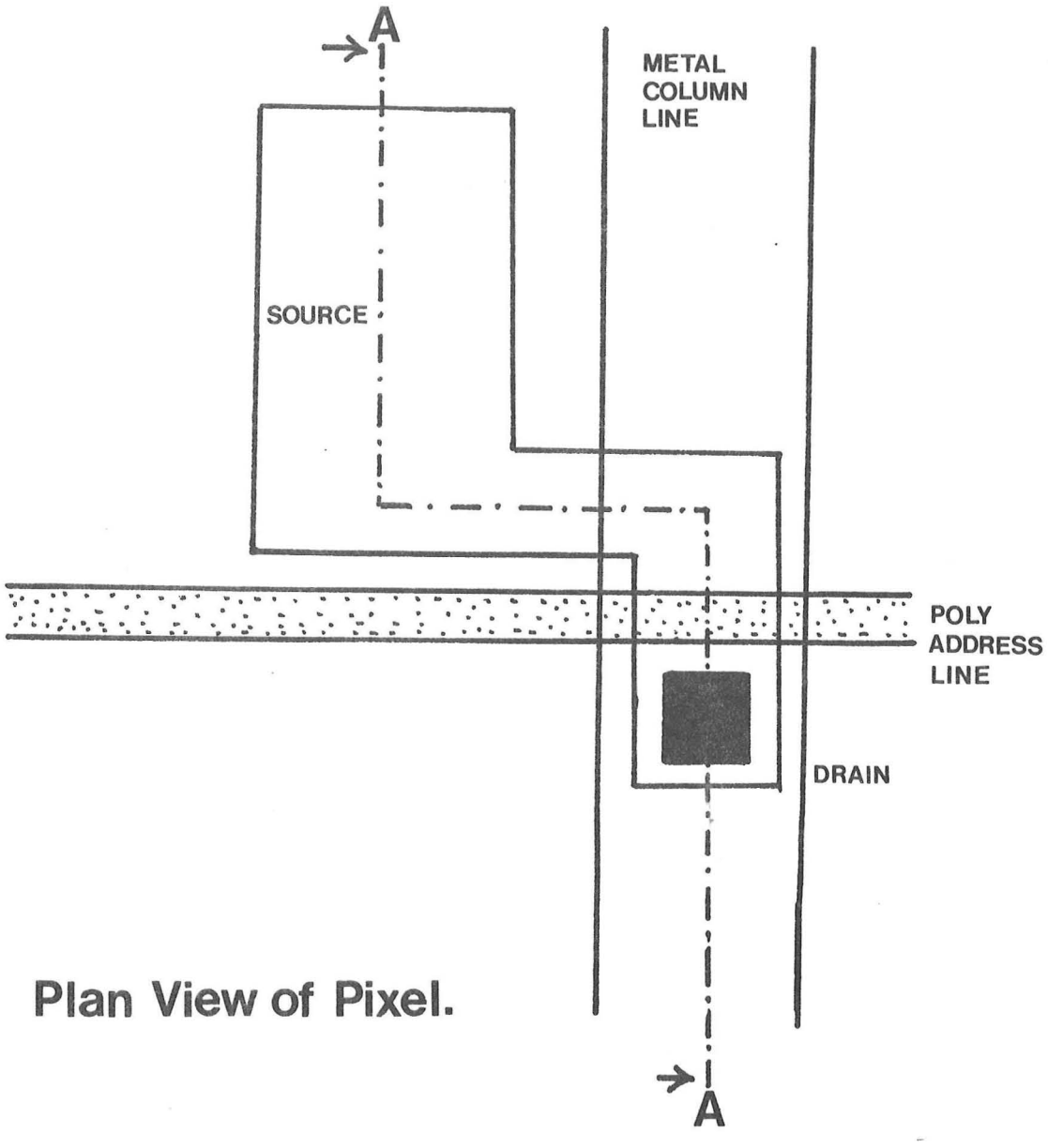


Fig.3b Plan View of Pixel.

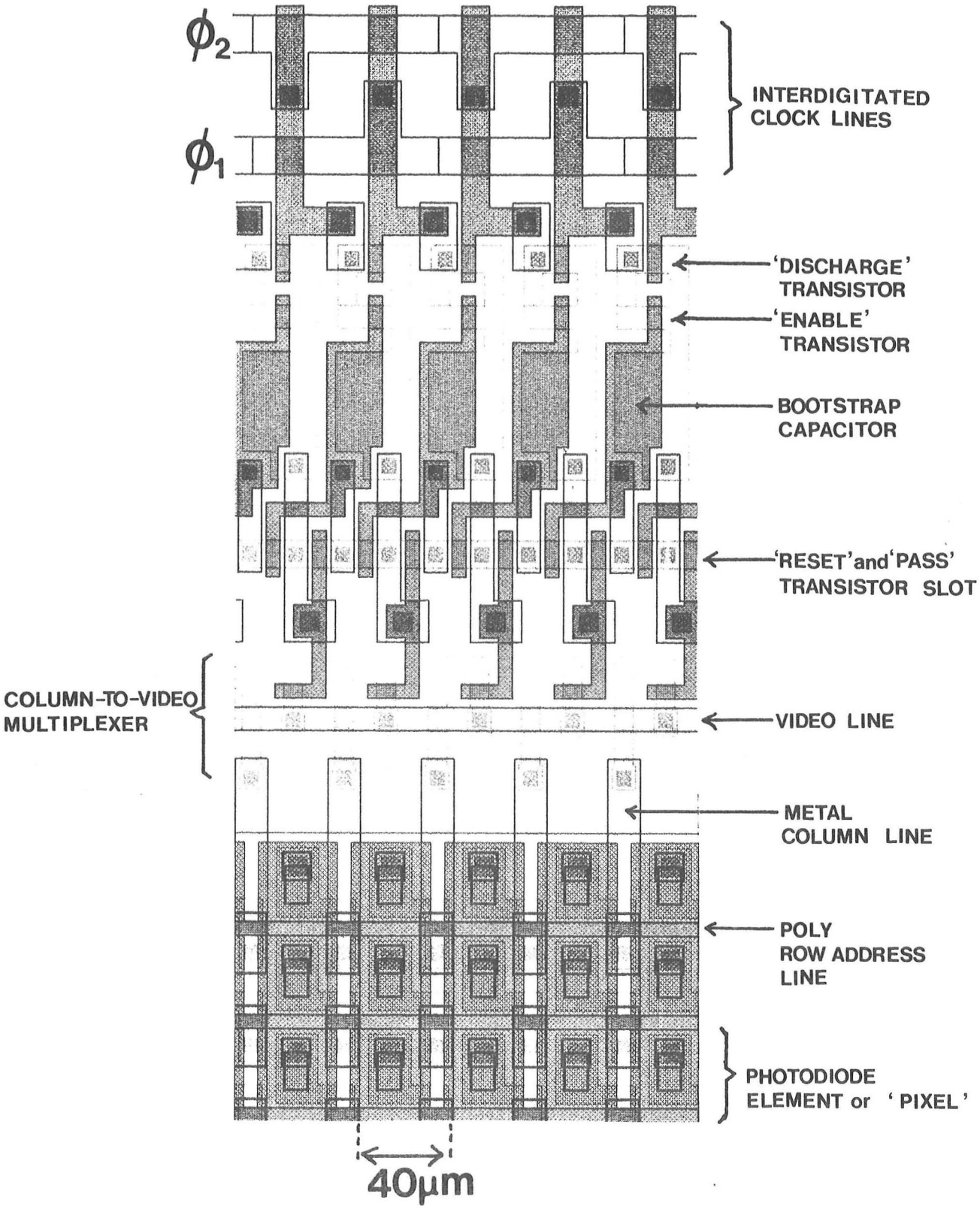


Fig.4 Photodiode and Scan Element Layout.

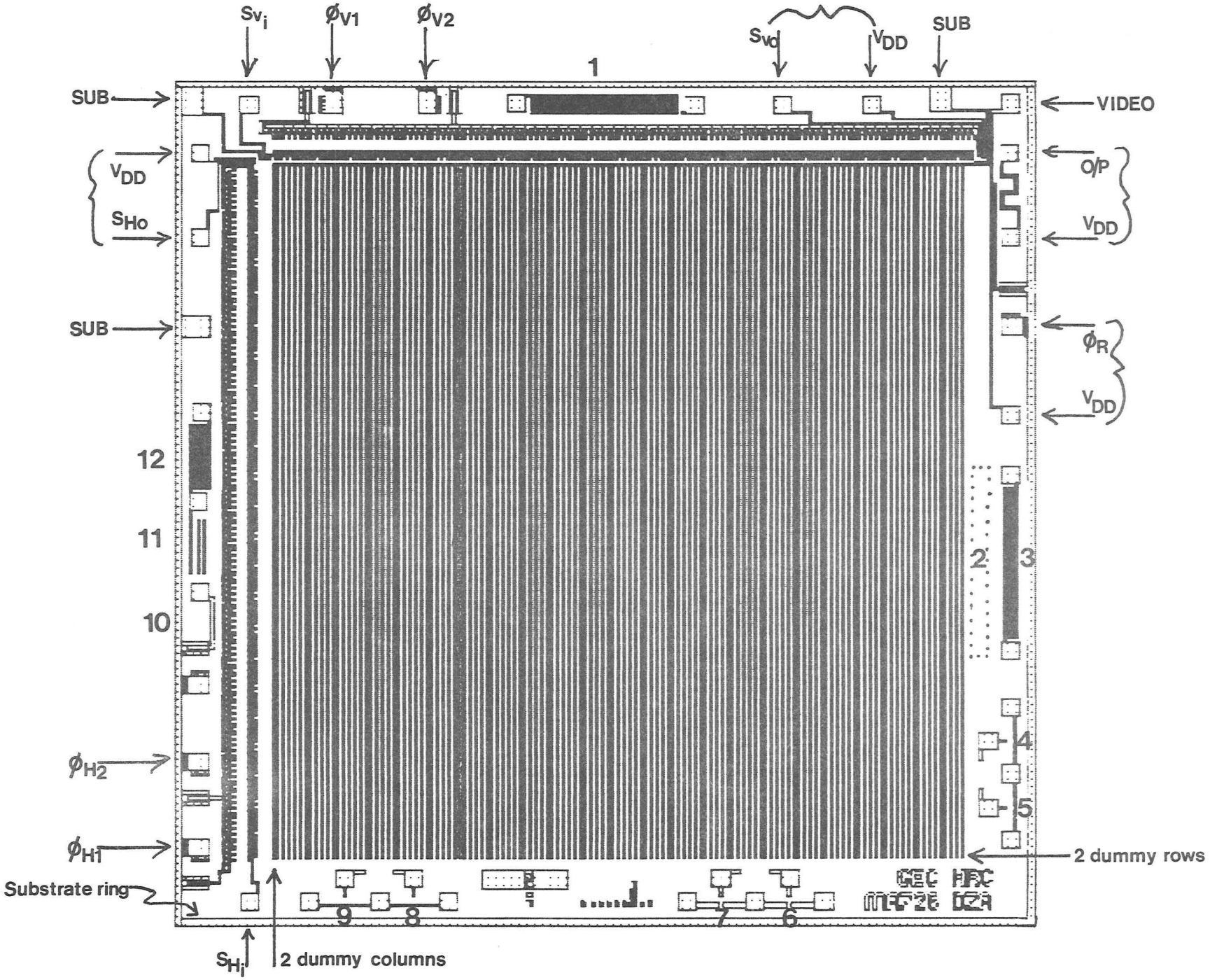


Fig.5 Overall Layout in Metal I.

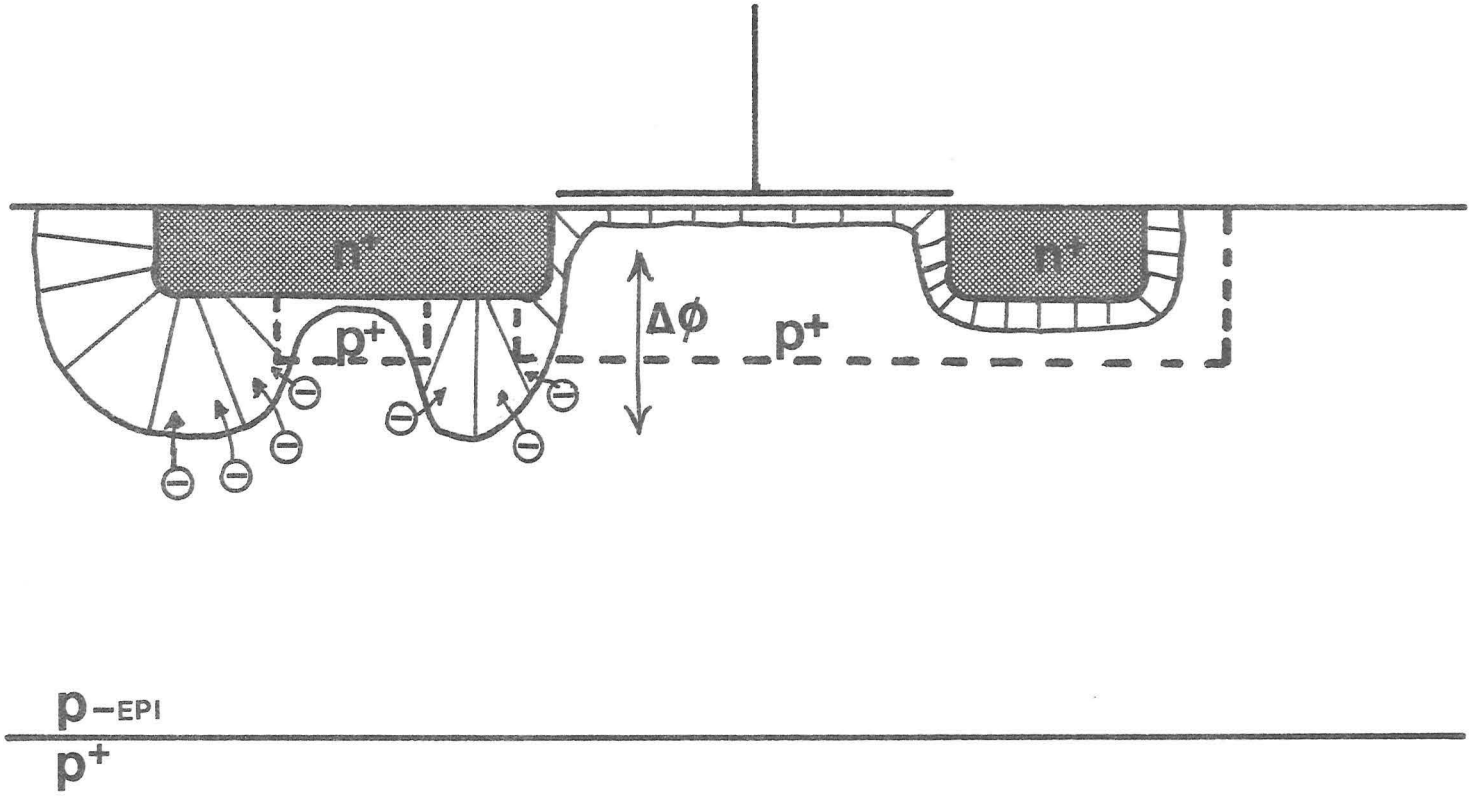
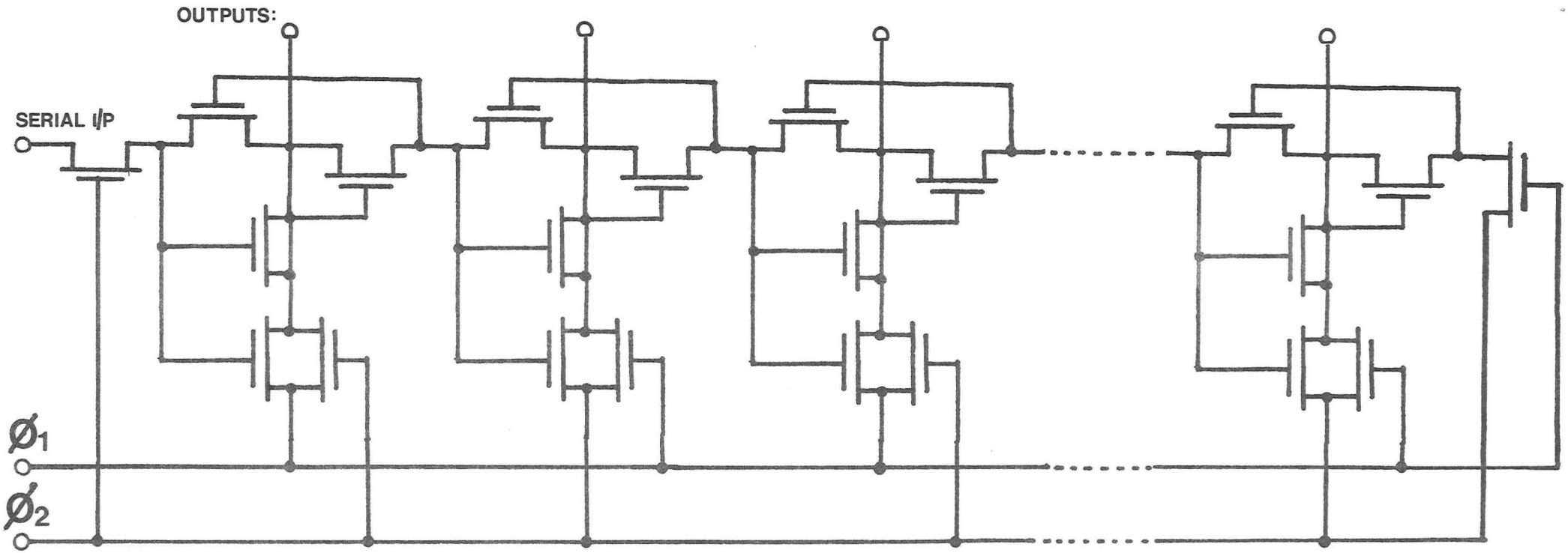


Fig.6 Effect of p-Well Implant Scheme.



Shift element :

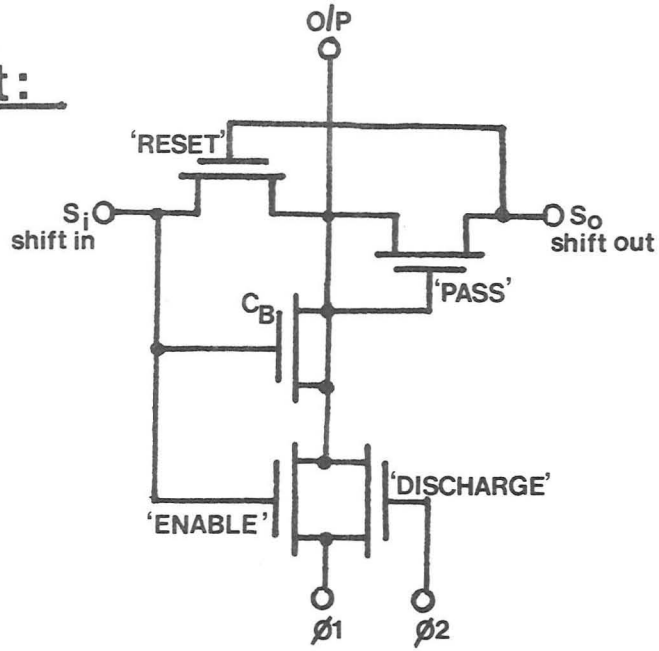
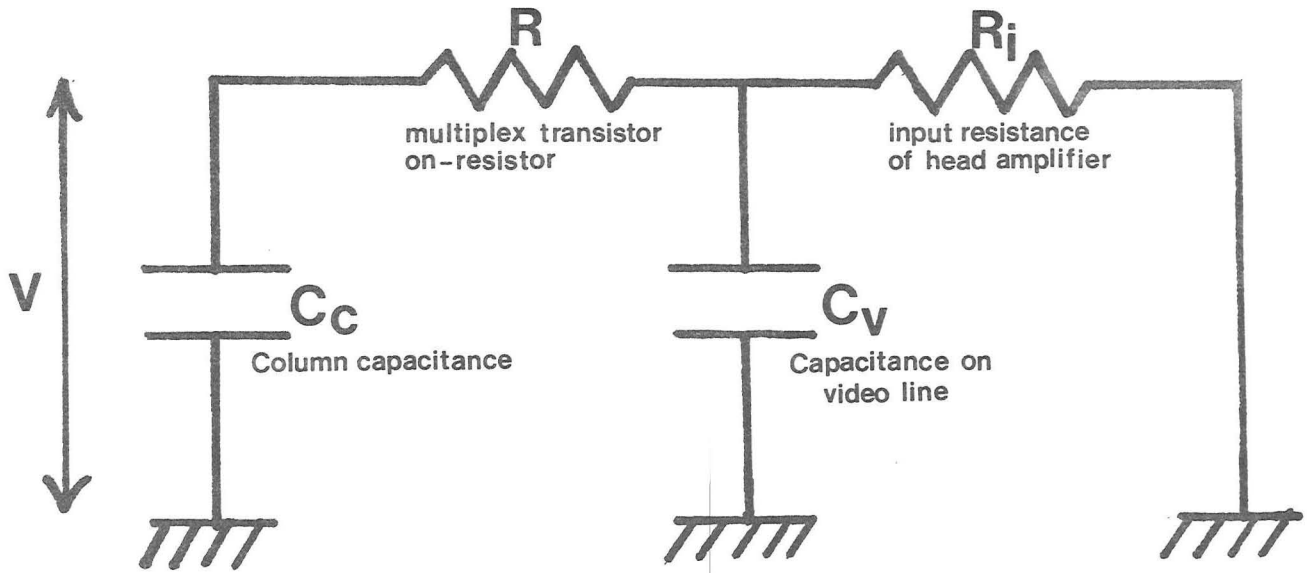
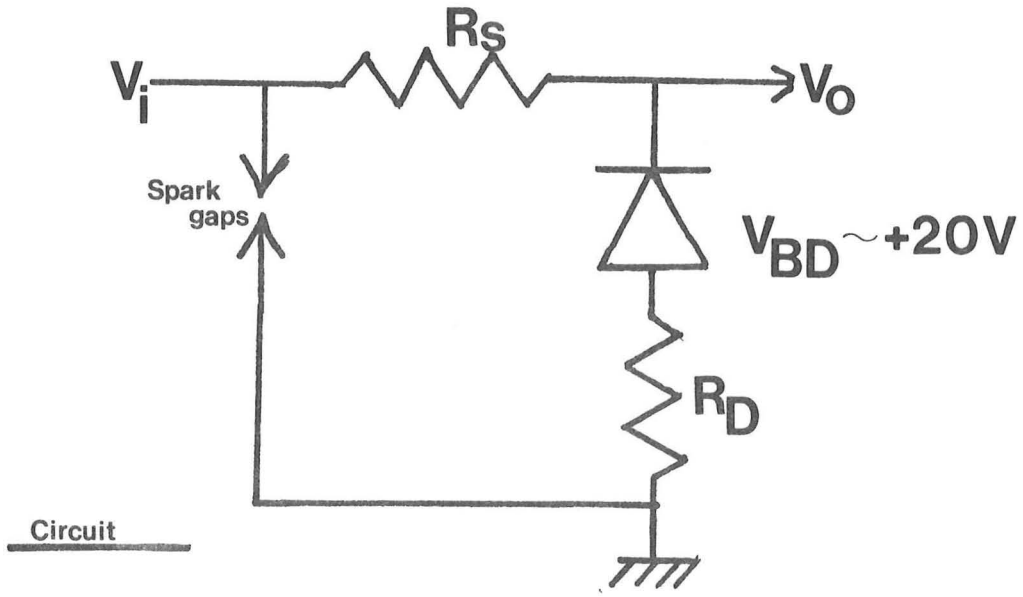


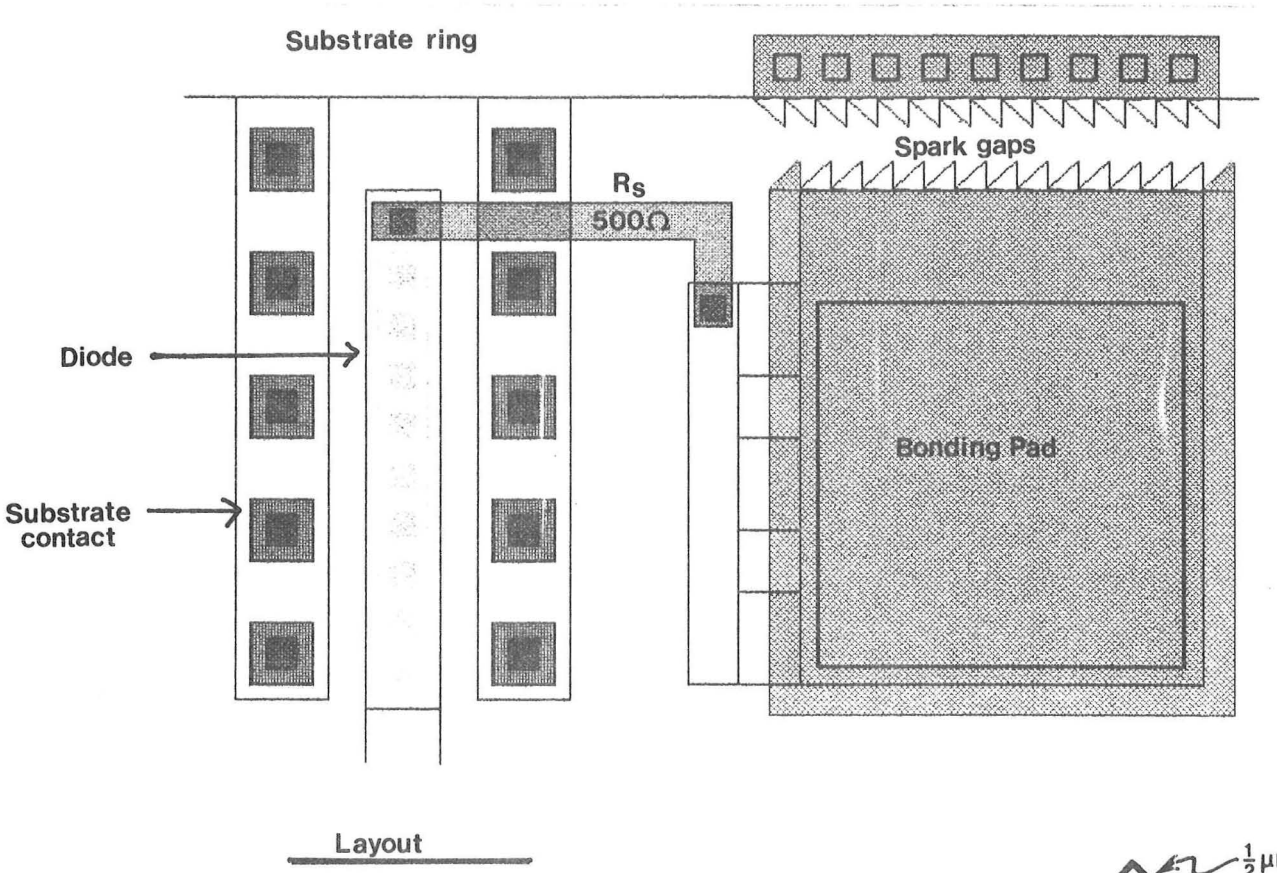
Fig.7 Shift Register Circuit.



$$\ddot{V} + \left\{ \frac{1}{C_V R} + \frac{1}{C_C R_i} + \frac{1}{C_C R} \right\} \dot{V} - \frac{V}{C_V C_C R R_i} = 0$$

Fig. 8 Column-to-Video Line Switching: Equivalent Circuit.





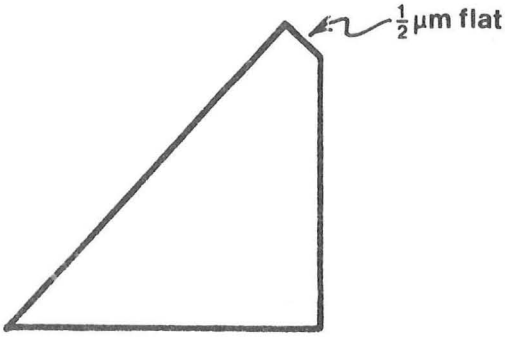


Fig.9 Gate Protection.