The relative permittivity of the ferroelectric film decreases and hence affects the dielectric resonator electric field and changes the resonant frequency.

The $TE_{01\delta}$ resonant mode was examined at room temperature using a vector network analyser HP8720C (Hewlett-Packard (Now Agilent), Palo Alto, CA, USA, with 1 Hz resolution).

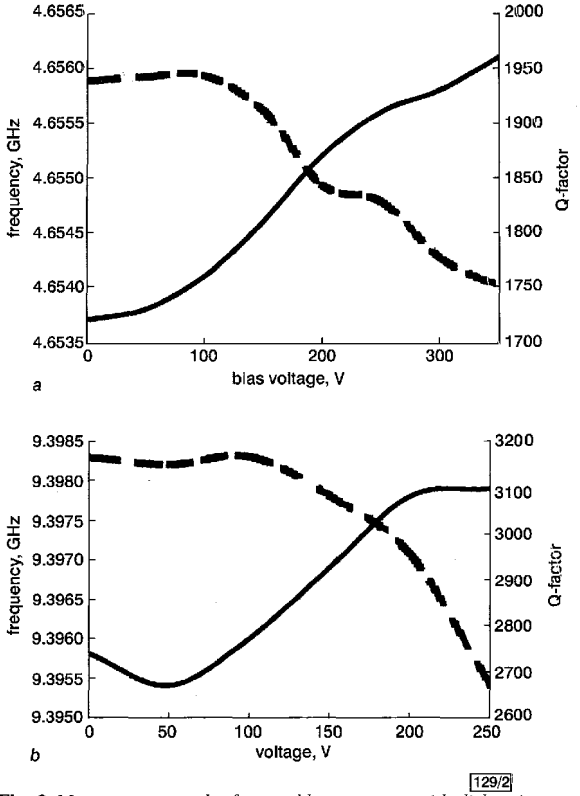

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Fig. 2 *Measurement results for tunable resonators with dielectric resonator of CTNA and Al_2O_3*

a CTNA
b Al_2O_3
——— centre frequency shifting
– – – – loaded Q-factor of resonator

Results and discussions: Experimental data are shown in Fig. 2. The resonant frequency of the $TE_{01\delta}$ mode was shifted by 2 MHz while the $Q.f$ was above 5000 GHz (for the CTNA sample) and above 10000 GHz (for the Al_2O_3 sample). The low tuning ratio might be explained by the BSTO film quality. Because the thick film of BSTO was deposited onto a silver substrate, there was an upper limit of approximately 900°C for the sintering temperature as the melting point of silver in air is 961°C. Sintered at 900°C, the BSTO film had 50 to 60% porosity, which reduced the effective ε_r and hence the tuning capability (measured at 1 MHz, the electrical tuning ratio $[C(0\,V) - C(350\,V)]/C(0\,V)$ was ~10%, while the Q-factor was ~80). It is thought that reducing porosity of BSTO film using alternative methods of preparation such as sol-gel, pulsed laser deposition, magnetron sputtering, etc., will improve the performance.

The loaded Q-factor for all the samples, measured at maximum applied DC bias, was at least over 1000. These values compare very favourably with the results presented by Beall *et al.* [2] (Q-factor ≃ 300), Buer and El-Sharawy [3] (Q-factor ≃ 3000 which drops to 500), Vendik *et al.* [4] (Q-factor ≃ 2500 which drops to 500). Moreover, the results achieved in [3, 4] are measured at cryogenic temperatures of 4 and 77 K, respectively.

Trinogga, in [5], reported a 200 MHz tuning but there are no data concerning the Q-factor of the circuit. Finally, we measured a high tuning ratio when the DR was placed directly on the ferroelectric element without a spacer. However, the Q-factor then reduced to ~100, a value too low for device application.

Conclusions: A method for fast, electrical tuning of a dielectric resonator is proposed. The results verify its underlying principle. By using a ferroelectric element, fast resonant frequency tuning of a DR while maintaining a useful Q-factor is possible. This is because the coupling between the high Q DR and the low Q ferroelectric element (film) can be sensitively balanced by altering the distance between the ferroelectric and the DR. This is achieved simply by adjusting the spacer height. Further improvements in the device are possible by using higher quality BSTO films prepared by alternative techniques.

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Low power, high speed, charge recycling CMOS threshold logic gate

P. Celinski, J.F. López, S. Al-Sarawi and D. Abbott

A new implementation of a threshold gate based on a capacitive input, charge recycling differential sense amplifier latch is presented. Simulation results indicate that the proposed structure has very low power dissipation and high operating speed, as well as robustness under process, temperature and supply voltage variations, and is therefore highly suitable as an element in digital integrated circuit design.

Introduction: As the demand for higher performance, very large scale integration processors with increased sophistication grows, continuing research is focused on improving the performance, area efficiency, and functionality of the arithmetic and other units contained therein. Low power dissipation has become a major issue demanded by the high performance processor market to meet the high density requirements of advanced VLSI processors. The importance of low power is also evident in portable and aerospace applications, and is related to issues of reliability, packaging, cooling and cost.

Threshold logic (TL) was introduced over four decades ago, and over the years has promised much in terms of reduced logic depth and gate count compared to traditional AND-OR-NOT (AON) logic-gate based design. However, lack of efficient physical realisations has meant that TL has, until recently, had little impact on VLSI. Efficient TL gate realisations have recently become available, and a number of applications based on TL gates have demonstrated its ability to achieve high operating speed and significantly reduced area [1].

Both static and dynamic TL gate implementations have been devised. Purely static gates such as neuron-MOS suffer from lim-

ited fan in [1], typically less than 12 inputs. In addition, some of the existing dynamic gates have relatively high static power dissipation, and some require multiple clock phases [1, 2], introducing the drawbacks associated with clock signal routing cost, clock skew and clock power dissipation. Although the dynamic approach proposed in [3] dissipates no static power, it will be shown that its dynamic power dissipation is comparable to the total power dissipation of other existing approaches.

In this Letter we propose a new realisation for CMOS threshold gates which operates on a single phase clock, is capable of high-speed operation, is suitable for high fan-in gate implementation and has a very low overall power dissipation.

Threshold logic: A threshold logic gate is functionally similar to a hard limiting neuron. The gate takes n binary inputs X_1, X_2, ..., X_n and produces a single binary output Y. A linear weighted sum of the binary inputs is computed followed by a thresholding operation. The Boolean function computed by such a gate is called a threshold function and it is specified by the gate threshold T and the weights w_1, w_2, ..., w_n, where w_i is the weight corresponding to the ith input variable X_i [4]. The output Y is 1 if $\Sigma_{i=1}^{n} w_i X_i \geq T$, and 0 otherwise. Any threshold function may be computed with positive integral weights and a positive real threshold, and all Boolean functions can be realised by a threshold gate network of depth at most two [4]. A TL gate can be programmed to realise many distinct Boolean functions by adjusting the threshold T. For example, an n-input TL gate with $T = n$ will realise an n-input AND gate and by setting $T = n/2$, the gate computes a majority function.

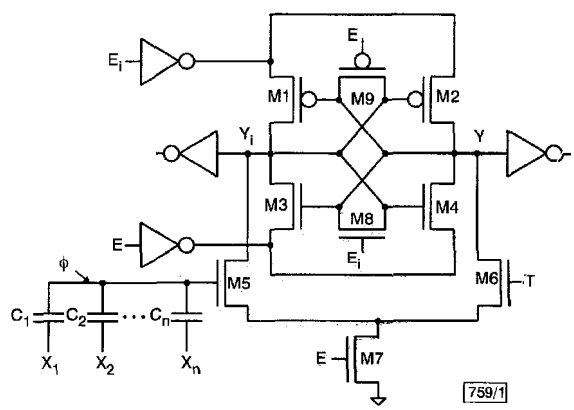

Fig. 1 *Proposed CRTL gate structure*

Charge recycling threshold logic (CRTL): Fig. 1 shows the proposed circuit structure for implementing a threshold gate with positive weights and threshold. It is based on the charge recycling asynchronous sense differential logic (ASDL) developed by Bai-Sun *et al.* [5]. The main element is the sense amplifier (cross-coupled transistors M1–M4) which generates output Y and its complement Y_i. Precharge and evaluate is specified by the dual enable clock signals E and its complement E_i. The inputs X_i are capacitively coupled onto the floating gate ϕ of M5, and the threshold is set by the gate voltage T of M6. The potential ϕ is given by $\phi = \Sigma_{i=1}^{n} C_i X_i / C_{tot}$, where C_{tot} is the sum of all capacitances, including parasitics, at the floating node. Weight values are thus realised by setting capacitors C_i to appropriate values. Typically, these capacitors are implemented between the polysilicon 1 and polysilicon 2 layers, although alternatives, such as trench capacitors available in DRAM processes, may obviously also be used.

The ASDL comparator architecture from which the proposed CRTL gate is derived implements high performance, energy efficient operation by recycling charge which has already been drawn from the supply. The enable signal E controls the precharge and activation of the sense circuit. Transistors M8 and M9 equalise the outputs. The logic gate has two phases of operation, the evaluate phase and the equalise phase. When E_i is high the output voltages are equalised. When E is high, the outputs are disconnected and the differential circuit (M5–M7) draws different currents from the formerly equalised nodes Y and Y_i. The sense amplifier is activated after the delay of the enable inverters and amplifies the difference in potential now present between Y and Y_i, accelerating the transition. In this way the circuit structure evaluates if the weighted sum of the inputs, ϕ, is greater or less than the threshold T, and a TL gate is realised.

To ensure reliable operation, the gate layout must be symmetrical to minimise the transistor mismatches and interconnects must be of similar length and width to eliminate interconnect-related mismatch. The delay of the enable inverter needs to be sufficiently large so that the output nodes have sufficient voltage difference at the start of sensing.

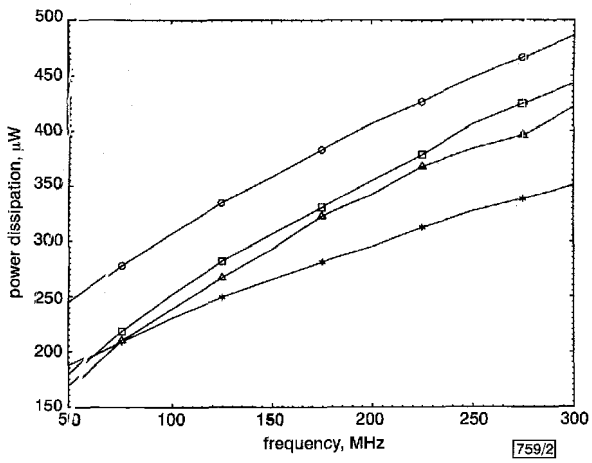

Fig. 2 *Power dissipation against frequency*

—○— clocked-neuron-MOS
—□— CCCL
—△— LPTL
—✳— CRTL

To evaluate and compare the performance of the proposed CRTL gate against other CMOS TL gate implementations, a 20-input majority gate ($T = 10$, achieved by setting voltage $T = V_{dd}/2$), was designed in a 0.25 μm process. The 20-input majority function was also implemented using clocked-neuron-MOS [1], CMOS capacitor coupling logic (CCCL) [2] and the TL structure reported in [3] (LPTL). The unit capacitance value used in each implementation was 5 fF. To compare the power dissipation, each of the gates was designed to have similar delay, output rise and fall times, and was loaded by equally sized inverters. All transistors were of minimum length for each implementation and transistor widths were selected to achieve the above timing requirements. All inputs to each gate were switched such that during each evaluation cycle the minimum majority or minority was achieved (11 out of 20 inputs were high or low, respectively). Also, the power dissipated in the inverters driving the clock and data inputs was included in the total power dissipation measured for each gate. Fig. 2 shows the HSPICE power dissipation simulation results for each of the gates against operating frequency for a 2 V supply. As shown in the Figure, for a typical operating frequency of 200 MHz, CRTL improves power dissipation by between 15 and 30% over the other CMOS threshold gate implementations.

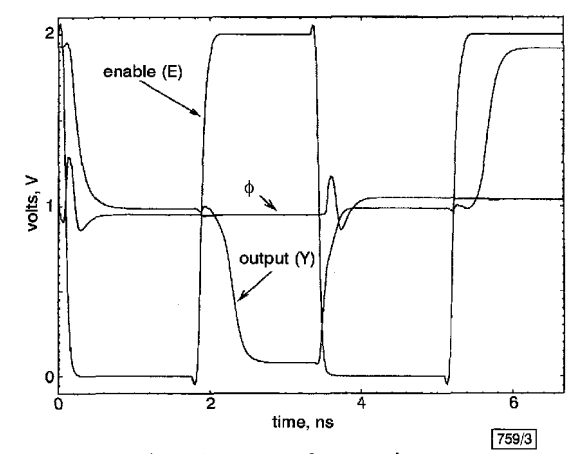

Fig. 3 *Input, enable and output simulation results*

To ensure correct behaviour under process and operating point variations, the proposed gate was tested at 45 corners (V_{dd} at 2, 2.5 and 3 V, process Slow-Slow, Slow-Fast, Fast-Slow, Fast-Fast and Typical-Typical, and temperature at –25, 75 and 125°C). Fig. 3 shows the transient waveform results from the HSPICE simulation for the 2 V-typical-75°C corner at 300 MHz. Simulation results of the 20-input majority gate also indicate that the CRTL gate can operate even at frequencies over 400 MHz with low power dissipation (below 400 μW) under worst case conditions (V_{dd} = 2 V, 125°C, Slow-Slow transistor corner).

Conclusions: A new CMOS threshold-logic gate has been proposed. A 20-input majority gate has been designed and simulated using the proposed CRTL structure to demonstrate its operation. A comparison with other TL realisations shows that this threshold gate has very low power dissipation. The gate is able to operate at clock frequencies of over 400 MHz, and it is robust under process, supply voltage and temperature variations.

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Effects of temperature on dispersion of high slope dispersion compensating fibres

V.M. Schneider

Several experimental high dispersion and dispersion slope fibres are measured for their temperature dependence. Supermode resonant coupling is responsible for an interesting trend in the dispersion and dispersion slope variation with temperature.

Introduction: The rapid development of the optical layer network and the increase in system transmission rates imposes serious restrictions for residual chromatic dispersion in the optical link. One of the best approaches to minimise the penalty by dispersion for a large bandwidth of wavelengths is the use of dispersion-compensating fibres. It is known that very high dispersion values can be achieved by supermode coupling in planar waveguides [1]. The same principle can be used to explain the high chromatic dispersion achieved in coaxial-like fibres [2] and the sensitivity of these profiles to macro-bending [3]. Recently, chromatic dispersion measurements, for a range of different class of fibres that are not exclusively dispersion-compensating fibres, showed an interesting trend [4]. It was found that an increase in the temperature dependence of the chromatic dispersion was related to the dispersion slope of the fibre. However, most of the fibres measured did not have very large dispersion and dispersion slope values, unlike those typically governed by supermode coupling.

In this Letter, several experimental fibres that presented high dispersion and dispersion slopes based on supermode resonance are measured, and the results are discussed. It is shown that the thermal characteristics of this class of fibres can vary widely, even when there is only a small change in the profile.

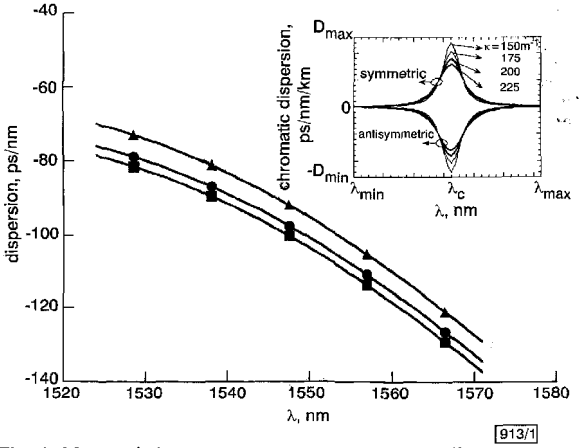

Fig. 1 *Measured dispersion against wavelength at different temperatures for coaxial-like fibre*
—■— –5°C
—●— 25°C
—▲— 55°C
Inset: Theoretical schematic diagram for supermode resonance and definition of resonance wavelength λ_c
Different coupling coefficients κ scale the dispersion amplitude while changing λ_c shifts the whole curve sideways.

Origin of the effect: A simple approach to analyse the dispersion characteristics of a fibre with a coaxial structure, such as the dispersion compensating fibres, is the use of supermode theory. In this case, the coaxial fibre is broken into two individual guides, the core and the ring guide. This is the analogy in cylindrical co-ordinates to a simple directional coupler in rectangular co-ordinates. A coupling coefficient κ is assumed between the core and the ring, as well as a dephasing term.

Since these individual guides have different group velocities and dispersion characteristics, the coupled system usually experiences a phenomenal increase in negative dispersion for the antisymmetric supermode. This happens near the critical resonant wavelength λ_c, where the dephasing is null, leading to resonant coupling. Very high negative dispersion and dispersion slope values can be achieved by careful design for appropriate coupling coefficients κ, group velocities differences, and resonant wavelength. For the fibres shown here, the theoretical λc was in the range of 1600 to 1700 nm.

However, due to this same resonant nature of the coupling, any small shift mainly in λ_c, or secondarily in the previously mentioned parameters, that are all a function of the chosen designed profile, will lead to considerable shifts in dispersion values. This can be observed in Fig. 1, for an experimental fibre with a minor plot showing the typical shape around λ_c, where large dispersion changes arise from temperature variations with typical operating ranges. Percentage variations of dispersion or dispersion slope related to ambient temperature at a certain wavelength can be calculated using

$$D(\%) = (D(55°C) - D(-5°C))/(D(25°C)) \quad (1)$$

This effect near λ_c is a major direct consequence of the changes in waveguide dispersion of the coupled system, and not in the minor material dispersion variation around the zero dispersion wavelength λ_o [4].

Experimental setup and results: To confirm this hypothesis, a number of experimental coaxial-like fibres with different profiles and reasonably high dispersion values per kilometre were chosen. The samples were allocated in a thermal chamber and dispersion measurements taken at the temperatures of –5, 25 and 55°C. A