Reference spur suppression technique using ratioed current charge pump

N. Kamal, S.F. Al-Sarawi and D. Abbott

Reference spurs are one of the main problems in integer-N phase-locked loops (PLLs). A ratioed current charge pump is proposed to suppress reference spur magnitude in the PLL output. The ratioed current charge pump can be implemented by resizing the source and drain network of the charge pump. A formula to calculate the ratioed current and transistor size is presented. The reference spur magnitude for a PLL with a ratioed current charge pump is compared to a conventional charge pump PLL, resulting in about 4 dBc/Hz improvement in the reference spur magnitude.

Introduction: Reference spurs are mainly caused by the phase/frequency detector (PFD) and charge pump (CP) circuit non-idealities, namely CP current mismatch, PFD delay, CP switching delay, CP current rise and fall time characteristics, and CP current leakage. These non-idealities cause a periodic ripple in the tuning voltage of a voltage-controlled oscillator (VCO), resulting in spurs at multiple reference frequency offsets from the carrier signal.

Several approaches have been carried out to suppress reference spurs in the phase-locked loop (PLL) output. One of these techniques involves lowering the VCO gain, while maintaining a wide VCO output frequency range [1, 2]. These techniques require a complex circuit design and modification of the PLL architecture. Another technique involves minimising the CP current mismatch and minimising the CP current leakage. Minimising CP current mismatch can be implemented by using a gain boosting circuit [3, 4] or a calibrated CP [5, 6]. Meanwhile, minimising the current leakage can be implemented by using a leakage current compensation circuit [7]. However, although CP current is matched, reference spurs still exist because of other circuit non-idealities such as switching delay. In this Letter, we propose a ratioed current CP to improve reference spur suppression. The ratioed current minimises the voltage ripple on the VCO tuning voltage that is caused by CP current mismatch, PFD delay and switching delay. In the following analysis we use the long-channel transistor model. The same analysis can also be applied for short-channel devices.

CP current mismatch and PFD delay: Owing to second-order effects, such as channel length modulation and the difference in parameters between nMOS and pMOS transistors, CP current, I_{up} and I_{dn} as shown in Fig. 1 are not matched [3]. Since the total charge transfer to the loop filter must be zero, the amount of PFD delay (t_{PFD}) either in the UP or DN signal has to be adjusted to compensate for the current difference as shown in Fig. 2. If I_{up} is larger than I_{dn}, the DN signal (t_{dn}) must be slightly longer than the UP signal (t_{up}), and vice versa. The current mismatch and differences in the PFD delay result in ripples on the VCO tuning voltage, resulting in reference spurs in the PLL output.

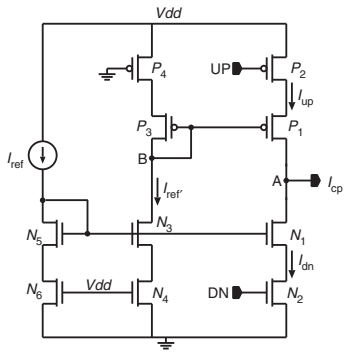

Fig. 1 *CP circuit*
Transistors N_1, N_3, N_5, P_1 and P_3 construct current sources for I_{up} and I_{dn} generation

Assuming that I_{up} is larger than I_{dn}, therefore, $t_{dn} = t_{PFD} + t_{diff}$, where t_{diff} is the PFD delay difference between the UP and DN signals, and $t_{up} = t_{PFD}$ as shown in Fig. 2a. Since the total charge transfer is zero when the PLL is in the locked state, $t_{diff_{Iup}}$ can be written as

$$\begin{aligned} I_{up}t_{up} - I_{dn}t_{dn} &= 0 \\ I_{up}t_{PFD} &= I_{dn}\left(t_{PFD} + t_{diff_{Iup}}\right) \\ t_{diff_{Iup}} &= t_{PFD}\left(\frac{I_{up}}{I_{dn}} - 1\right) \end{aligned} \tag{1}$$

If I_{dn} is larger than I_{up}, then $t_{up} = t_{PFD} + t_{diff}$, and $t_{dn} = t_{PFD}$ as shown in Fig. 2*b*, and $t_{diff_{Idn}}$ can be written as

$$t_{diff_{Idn}} = t_{PFD}\left(\frac{I_{dn}}{I_{up}} - 1\right) \tag{2}$$

According to (1) and (2), t_{diff} has a linear relation with both the CP current mismatch and PFD delay, and the ripple voltage in the VCO tuning voltage is proportional to t_{diff}. A higher t_{diff} results in a higher ripple amplitude, and hence increases the magnitude of the reference spurs.

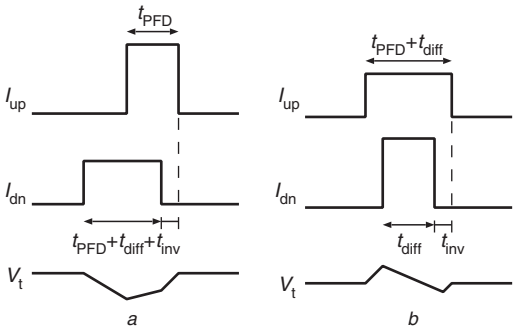

Fig. 2 *Effect of current mismatch to PFD delay (t_{PED}), and UP signal switching delay on ripple amplitude in VCO tuning voltage*
a $I_{up} > I_{dn}$
b $I_{dn} > I_{up}$

Switching delay: A switching delay only exists in the CP UP switch, which is caused by an added inverter. The effect of the switching delay on the ripple magnitude in the VCO tuning voltage depends on the CP current, either I_{up} larger than I_{dn} or vice versa.

Controlling the delay in the UP signal helps to reduce the ripple amplitude in the tuning voltage, hence decreasing the reference spur magnitude. Therefore, slightly larger I_{dn} when compared to I_{up} helps to reduce the reference spur magnitude. The optimum I_{dn} to I_{up} ratio is presented in the next section.

Ratioed current CP: In the ratioed current CP, the current source is designed so that I_{dn} is slightly larger than I_{up}. Before implementing the design, an optimum I_{dn} to I_{up} ratio has to be determined. When I_{dn} is larger than I_{up}, the I_{up} current switches ON longer than I_{dn}, so that the total charge transfer to the loop filter is zero. I_{up} is delayed by the switching delay of the UP switch, t_{inv}.

The optimum ripple amplitude in the VCO tuning voltage, ΔV, is achieved when $\Delta V_{top} = \Delta V_{bottom}$, and this can be attained if the I_{up} duration has $2t_{inv}$ longer than I_{dn}. Therefore, the time difference between I_{up} and I_{dn} is given by

$$t_{diff} = 2t_{inv} \tag{3}$$

Substituing this into (2) results in

$$\frac{I_{dn}}{I_{up}} = \left(\frac{2t_{inv}}{t_{PFD}} + 1\right) \tag{4}$$

This equation gives the ratio of I_{dn} to I_{up} in terms of switching delay (t_{inv}) and PFD delay (t_{PFD}). Parameters t_{inv} and t_{PFD} can be extracted from a transistor-level simulation.

The CP current is provided by a current mirror circuit as shown in Fig. 1. The sizes of N_3 and N_5 are similar to N_1, whereas the sizes of N_4 and N_6 are similar to N_2. Also, the sizes of P_3 and P_5 are similar to P_1.

Considering the channel modulation effect, I_{up} and I_{dn} are given by

$$I_{up} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{P_1}\left(\left|V_{GS_{P_1}}\right| - \left|V_{th_p}\right|\right)^2\left(1 + \lambda_p\left|V_{DS_{P_1}}\right|\right) \quad (5)$$

$$I_{dn} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{N_1}\left(V_{GS_{N_1}} - V_{th_n}\right)^2\left(1 + \lambda_n V_{DS_{N_1}}\right) \quad (6)$$

where λ_p and λ_n are the channel length modulation effect parameters for pMOS and nMOS, respectively.

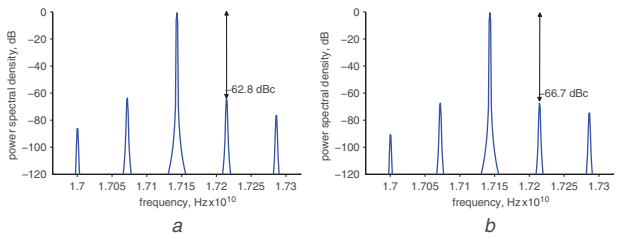

Fig. 3 *Reference spur magnitude comparison*

a Conventional CP
b Ratioed current CP

Referring to Fig. 1, as the sizes of P_1 and P_3 are similar, hence $\left(\frac{W}{L}\right)_{P_1} = \left(\frac{W}{L}\right)_{P_3}$ and the length of N_1 is similar to N_3; therefore the I_{dn} to I_{up} ratio can be simplified to

$$\frac{I_{dn}}{I_{up}} = \frac{\left(|V_{GS_{P_3}}| - |V_{th_p}|\right)^2\left(1 + \lambda_p|V_{DS_{P_3}}|\right)}{\left(|V_{GS_{P_1}}| - |V_{th_p}|\right)^2\left(1 + \lambda_p|V_{DS_{P_1}}|\right)} \times \frac{W_{N_1}\left(V_{GS_{N_1}} - V_{th_n}\right)^2\left(1 + \lambda_n V_{DS_{N_1}}\right)}{W_{N_3}\left(V_{GS_{N_3}} - V_{th_n}\right)^2\left(1 + \lambda_n V_{DS_{N_3}}\right)} \quad (7)$$

For a minimum ripple voltage magnitude, I_{dn} has to be larger than I_{up} by a ratio that is given by (4). Substituting this equation into (7), and solving for the W_{N_1} to W_{N_3} ratio results in

$$\frac{W_{N_1}}{W_{N_3}} = \left(\frac{2t_{inv}}{t_{PFD}} + 1\right)\frac{\left(\left|V_{GS_{P_1}}\right| - \left|V_{th_p}\right|\right)^2\left(1 + \lambda_p\left|V_{DS_{P_1}}\right|\right)}{\left(\left|V_{GS_{P_3}}\right| - \left|V_{th_p}\right|\right)^2\left(1 + \lambda_p\left|V_{DS_{P_3}}\right|\right)} \times \frac{\left(V_{GS_{N_1}} - V_{th_n}\right)^2\left(1 + \lambda_n V_{DS_{N_1}}\right)}{\left(V_{GS_{N_3}} - V_{th_n}\right)^2\left(1 + \lambda_n V_{DS_{N_3}}\right)} \quad (8)$$

Owing to channel length modulation, $V_{DS_{P_1}}$, $V_{GS_{P_1}}$, $V_{DS_{N_1}}$ and $V_{GS_{N_1}}$ vary according to the CP output voltage; therefore the ratio of W_{N_1} to W_{N_3} will also vary. For the reference spur analysis, only the VCO tuning voltage at the centre of VCO tuning frequency is considered. This is because at the centre frequency the VCO has its maximum gain, resulting in a maximum reference spur at that point. Therefore, the ratio of W_{N_1} to W_{N_3} was adjusted to result in a tuning voltage that operates the VCO at its centre tuning frequency.

Results: The reference spurs for two different PLLs are compared as shown in Fig. 3. The first PLL employs a conventional CP, whereas the second PLL uses the proposed ratioed current CP. Reference spur magnitude is obtained from a transient analysis at the transistor-level simulation. PLL output in the locked state is captured, and power spectral density (PSD) of the signal is calculated and plotted in Fig. 3. For the PSD calculation, an FFT with a length of 2^{19} and a Hamming window were used. The spectra in Fig. 3 show that the PLL with ratioed current gives a lower reference spur magnitude (− 66.7 dBc/Hz) when compared to the conventional CP PLL (− 62.8 dBc/Hz).

Conclusions: A ratioed current CP has been proposed for reference spur suppression in the PLL output. The CP optimum current ratio calculation has been presented. The schematic-level simulation shows that the ratioed current CP assists in reducing the reference spur magnitude by about 4 dBc/Hz. The proposed technique can be implemented with other reference spur suppression techniques to further reduce the reference spur magnitude.

25 March 2013
doi: 10.1049/el.2013.1010
One or more of the Figures in this Letter are available in colour online.

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