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Accurate Reference Spur Estimation using Behavioural Modelling

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***Abstract*—Reference spur is a periodic noise that can be observed at the output of an integer-N phase-locked loop (PLL). This noise is dominated by circuit non-idealities in phase/frequency detector (PFD) and charge pump. The spur magnitude is linearly related with Voltage Controlled Oscillator (VCO) gain. Estimating this noise using transistor level simulation is time consuming. Therefore, in this paper we present a Simulink behavioural model to accurately estimate the reference spur. PFD delay, charge pump current mismatch, rise and fall times effect and switching delay, in addition to non-linearity in the VCO gain, are all included in this model. The proposed model was used to estimate the reference spur for an 18.5 GHz PLL and the results were compared with transistor level simulation, and show less than 3% difference in the result.**

***Keywords*-Reference spur estimation, PLL modelling, very high frequency PLL, charge pump modelling, phase/frequency detector modelling.**

I. Introduction

A Phase-Locked Loop (PLL) based frequency synthesizer is one of the important circuit modules in an RF transceiver. The module provides a reference frequency to translate a baseband signal to an RF signal on the transmitter side, and from an RF signal to a baseband signal on the receiver side. The PLL module consists of a Voltage-Controlled Oscillator (VCO), frequency divider, Phase/Frequency Detector (PFD), charge pump (CP) and low pass filter (LPF) as shown in Figure 1.

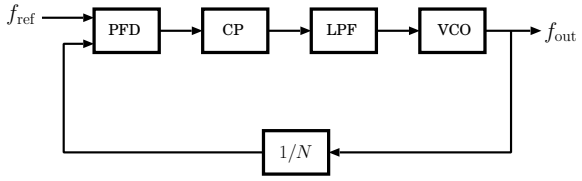

Figure 1. Phase-Locked Loop. Consist of Phase/Frequency Detector (PFD), charge pump (CP), low pass filter (LPF), Voltage Controlled Oscillator (VCO) and frequency divider.

The PFD compares the divided output signal from the PLL output with the reference clock, f_{ref}. The phase error between these signals is converted into a voltage by the charge pump and filtered using a low pass filter. The VCO output frequency is controlled according to the filtered voltage from the filter. The output frequency is then divided by a frequency divider and fed as a second input to the PFD.

Two types of PLL architectures are commonly used in RF transceivers, namely an integer-N PLL and fractional-N PLL. For the integer-N PLL, the output signal frequency is an integer multiple of the reference frequency. While for the fractional-N PLL, the output frequency is a fraction of the reference signal frequency. The choice between these architectures is based on frequency planning needed by the transceiver. The presented model is aimed at the integer-N architecture.

The PLL performance is based on the noise seen at its output. There are two types of noise, random noise and periodic noise. Random noise is also known as phase noise, while periodic noise for integer-N architecture is called reference noise, which represent the reference frequency noise at a specified offset from the carrier frequency.

Reference spur is a serious issue in RF transceivers as it can degrade the signal-to-noise-ratio in data reception and transmission. This spur is dominanated by non-idealities in the PFD and charge pump circuits, namely PFD delay, charge pump current leakage, current mismatch and charge pump switching delay [1]. In the literature, a number of approaches have been devised to eliminate or minimize the non-idealities in these circuits to minimise the reference spurs [2]–[5]. However, the affect of the circuit non-idealities on the reference spur have not been taken into account in their modelling.

In this paper, we present an accurate Simulink-based behavioural model to estimate the reference spur magnitude and settling time that take into account the PFD delay and the charge pump current mismatch, switching delay and effect of rise and fall times characteristic in the charge pump current. The proposed model is based on our initial investigation presented in [1], where we investigated the effect of a few parameters on the reference spur level, where a behavioural VCO in Verilog was used. In contrast, in

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this paper an improved accuracy work is aimed for a better accuracy in reference spur simulation using Simulink behavioural modelling. In addition, non-idealities that included in this proposed model helps to accurately predict PLL settling time.

So an improved charge pump current mismatch model is presented, where the current value is changing according to charge pump output current. In addition, the rise time and fall time effects on the charge pump current response are included in this work. Furthermore, the presented VCO model takes into account the VCO gain non-linearity. The inclusion of all of these effects in the behaviour model resulted in a more accurate reference spur estimation.

In Section II PLL components calibration are presented, where techniques on how necessary parameters are extracted from transistor level simulation are explained. In Section III, PLL Simulink-based model is presented. All PLL components modelling are discussed in this section. The proposed Simulink model is then verified by comparing reference spur magnitude and settling time from the model with results from transistor level simulation are presented in Section IV. Finally, this work is summarised in Section V.

II. PLL Behavioural Model Characterization

Before modelling each component in the PLL, important paramaters have to be extracted from the transistor level simulation for each PLL component. For this purpose, Cadence Sprectre and SpectreRF simulation tools are used. The components were modelled using Jazz Semiconductor 0.18 μm SiGe BiCMOS technology. The method used to extract important parameters from PFD, charge pump and VCO that affects the reference spur and PLL settling time from transistor level are discussed.

A. PFD calibration

PFD delay is an important parameter that was included in behavioural model. The delay for this component was estimated using transient analysis on the PFD circuit with both input signals have the same phase and frequency. As a result, both PFD outputs should have the same signals, with a short HIGH signal will be produced at the output. This delay is required to eliminate dead zone effect. The duration of this HIGH signal present the amount of delay in the PFD circuit.

B. Charge pump calibration

In the charge pump circuit, three parameters were identified to include in the behavioural model, which are current mismatch between the UP and DOWN currents, switching delay and charge pump current rise and fall times. According to simulation, leakage current for the process we are using is very small and does not significantly affect the reference spur level [1]. As a result, the leakage current effect is not included.

The charge pump current can be obtained from DC analysis. For this analysis, both UP and DOWN switches are ON and the output node is connected to a DC voltage with an initial value at zero. The DC voltage value is then swept up to the circuit supply voltage, in 50 mV steps. Then both $I_{\rm up}$ and $I_{\rm dn}$ currents are plotted as shown in Figure 2.

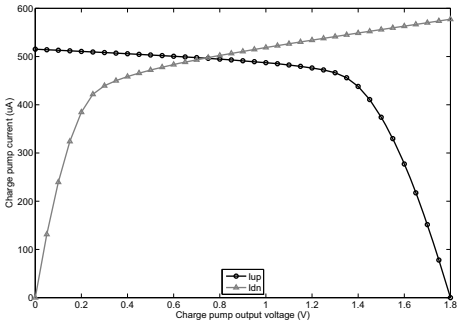

Figure 2. Charge pump mismatch current. $I_{\rm up}$ and $I_{\rm dn}$ value is varying depending on tuning voltage.

The delay in UP switch is due to inverter needed to invert signal from PFD output, as shown in Figure 3. The delay value is estimated from transient analysis simulation to the inverter. Rising and falling characteristic of the charge pump currents were also obtained from transient analysis.

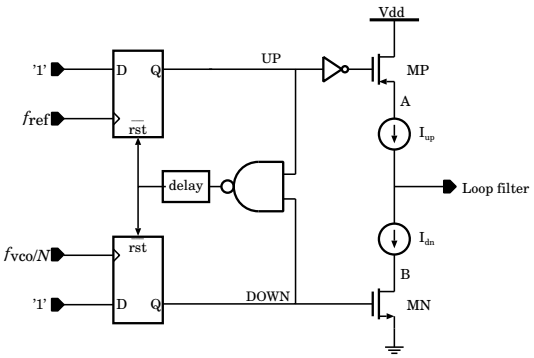

Figure 3. An inverter is required to invert UP signal from PFD.

C. VCO calibration

VCO gain ($K_{\rm vco}$) plays an important role on judging spur level and settling time. The input to the VCO is the filtered tuning voltage $V_{\rm tune}$ by the low pass filter, and the output is a sinusoidal signal with frequency $f_{\rm o}$. The output frequency depends on the tuning voltage and VCO gain, $K_{\rm vco}$. Ideally, the relation between the input tuning voltage and the output frequency is linear, resulting in a constant $K_{\rm vco}$. Unfortunately, in the real VCO implementation, $K_{\rm vco}$ only constant in the middle tuning voltage range, while varied at

both low and high tuning voltages as shown in Figure 4. The inclusion of this non-linearity in the behavioural model is critical to accurately estimate the reference spur of the PLL and predicting its settling time. As such variation in K_{vco} causes a different in spur level estimation at different tuning voltages.

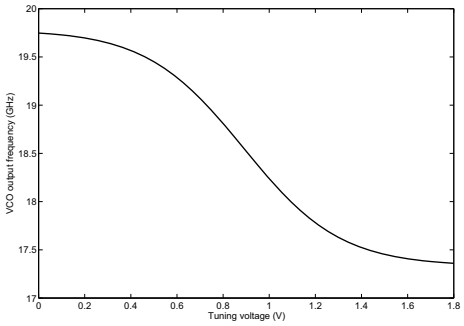

Figure 4. VCO output frequency (f_{o}) vs tuning voltage (V_{tune}). The graph slope is the VCO gain (K_{vco}). The graph is only linear in the middle tuning voltage range, but non-linear at the low and high tuning voltage.

The VCO output frequency versus the input tuning voltage of the oscillator shown in Figure 4 were obtained using Periodic Steady-State (PSS) analysis in Cadence tool. For these simulation, the tuning voltage was changed from 0 to supply voltage (1.8 V) in 50 mV steps.

III. PLL Simulink Model

PLL behavioural modelling in Matlab Simulink is shown in Figure 5. Each component in the PLL was modelled separately, and is discussed in detail in the following subsections.

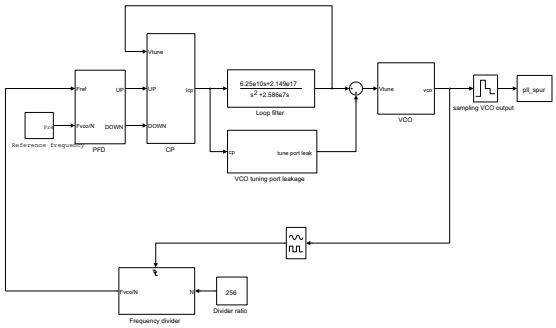

Figure 5. PLL Simulink model

A. PFD Simulink

PFD is constructed by two D-flipflops (DFF) and a NAND logic gate from the Simulink library as shown in Figure 6. A transport delay was used to represent PFD delay.

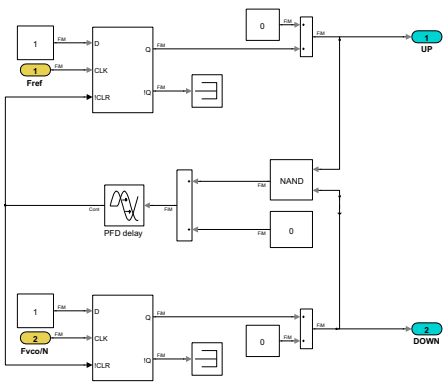

Figure 6. PFD Simulink model. Two D-flipflops and a NAND gate are used to model the PFD. A transport delay was used to represent PFD delay.

B. Charge pump Simulink

Charge pump current can be presented in two methods, namely interpolation and curve fitting. For interpolation, tuning voltage and current value from transistor level simulation were stored in two column array. This table is referred to in the behavioural model simulation whenever a charge pump current value is needed. If an exact value was not available in the given table, an interpolation between two adjacent points was performed. In Simulink, a lookup-table can be used for this method.

For the second method, a curve fitting technique was used to obtain a polynomial equation that relates the tuning voltage and charge pump current [6]. The polynomial order is dependent on the non-linearity between the tuning voltage and the current.

Figure 7 shows a comparison between interpolation and curve fitting methods for I_{up} and I_{dn} currents modelling, respectively. For the lookup table approach, the charge pump current values corresponding to tuning voltage between 0 and 1.8 V, in 50 mV steps were generated. Meanwhile, in the curve fitting method an 8^{th} order polynomial was needed. It should be mentioned that the order of the polynomial is circuit and technology dependent.

Figure 7 shows that interpolation method gives a better accuracy compared to the curve fitting method, with an error of less than 0.15%. Therefore, lookup table was chosen for the proposed Simulink model.

Figure 8 shows the charge pump Simulink behavioural model. The model has three input ports, namely V_{tune}, UP and DOWN. V_{tune} is from charge pump output voltage (which is also tuning voltage if a second order loop filter is used), and UP and DOWN are from PFD output. V_{tune} port is combined with two lookup tables, in order to determine I_{up} and I_{dn} values. UP and DOWN ports are multiplied by the output from lookup tables, so that the I_{up} and I_{dn} are only available when UP and DOWN signals are HIGH,

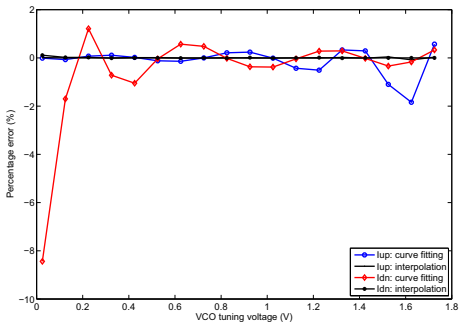

Figure 7. Charge pump current: comparison between interpolation and curve fitting method.

respectively. Then, $I_{\mathrm{up}} - I_{\mathrm{dn}}$ is performed to represent the current component that either enter or exit from loop filter. For the UP port, a transport delay was inserted to represent the switching delay, while the rise and fall times are modelled by rate limiters.

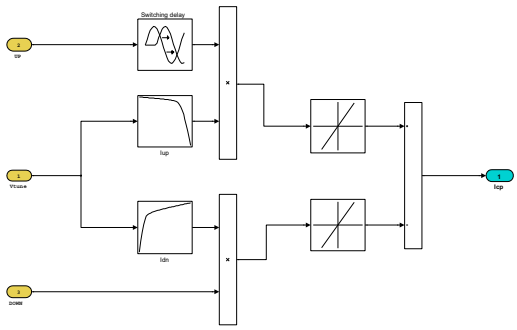

Figure 8. Charge pump Simulink model. Current mismatch, switching delay and rise and fall times characteristics are included in this behavioural model.

This charge pump model helps to accurately simulates PLL settling time, since the charge pump current non-linearity is taking into account. As shown on the Figure 2, when the tuning voltage is close to 0 or supply voltage (1.8 V in this case), I_{up} and I_{dn} value are much different and present a significant effect on the PLL tracking. This demonstrate the ability of the proposed model in modelling such effect that are only seen in transistor level modelling.

C. Loop Filter Simulink

A passive low pass filter was used for this work. The filter is modelled as a transfer function. In this work, a second order filter is used and its transfer function is given by

$$F_2(s) = \frac{R_2C_2s + 1}{R_2C_2C_1s^2 + C_1s + C_2s}, \qquad (1)$$

D. VCO Simulink

Many works have been published on VCO behavioural modelling [7]–[9]. However, the focus on these publications is on modeling the VCO phase noise. In contrast, this presented work focuses on the PLL reference spur modelling. Therefore, phase noise modelling is not included in this VCO.

Similar to the approach we have presented for the charge pump, the VCO behavioural model can also be implemented using interpolation [10] and curve fitting methods [11], [12]. As explained in section III-B, lookup table was used for interpolation techniques, while a polynomial equation is used for curve fitting. The VCO output frequencies as function of tuning voltage from 0 to 1.8 V, in 50 mV steps, was obtained from transistor level simulation, and a lookup table was generated, meanwhile for the curve fitting part, a seventh order polynomial was used. Simulation based on both of two methods are shown in Figure 9. The figure shows that the lookup table approach gives a slightly better accuracy, with percentage error is less than 0.01%.

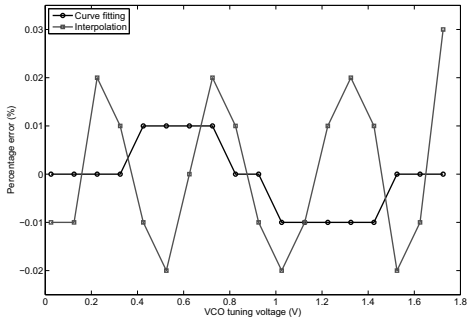

Figure 9. VCO output frequency vs tuning voltage: comparison between interpolation and curve fitting methods

VCO Simulink behavioural model is shown in Figure 10. The input port is named V_{tune}, which is from tuning voltage given by loop filter transfer function. This port is connected to lookup table in order to determine the VCO output frequency. Then, the VCO phase is calculated, where phase is the integral of the frequency modulo 2π. The VCO signal is attained by applying cosine function to the phase.

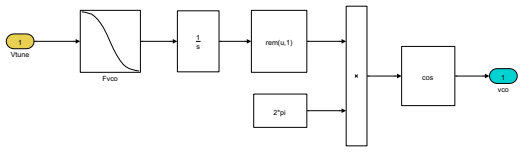

Figure 10. VCO Simulink model.

Similar to the charge pump current versus tuning voltage issue, when the tuning voltage around 0 and supply voltage (1.8 V in this case), VCO gain are much lower than the mid

range voltages. Therefore, the PLL tracking is much slower around these regions. This effect can be simulated using this VCO model, hence an accurate settling time for the PLL can be predicted in short simulation time.

E. Frequency Divider Simulink

Frequency divider can be modelled using a triggered subsystem as shown in Figure 11. Input of the model is dividing ratio, and VCO signal is used as a clock to the subsystem. Output of the model is a square wave signal with frequency given by f_{vco}/N, where f_{vco} is VCO signal frequency and N is dividing ratio.

Each clock cycle, a variable (initial value of zero) is incremented by 1 and the resulting value is divided by dividing ratio. The remainder of the division is compared to the half of dividing ratio. If the value is less than $N/2$, the output signal is at logic HIGH, and vice versa. This comparison is to produce an output signal with 50% duty cycle.

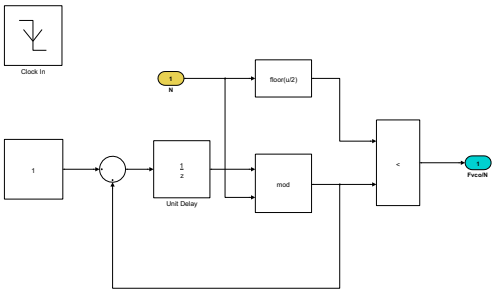

Figure 11. Frequency Divider Simulink model.

IV. Modelling Result

The proposed model is aimed simulating the reference spur and PLL settling time. Comparison between results obtained from the proposed model and transistor level simulation are presented in the following sebsections.

A. Reference spur

Reference spur can be obtained from the proposed Simulink model by plotting Power Spectral Density (PSD) of the VCO output. The first offset reference spur for 6 different VCO output frequencies are obtained. These data are then compared with reference spur magnitude from transistor level simulation as shown in Figure 12. In this figure, the difference in magnitude between the estimated reference spurs obtained from the proposed Simulink model and transistor level simulation is less than 1.5 dBc difference, with a percentage error of less than 3%.

B. PLL settling time

Non-idealities in PFD, charge pump and VCO circuits are included in the proposed Simulink model, resulting in an accurate settling time simulation. Figure 13 shows

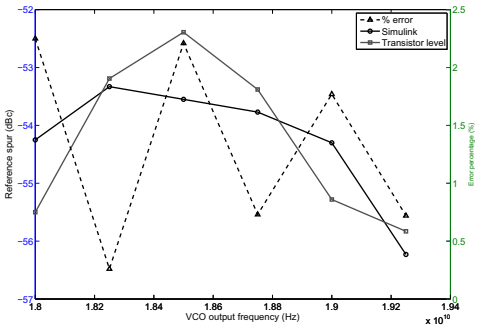

Figure 12. Reference spur magnitude comparison between Simulink model and transistor level simulation.

comparison in PLL settling time between the Simulink model in this work and transistor level simulation. Using this proposed Simulink model, dramatic reduction in simulation time achieved without compromising the performance estimation accuracy.

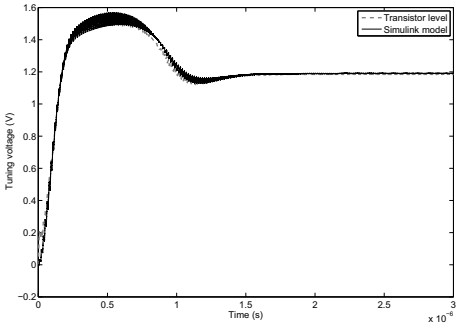

Figure 13. VCO tuning voltage plot. PLL settling time for both, Simulink model and transistor level simulation are about the same.

V. Conclusion

A PLL behavioural modelling in Simulink is presented. Each PLL component was modelled separately and connected together for an overall system simulation. The model includes PFD delay, charge pump current mismatch, switching delay and effect of rise and fall times. In addition, the VCO gain non-linearity was also considered in this model. Results from the presented model were compared with transistor level simulation, and present less than 3% difference in performance estimation when compared with full transistors model simulations. Using this proposed Simulink Model, 97% improvement in simulation period was achieved compared to transistor level simulation in Cadence Sprectre.

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