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# Read operation performance of large selectorless cross-point array with self-rectifying memristive device

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ABSTRACT

Memristive device based passive crossbar arrays hold a great promise for high-density and non-volatile memories. A significant challenge of ultra-high density integration of these crossbars is unwanted sneak-path currents. The most common way of addressing this issue today is an integrated or external selecting device to block unwanted current paths. In this paper, we use a memristive device with intrinsic rectifying behavior to suppress sneak-path currents in the crossbar. We systematically evaluate the read operation performance of large-scale crossbar arrays with regard to read margin and power consumption for different crossbar sizes, nanowire interconnect resistances, ON and OFF resistances, rectification ratios under different read-schemes. Outcomes of this study allow improved understanding of the trade-off between read margin, power consumption and read-schemes. Most importantly, this study provides a guideline for circuit designers to improve the performance of oxide-based resistive memory (RRAM) based cross-point arrays. Overall, self-rectifying behavior of the memristive device efficiently improves the read operation performance of large-scale selectorless cross-point arrays.



## 1. Introduction

The two-terminal memristive device based crossbar array is a promising candidate for future high density resistive memory arrays. Opportunities such as 3D integration, Field Effect Transistor (FET) fabrication compatibility, low power operation, and resistive nature of the memory rather than traditional capacitance-based storage are driving an intense industrial and academic research [1–4]. One of the very important challenges ahead of extremely large and dense scale memory development is the problem of sneak-path currents. This issue can make different device states (e.g. ON and OFF) inextinguishable, giving rise to a significant challenge when reading large-scale memory arrays.

To circumvent sneak-path currents, several approaches have been explored. One approach is to use two back-to-back bipolar memristive elements as shown in Fig. 1(a). This approach seeks to imitate the immense success of CMOS (complementary metal–oxide–semiconductor) technology in which either a pull-up (composed of a p-type transistor) or pull-down (composed of a n-type transistor) device is active at a given time. Such a complimentary configuration desirably limits the short-circuit currents through CMOS circuits. For memristive circuits a similar configuration, known as the complementary resistive switch (CRS) is utilized [5–7]. Such a configuration relies on the polarity difference between these two back-to-back connected memristive elements. Therefore, at a given time, it is guaranteed that at least one device is in high resistance state (HRS). This indicates that the total resistance of this configuration in equilibrium is always at the highest value, hence, limiting sneak-path currents in the crossbar array, see Fig. 2. This however comes at the cost of destructive readout, which means reading a device at any given time requires a write operation to be performed right after each read operation.

A common approach for addressing the issue of sneak-path currents has been the use of a selecting device. The selecting device can possibly be a transistor to form a one-transistor-one-memristive device (1T1M) structure, see Fig. 1(b), or a diode to form a one—selector—one—memristive device structure, see Fig. 1(c) [8]. The 1T1M structure efficiently suppresses sneak-path currents. It is worth mentioning that 1T1M memories are available commercially (Adesto's CBRAM, Panasonic's MCU) and also prototyped in large capacity (Sandisk). However, using a transistor as the selecting device at each crosspoint raises the footprint of each cell, and decreases the three-dimensional stacking capability of cross-

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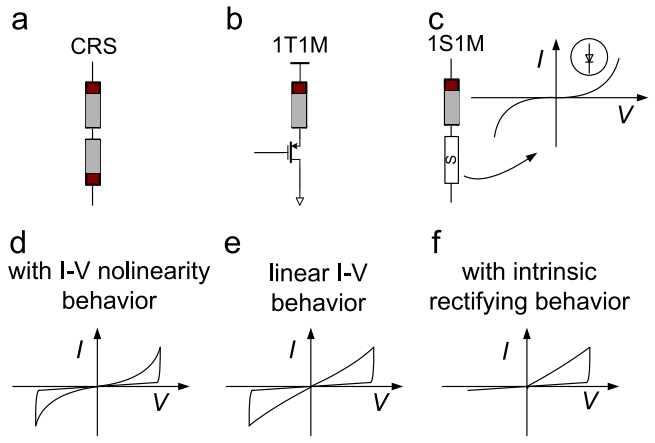
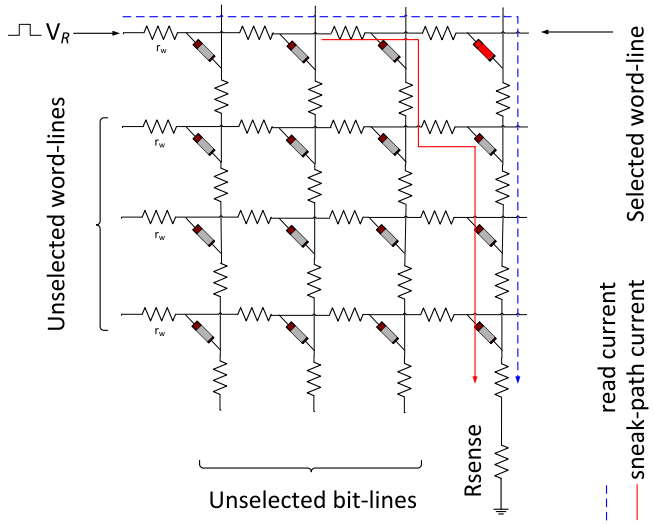



**Fig. 1.** *I–V* characteristic of selector. S represents a two terminal selector device.




| read-scheme | selected word-line | unselected word-lines | unselected bit-lines |
|---|---|---|---|
| V/2 | $V_R$ | $V_R/2$ | $V_R/2$ |
| V/3 | $V_R$ | $V_R/3$ | $2V_R/3$ |
| F-F | $V_R$ | floating | floating |
| G-G | $V_R$ | ground | ground |

**Fig. 2.** Schematic of crossbar memory architecture. Here we define three different read-schemes according to the biased voltage on selected word/bit-line and unselected word/bit-lines.

point arrays. In the case of the 1S1M structure, programming becomes a major challenge. This is mainly due to a large voltage drop on the selector and not on the memristive device. Additionally, the material and structure that allows an efficient memory device characteristics without much suffering from an implementation of integrated selector devices is a major challenge. Recently, special diodes that show a typical *I –V* (current–voltage) characteristic, see Fig. 1(c), were developed to permit sufficient current for programming. This is achieved by applying a voltage above threshold, enabling this special diode to exhibit exponential current behavior as experimentally demonstrated in [8–11]. The performance of this special diode—two terminal selector, however, is required to exceed all specifications for the memristive device including response time, cycling endurance, array yield, and variability, in order not to limit the overall memory (1S1M) performance and reliability. In addition, the selector should support ON-state current density in the order of several MA/cm$^2$ while maintaining OFF-state leakage current as low as possible [12].

To minimize memory cell footprint and fabrication complexity, an alternative is the memristive device crossbar without the selector, which has been studied in [13–15]. To suppress sneak-path currents when no selector is used, one approach is to engineer a large I–*V* nonlinearity, as shown in Fig. 1(d), by integrating an oxide layer to suppress the current even when the memristive device is in LRS (low resistance state) instead of using a memristive device showing a linear *I–V* characteristic, as shown in Fig. 1 (e). Such an approach improves the performance of the memristive device crossbar without a selector [13,14,16]. However, such an approach appears to suffer from life-cycle limitations [1] where the ability to realize a large OFF/ON resistance window diminishes over switching cycles.

The other approach is to exploit a memristive device with intrinsic rectifying behavior as shown in Fig. 1(f). This type of memristive device has been realized [17–22]. A rectification ratio in the order of $10^6$ has been achieved in [17] without a significant reduction in either its switching speed or writing endurance, which makes memristive devices with self-rectifying behavior a possible candidate for circumventing sneak-path currents. As a result, this type of memristive device offers an alternative path for realization of a large ultra-high density crossbar with small footprint and fabrication complexity. However, to the best of our knowledge, detailed read operation performance evaluation of large-scale crossbar arrays based on memristive devices with intrinsic rectifying behavior has not been investigated. Therefore, our motivation in this paper is to systematically study the read operation performance of crossbar arrays with this type of memristive device. In our study, we: (i) provide a Verilog-A behavioral model of a memristive device with intrinsic rectifying behavior based on published measured characteristics of these devices; (ii) evaluate read operation performance of large-scale arrays while considering different nanowire interconnect resistances, HRS/LRS resistances, rectification ratios under different read-schemes at different array sizes; (iii) demonstrate the improved performance using this type of memristive device as an alternative to reduce sneak-path currents in the crossbar; (iv) perform a read operation comparison among memristive devices with intrinsic-rectifying behavior, memristive devices with linear *I–V* characteristic (Fig. 1 (e)), and a 1S1M structure (Fig. 1(c)).

The rest of the paper is organized as follows: in Section 2, we define read margin and different read-schemes when carrying out read operations on crossbar arrays. The memristive device behavioral model is also provided; in Section 3, we study a purely passive crossbar array and analyze the read operation performance, specifically in terms of read margin and power consumption; read operation performance comparison with other types of memristive devices and discussions are presented in Section 4; followed by a conclusion in Section 5.

## 2. Crossbar array and device model

### 2.1. Crossbar array

A crossbar array shown in Fig. 2 comprises of two layers of parallel electrodes that are crossed perpendicularly, which act as word-lines and bit-lines respectively. At each crosspoint a storage element is formed, which can be programmed to the LRS or HRS representing either a logic '1' or '0' when appropriate voltages are applied to word-lines and bit-lines. Unfortunately, as stated in Section 1, this architecture suffers severely from sneak-path currents, hence appropriate approaches are necessary to suppress

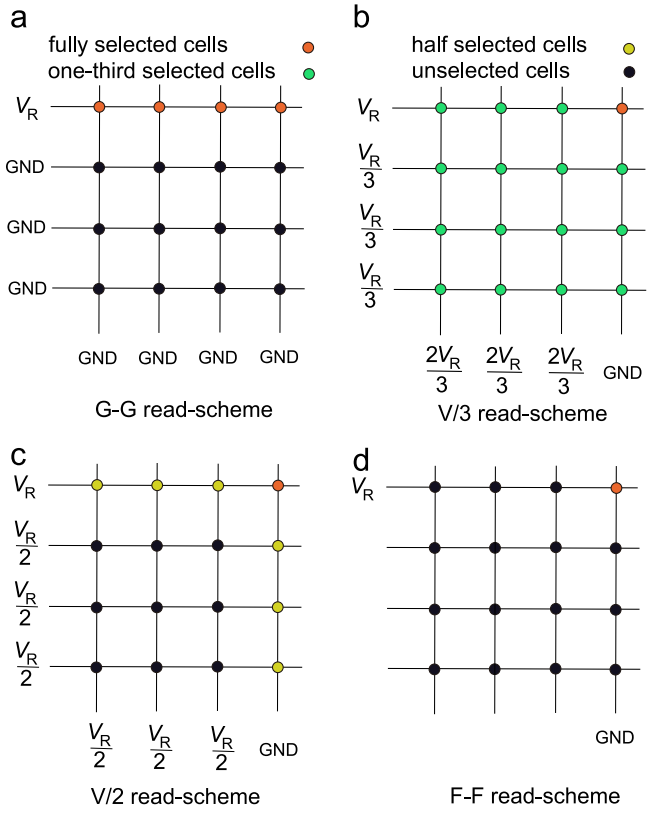



**Fig. 3.** Illustrations of read-schemes.

them. Because sneak-path currents aggravate read/write operation performance of the crossbar array and hence, limit the maximum size of a crossbar.

The source of sneak-path currents is shown in Fig. 2. As can be seen, besides the desired *read current*, there are many current paths—one such current path is shown—flowing into the selected bit-line blurring the desired *read current*. As discussed earlier, an alternative to suppressing sneak-path currents and, consequently, improving read/write operation performance is by employing a memristive device with intrinsic rectifying behavior.

In the following simulations a sense resistor is used to connect to the selected bit-line serially to simplify the read operation with large-scale crossbars. Then the voltage drop across the sense resistor is measured to sense the state of the target-cell (the cell that is being measured). To obtain the best read margin, the sense resistor value, $R_{\text{sense}}$, is selected based on [23,12]:

$$R_{\text{sense}} = \sqrt{R_{\text{ON}} R_{\text{OFF}}}. \tag{1}$$

The read margin, RM, is defined as [12]:

$$\text{RM} = \frac{V_{\text{out}}(\text{LRS}) - V_{\text{out}}(\text{HRS})}{V_{\text{R}}} \tag{2}$$

where $V_{\text{R}}$ is the read voltage applied to the selected word-line as shown in Fig. 2. The $V_{\text{out}}$(LRS) and $V_{\text{out}}$(HRS) are voltages measured in $R_{\text{sense}}$ resistor when the target-cell is in the LRS and HRS, respectively. In other words, such a voltage sensing scheme is being considered in this paper.

In the literature, there are a number of read-schemes for crossbars that include V/2, V/3, F–F (Floating–Floating) and G–G (Ground–Ground), where $V$ is the rail-to-rail (maximum) potential difference. The voltage bias requirements for these read-schemes are shown in Fig. 2 and more details are shown in Fig. 3.

Due to the influence of sneak-path currents, the output voltage swing is dependent on both the stored data and the position of the target-cell to be read within the array. Additionally, taking the interconnect resistance into account, the read margin will deteriorate further if the target-cell is located in the furthest corner from the word/bit-line voltage sources. In the case of Fig. 2, the target-cell is the top right corner cell. In this paper, the read operation performance is performed when the target-cell is under this worst-case position.

In the G–G read-scheme, the voltage potential applied to memristive devices that locate in the word-line is almost $V_R$—these memristive device cells are called *fully selected cells* as shown in Fig. 3(a), whereas voltage across other memristive devices is nearly 0 V. Therefore, most sneak-path currents originate from these fully selected cells. In the V/3 read-scheme, memristive devices (except the selected top-right corner one) situated in the whole array have a voltage potential of $\frac{V_R}{3}$—these memristive device cells are called *one-third selected cells* as shown in Fig. 3(b), which provide the source of sneak-path currents. In the V/2 read-scheme, memristive devices (except the target-cell in the top-right corner) in the selected word-line and selected bit-line have a voltage potential of $\frac{V_R}{2}$—these memristive device cells are called *half selected cells* as shown in Fig. 3(c). Sneak-path currents result from these half selected cells [24]. In the F–F read-scheme, the sneak current paths are due to unselected cells as shown in Fig. 3 (d). In [12,24], it has been demonstrated that the G–G read-scheme has the worst power consumption performance but the best read margin, while the F–F read-scheme has the best power consumption performance but the worst read margin. In other words, there is a trade-off between power consumption and read margin.

### 2.2. Memristive device model with intrinsic rectifying behavior

The memristive device model with intrinsic rectifying behavior is investigated in this subsection. We use a simplified mathematical model for this memristive device to match its characteristics empirically reported in [17–19]. Subsequently we provide a model implemented in Verilog-A for the following simulations.

A memristive device has a state variable $\omega \subset [0,1]$ corresponding to the value of its memristance $R_m$, which is a function defined as

$$R_m = \begin{cases} R_{\text{OFF}}(R_{\text{ON}}/R_{\text{OFF}})^{\omega}, & (v \geq 0) \\ R_{\text{OFF}}, & (v < 0) \end{cases} \tag{3}$$

where $v$ is the applied voltage across it. According to Eq. (3), $R_m = R_{\text{OFF}}$ when $\omega = 0$, while $R_m$ is in the $R_{\text{ON}}$ state if $\omega = 1$.

The memristive device is observed having a well-defined threshold voltage. On the one hand, if the absolute biased voltage applied to the memristive device is smaller than the threshold voltage, the state variable stays unchanged or changes minimally. On the other hand, once the bias voltage is larger than the threshold voltage, the state variable changes abruptly. Here we use symmetric threshold voltages, which can be different in practical memristive device implementations. The dynamic switching behavior of the memristive device is defined as

$$\frac{dw}{dt} = \begin{cases} \alpha(v - V_{\text{TH}}), & (v \geq V_{\text{TH}}) \\ \alpha(v + V_{\text{TH}}), & (v \leq -V_{\text{TH}}) \\ \beta v, & \text{otherwise}, \end{cases} \tag{4}$$

where $V_{\text{TH}}$ is the threshold voltage. The $\alpha$ and $\beta$ coefficients are programming rates. Here, we set $\beta = 0$ assuming that the smaller voltage does not alter the state variable, and hence, does not perturb the memristance during read operation [25].

The developed behavioral model created in Verilog-A language is adapted from [25] and given in the Appendix. Simulated $I$–$V$ curve in Fig. 4 shows the intrinsic rectifying behavior.

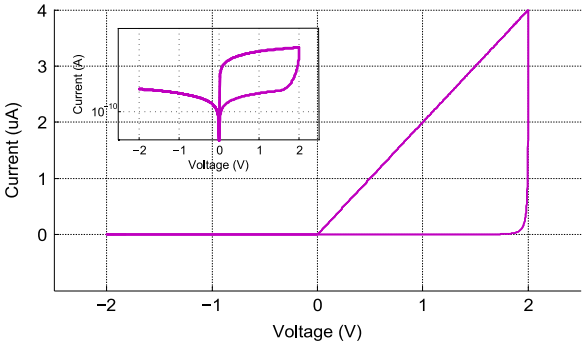



**Fig. 4.** Simulated *I–V* characteristic of the memristive device behavioral model with intrinsic rectifying behavior. It is obtained by using a sinusoid signal with 10 MHz frequency and 2.0 V (peak-to-peak voltage) amplitude. The inset figure illustrates the same *I–V* characteristic while the *y*-axis is on a logarithmic scale.

**Table 1**
List of parameters used in simulations, and the default values of these parameters.

| Description | Value |
|---|---|
| High resistance state $R_{OFF}$ | $5 \times 10^8\ \Omega$ |
| Low resistance state $R_{ON}$ | $5 \times 10^5\ \Omega$ |
| Sense resistor $R_{sense}$ | $1.58 \times 10^7\ \Omega$ |
| Interconnect resistance $r_{wire}$ | $5\ \Omega$ |
| Threshold voltage $V_{TH}$ | 1.5 V |
| Read voltage $V_R$ | 1.0 V |
| Ratio of $R_{OFF}/R_{ON}$ | $1 \times 10^3$ |
| Programming rates $\alpha$ | $2.5 \times 10^8\ (\mathrm{V\,s})^{-1}$ |
| Programming rates $\beta$ | $0\ (\mathrm{V\,s})^{-1}$ |

## 3. Results and analyses

In this section, the aforementioned memristive device model is integrated into a crossbar array to study the read margin and power consumption under different crossbar sizes, read-schemes, wire interconnect resistances, rectification ratios and LRS resistances when the rectification ratio is constant.

Simulations are carried out using Cadence tools, then extracted data are post-processed in MATLAB. In these simulations the wire interconnect resistance is also taken into consideration to provide a more realistic assessment of the crossbar array performance. The default parameters used in the following simulations are listed in Table 1. Note that this paper focuses on the reading rather than the writing operation performance. For the following simulations it is assumed that the device resistance does not change when a reading voltage $V_R = 1$ V is applied to the word/bit-lines since the threshold voltage used is 1.5 V.

The idea developed in this paper utilizes static device states and is minimally affected[1] by device dynamics. Therefore a behavioral model rather than a compact model like [26] is used. The behavioral model can meet the requirement to obtain reasonable results when conducting the simulations. In addition, a simple behavioral model speeds up the simulation in Cadence, especially when the crossbar size increases and the large number of wire interconnect segments are taken into consideration. In this paper, the maximum size of the crossbar considered for our analysis is $128 \times 128$. To evaluate a larger crossbar requires future work that may be carried out by using machine learning algorithms to significantly improve the simulation speed [27].

[1] Device behavior under a small applied bias is considered in this paper to be insignificant because (1) the voltage used for a 'read' operation is much smaller than the switching threshold, (2) the device current–voltage curve is very nonlinear.

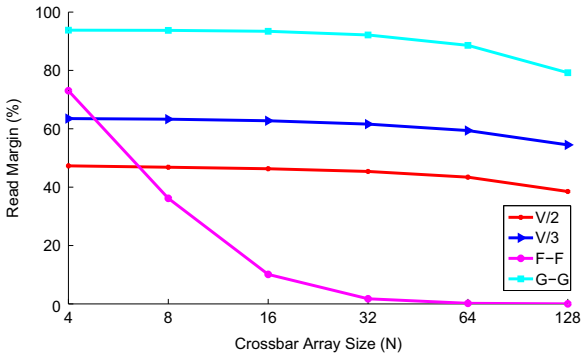



**Fig. 5.** Read margin as a function of the crossbar size under different read-schemes, where *N* is the number of columns or rows of a crossbar. Here the number of columns equals the number of rows.

### 3.1. Read-scheme and crossbar size

The read margin and power consumption at different crossbar sizes under different read-schemes are studied in this section. The simulated size of the crossbar is from $4 \times 4$ up to $128 \times 128$. In addition, all aforementioned read-schemes—V/2, V/3, F–F, and G–G—are investigated respectively.

The read operation performance results for the read margin and power consumption as a function of the array size are shown in Figs. 5 and 6, respectively. As for the read margin, the G–G read-scheme has the best performance, while the F–F read-scheme has the worst performance when the array size increases to $8 \times 8$.

In the G–G read-scheme, sneak-path currents from the *half selected cells* in the selected word-line are drained to unselected bit-lines. As a consequence, only relatively small sneak-path currents flow into the selected bit-line, which contributes to the best read margin performance. Conversely, in the F–F read-scheme all of the sneak-path currents flow into the selected bit-line. As a consequence, increasing the crossbar size leads to an exponential increase in the number of sneak current paths within the array, resulting in the worst read margin for the F–F read-scheme. Even though the memristive device already shows an intrinsic rectifying behavior that was specifically introduced to reduce the sneak-path currents. In terms of the other three read-schemes of V/3, V/2, G–G, there is a slight decrease in the read margin with increased array sizes.

Power consumption is shown in Fig. 6. The power consumed when the target memristive device stays either in the HRS or LRS is measured separately. It can be seen that the power consumption difference is very small (almost the same) when the selected memristive device is in the HRS and LRS respectively, except for the F–F read-scheme when the crossbar size is small (smaller than $8 \times 8$ in our study). This can be explained by the fact that unselected cells consume most of the power due to sneak current paths. This can also be verified by the larger power consumption difference under the F–F read-scheme when the crossbar size is small. In this case, most power is consumed by the target-cell as the sneak-path currents can be efficiently reduced, consequently, the large power consumption difference in the HRS and LRS can be clearly observed. In overall, the F–F read-scheme consumes minimum power, whereas the G–G read-scheme consumes the largest power. Note that the power consumption under the F–F read-scheme is only a very small fraction of the other three read-schemes, especially when the crossbar array size becomes larger. The power consumption under the F–F read-scheme almost stays

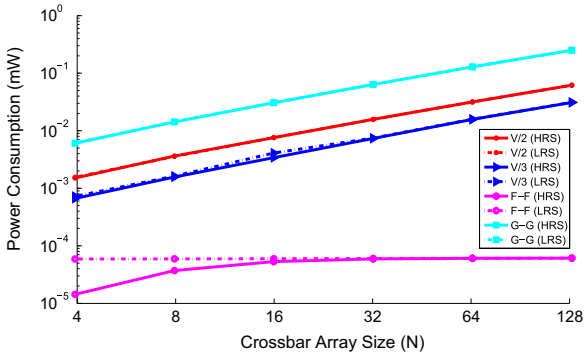



**Fig. 6.** Power consumption as a function of crossbar size under different read schemes. Here, *N* represents the number of columns or rows of a crossbar.

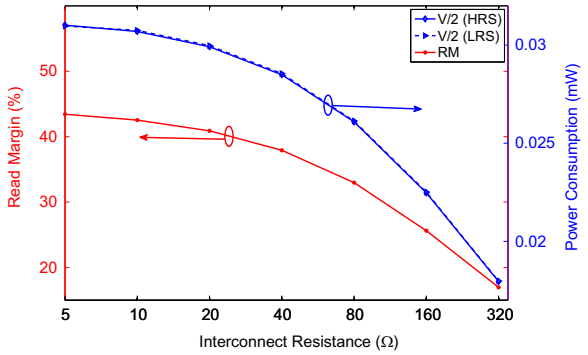



**Fig. 7.** Read margin and power consumption as a function of the interconnect resistance. The crossbar size is fixed at $64 \times 64$. The V/2 read-scheme is used.

unchanged, while the power consumption of the other three read-schemes increases.

### 3.2. Interconnect resistance

The influence of interconnect resistance on read operation performance is shown in Fig. 7. It indicates that increasing interconnect resistance aggravates the read margin. However, increasing interconnect resistance does reduce the overall power consumption. The read margin drops by 50% as the interconnect resistance rises from 5 Ω to 320 Ω. In order to achieve a high read margin performance, the interconnect resistance should be as small as possible despite the fact that a larger interconnect resistance can result in a slight increase in the overall power consumption.

Sources of read margin deterioration caused by interconnect resistance are: (i) voltage drops across the selected word/bit-lines; (ii) the unbalanced increasing and decreasing voltage potential on unselected word/bit-lines, resulting in increasing the number of leakage current paths flowing into the selected bit-line.

### 3.3. Different memristive device parameters

#### 3.3.1. Resistance of ON/OFF

Fig. 8 shows the influence of the ON/OFF resistance on read operations. To ensure the ratio of HRS/LRS is kept constant during the simulation, the $R_{OFF}$ value is changed accordingly. Consequently, the sensing resistor, $R_{sense}$ also needs to be changed according to Eq. (1).

The read margin improves if the $R_{ON}$ resistance increases. The overall power consumption also improves as the $R_{ON}$ resistance increases. It is observed that increasing $R_{ON}$ resistance improves performance of both of the read margin and the power

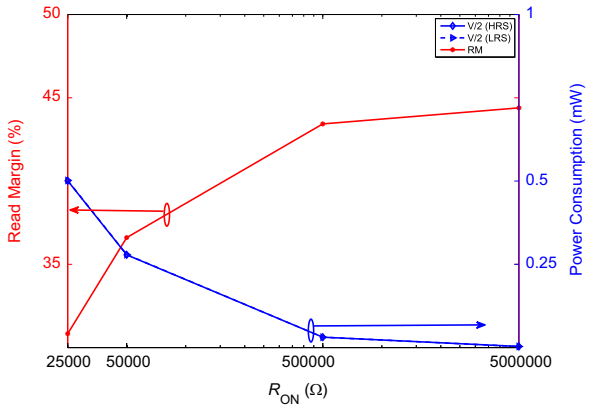



**Fig. 8.** Read margin and power consumption as a function of the $R_{ON}$ resistance. The crossbar size is fixed at $64 \times 64$. Rectification ratio is kept at $10^3$. The V/2 read-scheme is used.

consumption performance. However, it should be noted that there is still a trade-off among read margin, power consumption and readout speed requirements.

#### 3.3.2. Rectification ratio dependence

In this part, the $R_{ON}$ resistance remains unchanged, while the rectification ratio[2] changes to different values. The read margin and power consumption as a function of rectification ratios are shown in Figs. 9 and 10, respectively.

It can be seen from Fig. 9 that read margin improves as the rectification ratio increases, especially for the F–F read-scheme. The fact is that the sneak-path currents can be suppressed significantly as the rectification ratio increases. Therefore, read margin performance benefits from the self-rectifying behavior.

In the F–F read-scheme, all of the sneak-path currents flow into the selected bit-line. To form such a sneak path in the F–F read-scheme, the sneak path current must pass through at least one unselected reverse biased memristive device, which forces this memristive device to show rectifying behavior—a high resistance. Therefore, the sneak path currents will be significantly suppressed —although total resistance in the crossbar will increase greatly—as the rectification ratio increases and, consequently, resulting in an exponential reduction in power consumption. As for G–G, V/2, and V/3 read-schemes, most of the sneak-path currents pass through the unselected memristive devices that operate in the forward region and directly flow into unselected bit-lines. In other words, very limited sneak-path currents pass through unselected memristive devices as reverse polarity currents then flow into the selected bit-line. Total resistance change in crossbar array as a function of rectification ratio is negligible. As a consequence, the power consumption in G–G, V/2 and V/3 read-schemes is not affected. In addition, the power consumption difference in the HRS and LRS states becomes larger since the sneak-path currents are significantly suppressed. Hence, less power is consumed by unselected cells and power consumption of the selected cell will be dominant as the rectification ratio increases.

## 4. Comparison and discussion

In this section, we firstly compare read operation performance of a self-rectifying memristive device with linear memristive device, see Fig. 1(e). Secondly, we compare read operation performance of a self-rectifying memristive device with the 1S1M

[2] It is also the ratio of HRS/LRS according to the mathematical model.

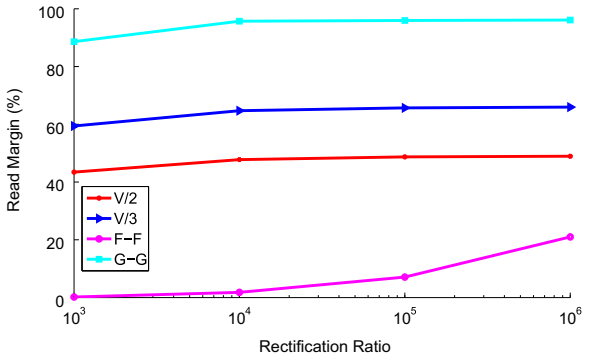



**Fig. 9.** Read margin as a function of different rectification ratios under different read-schemes. The crossbar size is fixed at $64 \times 64$. $R_{ON}$ is fixed at $5 \times 10^5$ Ω.

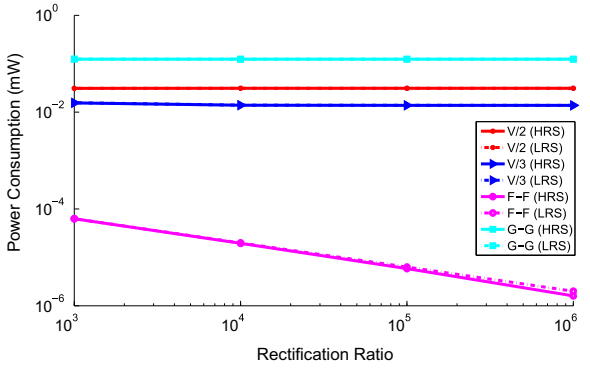



**Fig. 10.** Power consumption as a function of rectification ratios under different read-schemes. The crossbar size is fixed at $64 \times 64$. $R_{ON}$ is fixed at $5 \times 10^5$ Ω.

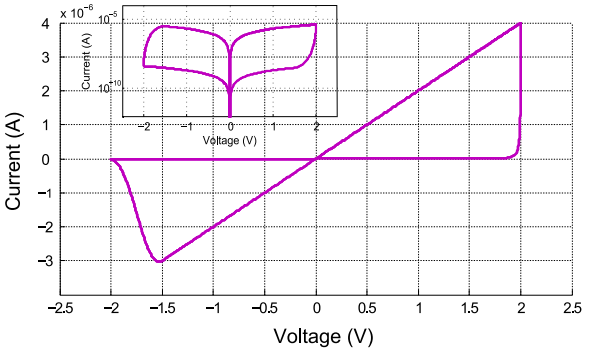



**Fig. 11.** Simulated *I–V* curve of the behavioral model without intrinsic rectifying characteristic. Simulation settings are the same as those used in Fig. 4. The inset figure shows the same *I–V* curve but the *y*-axis is on a logarithmic scale.

structure, see Fig. 1(c). Intuitively one might expect that increasing nonlinearity of the selector is always going to improve the read operation performance of the 1S1M structure similar to the observation in Figs. 9 and 10, which show that the read operation performance improves as the rectification ratio increases. However, the following investigations demonstrate this is not always the case.

### 4.1. Comparison with the linear memristive device

The *I–V* characteristic of the linear memristive device model (with linear resistance behavior in the LRS) is shown in Fig. 11, which has same parameter settings used in Fig. 4, except the rectifying behavior.

Based on the results as shown in Figs. 12 and 13, it can be observed that both of the read margin and power consumption

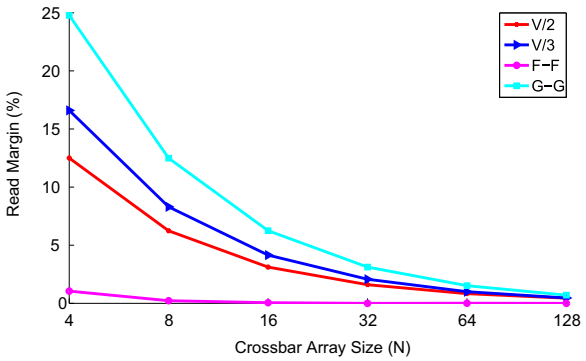



**Fig. 12.** Read margin as a function of crossbar size under different read-schemes, where *N* is the number of columns or rows of a crossbar.

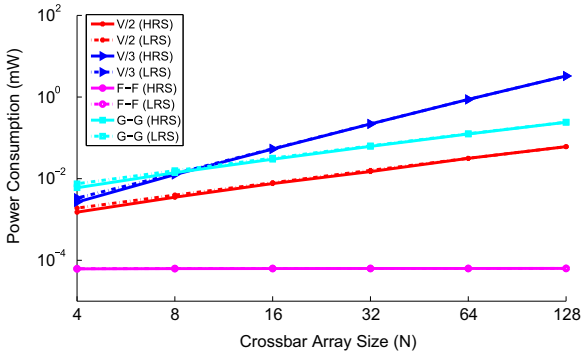



**Fig. 13.** Power consumption as a function of crossbar size under different read-schemes, where *N* is the number of columns/rows of a crossbar.

performance significantly deteriorate in comparison with the results in Figs. 5 and 6. As for the read margin, the G–G read-scheme still has the best performance and the F–F illustrates the worst performance and that is similar to results obtained in Section 3.1. Without the self-rectifying behavior, the sneak-path currents cannot be effectively suppressed, resulting in severely decreased read margin. Especially for the F–F read-scheme, the read margin is too small for practical applications, even when the array size is very small (for example, $4 \times 4$). In contrast to the read margin performance using the memristive device with self-rectifying behavior where no obvious deterioration in read margin is seen as the crossbar size scales to $128 \times 128$, the read margin for linear memristive device suffers from a significant degradation as the crossbar size increases.

The V/3 read-scheme has a worse power consumption than the G–G read-scheme when the crossbar sizes is larger than $8 \times 8$, which does not follow the results presented in Section 3.1, where the G–G read-scheme always showed the largest power consumption. In addition, the other difference between the results in Fig. 6 and the results in Fig. 13 is that the power consumption increases faster as the size of crossbar increases when using a linear memristive device. Further, since the sneak-path current is always dominant, Fig. 13 does not show a clear power consumption difference between HRS and LRS that exists in Fig. 6 when the crossbar size is small.

### 4.2. Comparison with the 1S1M structure

In this subsection, we compare the read operation performance with 1S1M structure. As for 1S1M structure, the memory cell is made up of a selector and a memristive device serially connected. The selector has the characteristic of allowing both polarities to conduct beyond a threshold. The mathematical model is defined

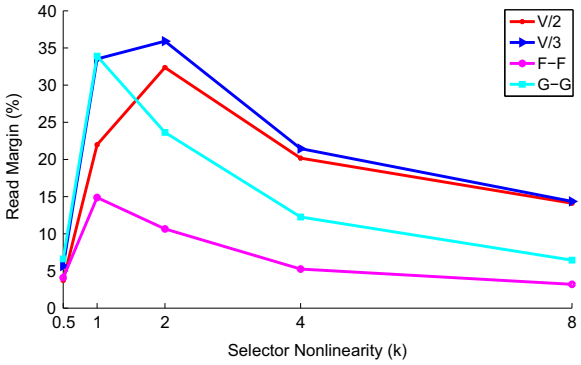



**Fig. 14.** Read margin as a function of nonlinearity ($k$) of the selector. The size of crossbar array is fixed at $64 \times 64$.

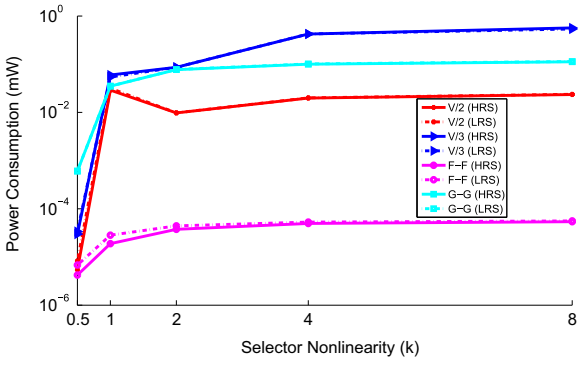



**Fig. 15.** Power consumption as a function of nonlinearity ($k$) of the selector. The size of crossbar array is fixed at $64 \times 64$.

as [12]:

$$I_{sel} = \gamma \sinh(\alpha V), \quad \text{where } \alpha = kp, \tag{5}$$

the parameter $\gamma$ is a conductance parameter with the value of 2 pA and the parameter $k$ determines the nonlinearity of the selector. Here, the coefficient $p = 18.4$, a constant value, is set to the same value presented in [12]. To model the 1S1M structure, one selector is serially connected with one resistor acting as a memory cell. Here, the resistance of the resistor are set to be $5 \times 10^5\ \Omega$ and $5 \times 10^8\ \Omega$ to stands for $R_{ON}$ and $R_{OFF}$, respectively. The rest of the parameters are the same as those given in Table 1.

During simulations, the value of $\gamma$ is kept fixed, while $k$ was changed to determine the nonlinearity of the selector, which influences the read operation performance. Results are shown in Figs. 14 and 15. In contrast to the results that increasing the rectification ratio always result in an increased read margin as discussed in Section 3.3.2, it can be seen that there exists an optimum nonlinearity for the selector to achieve the best read margin. So using the 1S1M structure, there is an issue that the nonlinearity must be cautiously considered along with the forward current $I_{ON}$ to acquire the maximum read margin. In other words, the forward current $I_{ON}$ must be kept as small as possible, then increasing the nonlinearity of the selector will help increase the read margin eventually [11].

In addition, the power consumption always increases for the 1S1M structure when $k$ increases, which is also different from the power consumption results reported in Section 3.3.2 where we show that power consumption does not obviously increase when increasing the rectification ratio. Moreover, the power consumption under F–F read-scheme *does not* benefit from the rise of rectification ratio that is in contrast to the results shown in Fig. 10.

## 5. Conclusion

In this paper, the read operations of the crossbar array are studied with the proposed memristive behavioral model. We verify that rectification behavior significantly improves the read operation performance. As a circuit design guideline, it can be concluded that the G–G read-scheme shows the best read margin and the F–F demonstrates the worst read margin as the array size increases. The F–F read-scheme has the best power performance in comparison with the power consumed by the other three read-schemes (V/2, V/3 and G–G read-schemes). Moreover, studies on interconnect resistance suggest that the wire resistance should be kept as small as possible to achieve improved read margin. Furthermore, the read operation dependence on memristive device parameters is investigated. The numerical results indicate larger HRS/LRS resistance and higher rectification ratio are desirable. Finally, we demonstrate the advantages of pursuing this intrinsic rectifying behavior within memristive devices based on two comparisons in Section 4. From the comparison in Section 4.1, as expected, the rectification does suppress sneak-path currents in crossbar memory leading to an improved figure-of-merit for the read operation performance. In terms of the comparison in Section 4.2, we show that increasing the nonlinearity of selector in 1S1M structure does not always lead to better read operation performance. In contrast, it can deteriorate the read margin and power consumption performance without careful selection of the selector parameters. So the memristive device with intrinsic rectifying behavior is a promising alternative that can act as a crosspoint cell in selectorless crossbar array memory.

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## Appendix A

```
`include "disciplines.vams"
`include "constants.h"
`include "constants.vams"
//behavioral model of memristive device
   with self-rectifying behavior.
module memristor (p,n);
    inout p;//positive terminal
    inout n;//negative terminal
    electrical p, n;

//parameter defination and default
   values. Detailed descriptions and
   unit of them can be found in Table
   1.
    parameter real roff=5E8;
    parameter real ron = 5E5;
    parameter real winit = 1;
    parameter real Vth=1.5;
    parameter real alpha=2.5E8;
    parameter real beta=0;

    real dwdt;
    real w_normal_last;
    real w_normal;
    real R;
    real first_iteration;
    real stop;
    ////        main        ////
    analog begin
        if (first_iteration==0) begin
        w_normal_last=winit;
        //if this is the first iteration
           , start with winit;
        end

        if (V(p,n) >= Vth) begin
            dwdt=alpha*(V(p,n)-Vth);
        end else if (V(p,n) <= -Vth)
           begin
            dwdt=alpha*(V(p,n)+Vth);
        end else begin
            dwdt=beta*V(p,n);
        end

        w_normal=idt(dwdt,w_normal_last,
           stop);
        if ((w_normal>=1)&&(V(p,n)>0))
           begin
            w_normal_last=1;
            stop=1;
        end
        else if ((w_normal<=0)&&(V(p,n)
           <0)) begin
            w_normal_last=0;
            stop=1;

            end
            else if (stop!=0) begin
                w_normal_last=w_normal;
                stop=0;
            end

            if((V(p,n)< 0)) begin
                R=roff;
            end
            else if (V(p,n)>= 0) begin
                R=roff*pow(ron/roff,w_normal
                   );
            end

            I(p,n) <+ V(p,n)/R;
            first_iteration=1;
            end
    endmodule
```

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