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Integrated Memristor-MOS (M^2) Sensor for Basic Pattern Matching Applications

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This paper introduces an integrated sensor circuit based on an analog Memristor-MOS (M^2) pattern matching building block that calculates the similarity/dissimilarity between two analog values. A new approach for a pulse-width modulation pixel image sensor compatible with the memristive-MOS matching structure is introduced allowing direct comparison between incoming and stored images. The pulsed-width encoded information from the pixels is forwarded to a matching circuitry that provides an anti-Gaussian-like comparison between the states of memristors. The non-volatile and multi-state memory characteristics of memristor, together with the related ability to be programmed at any one of the intermediate states between logic '1' and logic '0' brings us closer to the implementation of bio-machines that can eventually emulate human-like sensory functions.

Keywords: Memristor, Pattern Matching, Non-Volatile Memory, TiO_2, Thin Films.

RESEARCH ARTICLE

1. INTRODUCTION

The increasing demand for ultra-dense chips, high-speed communication, and high storage creates a need for 3-D integrated architectures providing an option for higher levels of integration. High power consumption, and cooling techniques, addressing modes, coding and decoding data structures, and transferring data from a non-volatile type of memory to RAM (Random Access memory) type memories at high speed create numerous complexities for future integrated systems. Numerous approaches have been proposed for pattern matching, recognition, and classification that are based on VLSI implementation as a common tool in many applications, including object recognition, stereo matching, and object tracking.

However, despite advances in technology, hardware implementation of an integrated sensory system remain as a barrier. The recent emergence of the memristor, the 4th fundamental element,[1,2] creates an opportunity for increased integration density beyond the present limits of CMOS scaling.

In this paper a basic block for a sensor with application in pattern recognition systems is proposed that combines the inherent memory behavior of memristors[3] and the computational functionality of MOS transistor as part of a smart sensory system. In the pattern recognition, the goal is to identify a mapping function, $h{:}\alpha \rightarrow \beta$, that maps inputs $\alpha \in A$ to templates $\beta \in B$ or generally to a number of categories C_j, where $j \in N$.

The α and β vectors can be written in terms of normalized state variables w_i and w_t for the input memristor M_i and template memristor M_t, respectively, as shown in Figure 1(a), where $\alpha = \{w_i^{(1)}, w_i^{(2)}, \ldots, w_i^{(n^2)}\}$ and $\beta = \{w_t^{(1)(y)}, w_t^{(2)(y)}, \ldots, w_t^{(n^2)(y)}\}$.

The $w_i^{(j)}$ variable represents the j-th instance of the input vector, α, which corresponds to an input pixel value, and $w_t^{(x)(y)}$ variable demonstrates the x-th instance of the y-th template vector, where $x = 1, 2, \ldots, n^2$, $y = 1, 2, \ldots, m$, n^2 is the size of each vector, and m is the number of templates.

The proposed sensory part of the imaging circuit combines both the image sensor and pattern matching circuitry as a single entity. The computational process is performed in three steps: (1) Light-to-time conversion phase by the image sensor. (2) Programming phase by memristor, and (3) Computational phase or matching process by M^2 block. The imager has been implemented and fabricated using 0.13 μm Samsung Electronics standard CMOS process developed specifically for CMOS mixed-signal circuits. With reference to Figure 1, the imager raw data is fed to analog matching circuitry whereby the light output is

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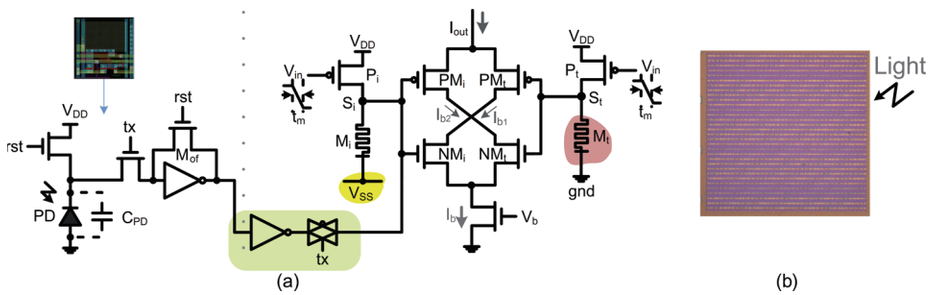

Fig. 1. Block diagram of the proposed integrated memristor-MOS (M^2) sensory circuit for pattern matching and recognition. (a) Single cell circuit and the sensor layout. (b) Micrograph of the pixel array.

encoded into a variable pulse widths determined by the level of light intensities. This signal changes the internal state of memristor, M_i, and hence its conductance. The stored template state is also encoded in memrisor M_t.

Comparison between the two memristors states defines the distance between the two image vectors, α and β. Memristor-based device SPICE simulations (Cadence Spectre) were used to verify the functionality.[2–4]

In this paper, a memristive device is a bipolar Resistive Random Access Memory (ReRAM) that its underlying physics of switching and/or gradual change of resistance can be described based on either Valance Change Memory (VCM) or Electrochemical Metalization (ECM)systems. Each cell contains one transistor and one ReRAM device (1T1R).

2. INTEGRATED MEMRISTOR-MOS SENSORY CIRCUIT

The basic CMOS image sensor pixel, memristor-MOS analog comparator schematics, and the pixel layout are illustrated in Figure 1(a). The micrograph of the fabricated 64×64 CMOS image sensor chip is shown in Figure 1(b).[5] Initially, the incident light is converted to time that appears

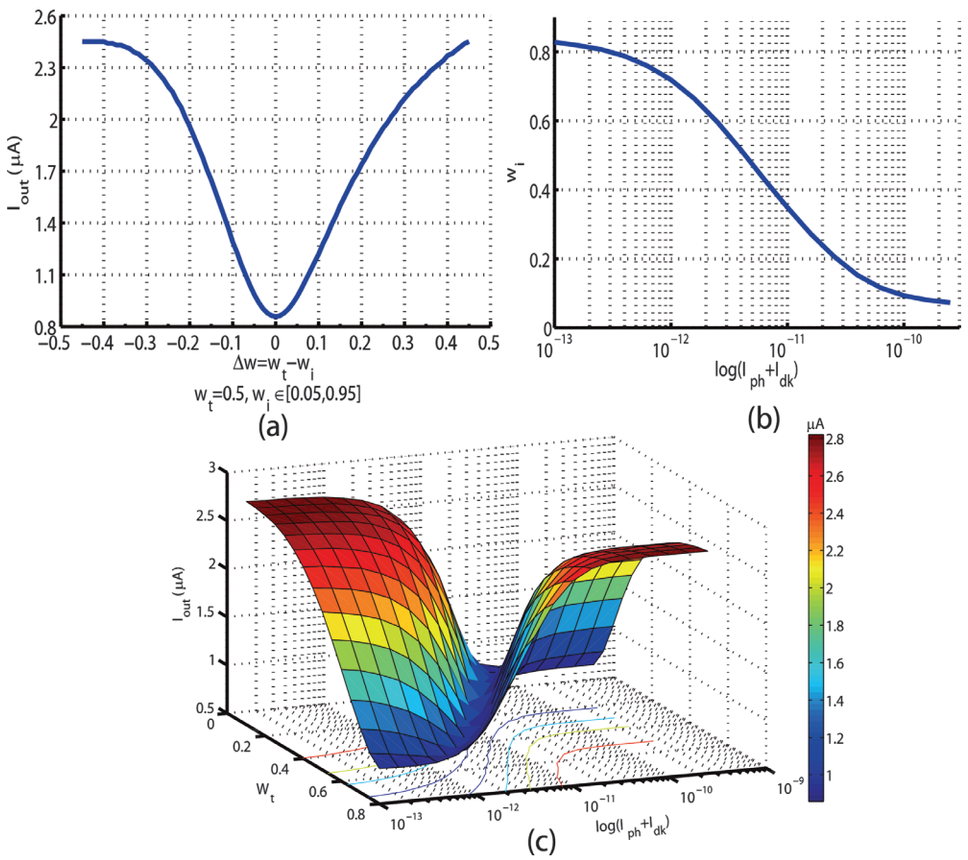

Fig. 2. Simulated circuit response as a function of light intensity. Explanation of subfigures is provided within the text.

at the output. The offset voltage introduced by the inclusion of an inverter instead of the more complex comparator is removed by inclusion of nMOS transistor, M_{of}, while the pixel is in its reset phase. The 't_x' signal is enabled and remains high for the entire integration period, T_{int}. In our simulations $T_{\text{int}} \approx 2$ ms.

The flushed-based reset approach reduces the reset noise and eliminates the possibility of image lag, which is a serious problem in image recognition systems.

Figure 2(a) demonstrates the behavior of the expected mapping function, $h(\cdot)$, that corresponds to current I_{out} which is a function of $\Delta w = w_t - w_i$. The template memristor's state variable, w_t, is programmed at 0.5. In this case, once w_i corresponds to a perfect match, $w_i = 0.5$ and $\Delta w \approx 0$. In the absence of a perfect match, lowest I_{out} shows the nearest match that can be attained. Such a behavior is brought about by $\text{PM}_t - \text{NM}_i$ and $\text{PM}_i - \text{NM}_t$ transistor pairs in the cross-coupled structure. An important part of the computation phase is the application of an input ramp, V_{in}, for the matching duration, $t_m = 10\ \mu$s. At each step the applied voltage corresponds to $V_{\text{DD}} = 0.8$ V. Applying this input ramp to the two pMOS pull-up transistors in the memristive inverters structures, P_i and P_t, mimics the behavior of switching and translates the stored states into a time difference between switching points S_i and S_t shown in Figure 1(a). The V_{SS} node illustrates switching between ground and initialization voltage to program w_i at 0.05.

In our simulations, low light levels correspond to memristor's high states ($w_i \rightarrow 0.95$) and conversely high light levels correspond to low states ($w_i \rightarrow 0.05$), as shown in Figure 2(b). Programming of memristor state, w_i, as a function of total photo current shows a capability of writing analog data for each particular light intensity. The curve in Figure 2(c) highlights a valley based on the programming steps of w_i as a function of the incident light. High light levels write low values in w_i, so the valley occurs when w_t is close to its low states. When w_t has a high value low light illuminations result a better match (w_t and $w_i \in [0.05, 0.95]$). The same scenario is applicable for the intermediate states.

The output currents from an array of parallel pixels are subsequently summed to identify either similarity or dissimilarity between incoming and stored images. Thus, the expected mapping function uses this information to map the input pattern, A, to y-th template, B_y, and/or categorizing A in j-th class, C_j.

It worth mentioning that precise programming of memristive devices in different analog values is possible and has already been proven experimentally.[3]

3. CONCLUSION

An integrated memristor-MOS smart sensor block as part of a pattern recognition has been introduced that integrates the multi-state non-volatile memory characteristics of memristor as part of an analog similarity detection circuitry. The integrated structure is based on a new single-inverter pulse-width modulation whereby the light is converted into memristor states. The proposed approach is highly suitable for implementation in pattern recognizers and pattern matching architecture.

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