

A Pulse-Frequency Modulation Sensor Using Memristive-Based Inhibitory Interconnections

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This paper proposes a programmable inhibitory interconnection network between pixels in an array of novel low-voltage Schmitt-trigger-based PFM sensors that will be of interest for future applications in memristor-based early vision processing. In addition, a new low-power inverter-based pulse-frequency modulation (PFM) design and its integration with the network is also presented. To ensure no change in the memristors conductance in the network, the CMOS imager was designed for low voltage operation. That has resulted in a significant power reduction, better than 60%, and a comparable linear dynamic range when compared to published designs in the literature. The design was performed using a 0.13 μm Samsung Electronics standard CMOS process, using 0.75 V supply voltage.

Keywords: Memristive Devices, CMOS Image Sensor, Pulse-Frequency Modulation.

1. INTRODUCTION

The light intensity can be represented either as pulse-frequency (pulse-frequency modulation (PFM)), pulse-width (pulse-width modulation (PWM)), pulse-amplitude (pulse-amplitude modulation (PAM)), or phase (pulse-phase modulation (PPM)) of a signal. The targeted application for the proposed sensor is an early vision processing system using a CMOS image sensor that uses a memristor-based crossbar array combined with either a PWM or PFM sensors. According to Figures 2 and 7 in Ref. [16], PWM and PFM sensors can be used for building a vision chip in combination with a resistive network. With the emergence of new nanostructure and nano-devices and the possibility of integrating some of these devices with main stream CMOS technologies, new approaches for circuits and systems are possible.

One of these emerging devices is the memristor, which was postulated by Leon Chua in 1971 as the fourth fundamental circuit element, that links magnetic flux to electric charge.⁵ This device was later demonstrated by HP at nanometer scale level in 2008.¹⁹ The new device has a non-volatile internal state that can be programmed electrically by controlling the voltage across the device and current passing through it overtime resulting in a linear conductance at some parts of its characteristics.⁹

In bio-inspired imager design, shunting inhibition models of biological vision systems are used to provide local and global adaption mechanisms to improve the quality of captured images to perform some early vision processing such as image enhancement and edge detection.⁴ In some CMOS-based implementations, a resistive network is used to implement the needed convolution kernels.¹³ However, using resistors is both area hungry and suffers from process variation. Another alternative is to use transistors operating in the linear region of operation with their conductance tuned external by controlling the gate-source voltage of these devices.⁶

However, this approach has a number of limitations: (i) the transistors size used is large and its size is dictated by the used fabrication process, (ii) a bias voltage will always be needed to maintain the device operation at a specific conductance, and more importantly (iii) the transistor conductance is not constant as it is a function of the drain-to-source voltage. The later presents an significant issue as interaction between adjacent pixels needs to be constant.¹⁵ Another approach is to use current mode circuit to build these shunt inhibition kernels.⁴ However, area requirements are still an issue in addition to associated process variation and needed control signals. In light of these limitations, memristor, as a fundamental element, presents itself as an ideal candidate in terms of small area, linear conductance and programmability.^{18,7}

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Also, using the memristor will continue to allow higher degrees of parallel processing capability which is well matched with the early vision information processing in mammalian retina.^{7, 23, 20} It is suggested that memristive devices can be used to implement the outer plexiform layer (OPL) and the horizontal and bipolar cells in the inner plexiform layer (IPL).⁷ The photoreceptor layer can either provide a pulse amplitude (PAM), width (PWM), or frequency (PFM) to be compatible with the memristive grid. From a system level design approach, there is a need to design and tested each individual module to ensure an appropriate functionality. For instance, here we proposed a novel PFM circuit which operates at low-voltages close to $V_{DD}/2$ that allows the circuit to works below the memristor's threshold voltage and, as a result, the memristor's conductance is maintained during the mutual inhibitory process.

This paper is organized as follows. Section 2 discusses the PFM sensor concept, followed by a review of previous works on designing PFM sensors in Section 3. Comparison between the proposed PFM sensor and available sensors in the literature is given in Section 4. Section 5 discusses an application of memristive devices in implementing a programmable inhibitory interconnections between PFM pixels.

In this paper, a memristor (memristive device) is a bipolar Resistive Random Access Memory (ReRAM) that its underlying physics of switching and/or gradual change of resistance can be described based on either Valance Change Memory (VCM) or Electrochemical Metalization (ECM) systems. Each cell contains one diode and one ReRAM device (1D1R). These diodes are special designed diodes (two diodes configurations) that enables a 'bipolar' ReRAM device operates with both positive and negative potential differences.

2. PULSE-FREQUENCY MODULATION SENSOR

The core part of the PFM sensor is an oscillator. One of the first oscillators is current-controlled oscillators. Due to a direct relation between frequency and power in these oscillators, a large amount of power will be consumed to produce a high rate frequency and, therefore, they are very attractive for biomedical applications.¹⁶ The conceptual schematic of the PFM digital pixel, which is also known as light-control oscillator (LCO), is shown in Figure 1(a). When the photodiode node (PD) is initially charged to V_{DD} and then its voltage, V_{pd} , decreases in proportion to the incident light intensity. Once V_{pd} reaches a predefined reference voltage level, V_{ref} , the comparator's output switches from a high voltage (logic "1") to a low voltage (logic "0").

The PWM can be achieved by removing the feedback loop and resetting the photodiode using an external input.

One of the basic differences between the two structures is that there is no initial reset phase in PFM, while in PWM the reset signal is controlled externally so the photodiode can be precharged to V_{DD} . So, the operation of a PWM structure can be described mathematically as

$$T_d = \frac{(V_{DD} - V_{ref})C_d}{i_d} \quad (1)$$

where T_d represents the discharge time of the photodiode capacitor, C_d , node voltage, V_{pd} , from V_{DD} to V_{ref} . The i_{dm} shows the total current, which is the sum of photo-current, i_{ph} , and dark current, i_d . Therefore, the pulse width at the comparator's output can be modulated by the incident light intensity.^{3, 10, 14} Therefore, the comparator's output pulls the feedback node (fb) down, so the photodiode is recharged to V_{DD} through the reset transistor, M_{rst} . This scheme shows a multiple-reset structure which reduces the photo-current saturation problem and produces a digital pulse frequency as a result of the iterative resetting scheme. Thus, the operation of a PFM structure can be define as

$$f = \frac{i_{pd}}{(V_{DD} - V_{ref})C_{pd}} \quad (2)$$

where f is the output frequency that acts as input clock for a n -bit inpixel counter, i_{pd} is the sum of photo and dark currents, and C_{pd} is the photodiode parasitic capacitance. There are several advantages in using a PFM pixel. Firstly, the digital output is far more robust compared to its analogue counterpart in terms of the overall noise effects. Secondly, it is far less sensitive to the supply voltage scaling since the optical energy is directly converted into a floating-point like digital frequency, so the pixel's performance constraints are no longer dependent on the output voltage dynamic range. This advantage significantly helps to increases frequency dynamic range and linearity of the conversion process.²² These advantages motivate us to design a new PFM pixel that consumes less power and operates under a relatively low supply voltages to study the inhibitory interconnections between cells.

In the literature, various approaches for designing a PFM image sensor are investigated.^{8, 17, 22} In this paper, we propose a new design for an inverter-based PFM (iPFM), which consumes less power and has a comparable dynamic range with conventional implementations. To obtain this efficient PFM, various Schmitt-trigger gates were used and their effect on the main signal path, power consumption, and the dynamic range were investigated. Simulation results show that, the proposed design, which uses a non-symmetric Schmitt trigger,¹ result in a low-voltage PFM that can operate from a low supply voltage (0.75 V) and provides low-power consumption, while retaining a comparable dynamic range of operation with the conventional Schmitt trigger, inverter-based, or operational transconductance-amplifier-based designs.

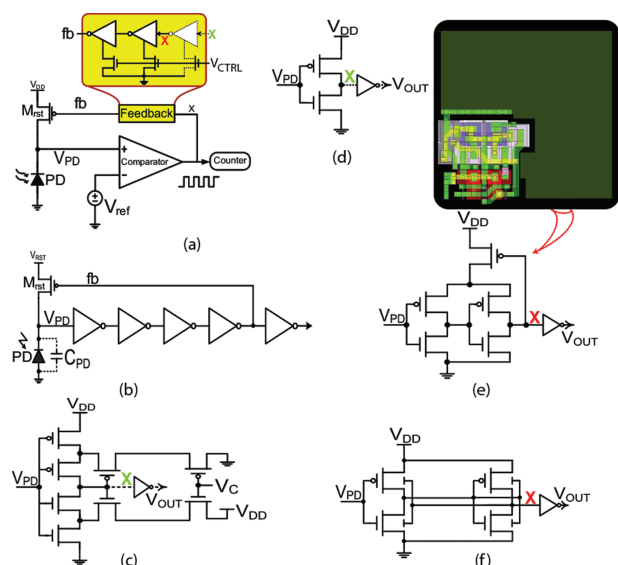


Fig. 1. Pulse-frequency modulation pixels. (a) A generic implementation, indicating the feedback and the main path branches. The yellow box illustrates the feedback inverter chain. If the X signal is shown in green in (c)–(f) the signal passes three inverters and if it is red the signal passes only two inverters. Voltage control, V_{CTRL} , is applied to control the speed of feedback. (b) An inverter-based pixel with all inverters in the main path (pix-conv1).¹⁰ (c) Schmitt-trigger circuit for replacing the comparator in (a). This is a conventional implementation of a Schmitt-trigger circuit (pix-conv2). (d) A single inverter implementation of the main path (pix1). (e) (from Ref. [1]) and (f) (from Ref. [24]) show two types of low power Schmitt-trigger circuits to be used as a replacement for the first inverter. The designs are called pix2 and pix3 in simulations and experiments. This is the first try to combine the pix2 circuit in (e) with a PFM pixel implementation. A $10 \times 10 \mu\text{m}^2$ layout of the PFM pixel based on (e) is also shown.

3. PREVIOUS WORK ON PFM SENSORS

Several parameters should be considered when selecting a comparator these includes, input referred offset voltage, gain variation, area, switching delay, minimum and maximum detectable illuminations, low-voltage operation, etc. An experimental study, in Ref. [22], shows a two-stage comparator and a symmetric operational transconductance amplifier (OTA)-based designs. The switching delay of this comparator is dependent on the voltage difference at the input, while switching delay in the Schmitt trigger is constant due to the inherent positive feedback in these structures. However, this results in a lower frame rate.²² An increase in the integration time is a problematic as this will result in modifying the memristor's conductance.

In order to design a new low power PFM, previous designs could be examined and also some new designs that are not considered in previous studies. Firstly, a design that is shown Figure 1(b) and is named “pix-conv1” in simulations.¹⁰ This design uses conventional inverters that are placed in the main signal path. The first two inverters in this chain are for discharging the photodiode and the last one is to reset the photodiode and start a new pulse. The other inverter that is out of the chain is just a signal

shaping inverter. This design can be modified if the PMOS reset transistor is replaced with a NMOS transistor. This replacement helps having lower power consumption due to removing the short circuit current when NMOS is on at the cost of using more silicon area. In addition, this change results in a better FPN in terms of threshold voltage, V_{th} , variation of the MOSFET devices.^{3,22} Note that a significant amount of consumed power is dissipated by the first inverter. Therefore, to reduce this power the first inverter can be replaced with a hysteresis adjustable conventional Schmitt trigger gate as shown in Figure 1(c). In this figure, only the main path is shown and the photodiode, reset transistor, and the feedback path are omitted to highlight the new changes to the circuits. This design is named “pix-conv2.” Based on our simulations, in order to have a dynamic range similar to previous published designs, the supply voltage should be 0.9 V and because of the power hungry Schmitt trigger this design consumes higher power. Furthermore, the standard deviation of power consumption in this design is relatively high, as shown in Figure 1, implying a highly unpredictable power performance.

One idea that results in lower power consumption is inserting a CMOS inverter between nodes V_{PD} and X, as in Figure 1(d) as “pix1.” The other inverter is the output inverter. This design is also simulated and the results are reported for the comparison, in Figures 2 and 3. Depending on the number of inverters in the main signal path, even or odd number, the output of the main signal path should be connected to an appropriate number of inverters in the feedback. To further reduce the power, the simple inverter was replaced with a low power Schmitt trigger in Figure 1(e) which is previously presented in Ref. [1]. In addition, another Schmitt trigger design for designing a low power PFM is shown Figure 1(f).²⁴ The longed for this paper design expectation implies that choosing a CMOS inverter will be a good approach. The inverter-based PFM (iPFM)

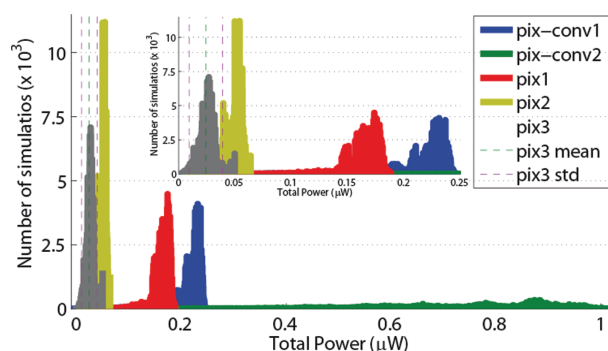


Fig. 2. Power dissipation of the PFM pixels in Figure 1 under a wide range of light intensities. It is clear that the pix2 (Fig. 1(e)) and pix3 (Fig. 1(f)) are far more improved than the other circuits in terms of both mean power dissipation and also predictability of power dissipation under a wide range of light intensities. The pix2 shows the lowest and the pix-conv2 demonstrates the highest deviation from their mean power consumption.

structure present a promising option for low-voltage operation and low-power applications such as implantable devices and mobile applications.^{22, 10} A few types of iPFM pixels have been introduced in Refs. [10, 21] but despite all of these advantages, all of them suffer from: (i) a considerable increase in power consumption, and (ii) the the feedback inverters were placed in the main signal path. The design named pix2 (Fig. 1(e)) shows a better power consumption in terms of variation and mean value, as demonstrated in Figure 1. Figures 1(d) and (e) illustrate the application of one single inverter and a low power Schmitt-trigger circuit in the design of a PFM pixel.

4. COMPARISONS OF THE PFM PIXELS

The proposed cell was simulated using 130 nm mixed-signal CMOS technology. The supply voltage used for analysing the design is 0.75 V, while the nominal V_{DD} of the process is 1.2 V. The feedback inverter chain is also operating from 0.75 V supply voltage. The control transistor is shared between the three feedback inverters and is controlled using $V_{CTRL} = 0.6 \times V_{DD}$ (in Fig. 1(a)), while the reset supply voltage has been set to about the same value. Thus, the control signal can be directly connected to the reset supply voltage. Implemented layout that is shown in Figure 1(e) demonstrates a fill factor of 65%.

A comparison between these cells is shown in Figure 2. A post-layout Cadence simulation at 0.75 V shows better than 60% reduction in the mean value of total power consumption for the proposed structure while the dynamic range and the frequency response linearity are still comparable with the conventional design, as illustrated in Figure 3. Figure 2 shows the proposed circuit consumes 60% less power compare to “pix1,” which has closest power consumption to the proposed structure “pix2.” We have calculated this improvement using mean values of power. Low photo currents range are not shown in Figure 3. The simulations have been carried out using

different light intensities. Low frequencies can be measured (from the actual fabrication) down to a few Hz but a linear frequency response corresponding to the log-scale light intensity ($\text{mW} \cdot \text{cm}^{-2}$) starts around 100 Hz. Therefore, early results show a minimum (detectable intensity) and maximum (maximum intensity) frequencies of $f_{\min} = 100$ Hz and $f_{\max} = 50$ MHz, respectively.

The simulations, however, only carried out in the range of 1 pA to 10 nA to get detectable frequency response from all the circuits. Moving towards high light intensities causes a large nonlinearity at the output pulse-width which should ideally keep a constant value. This nonlinearity then causes a significant degradation in dynamic range as shown in Figure 3. The figure shows the maximum detectable current for both of the designs is to be around 6.7 nA, which corresponds to 60 MHz for the pix2. Clearly, the ratio of the low and high frequencies for all the circuits indicate very close results in terms of dynamic range. Therefore, the pix2 is a design that provides a comparable dynamic range with lower power consumption. The pix3, Figure 1(f), however, shows a better overall performance in Figures 2 and 3. The main reason that the pix3 is not a good option is because of its layout complexity. Connecting body contacts of the MOSFET transistors to any other voltages than the lowest and highest potentials creates a significant complexity in terms of layout implementation and increased pixel area to meet the design rules for wells biased at different voltages.

5. INHIBITORY INTERCONNECTIONS

An inhibitory interconnection can be realised in a PFM image sensor with a simple addition of a reset transistor (Fig. 4(b)), in this case the reset in the pixel controlled by the neighbouring cells and not the pixel's output.¹⁶ This interconnection can be implemented in a flexible fashion by utilising the capabilities of the nonvolatile, programmable, and small area memristive device.

In addition to the programmability and non-volatility of memristors, they are capable of storing multilevel intermediate states. For instance, recently, it has experimentally observed that a memristor is capable of storing up to tens of different states.^{12, 2} This adaptivity can be utilized to serve different purposes in early vision processing. In this paper we have adapted a memristor model in Ref. [11]. The model suggests that the highly nonlinear switching dynamics of the memristor is perhaps due to thermal effects, which implies a switching speed in the range of nanoseconds when a larger voltage than the memristor's threshold voltage is applied. This threshold voltage is around 2.0 V, which is much higher than the image sensor's operational voltage of 0.75 V. Therefore, we neither expect switching nor any change in the memristor's state variable (conductance). Figure 4(a) shows the configuration of pixels that consist of Figure 1(e) and memristive device

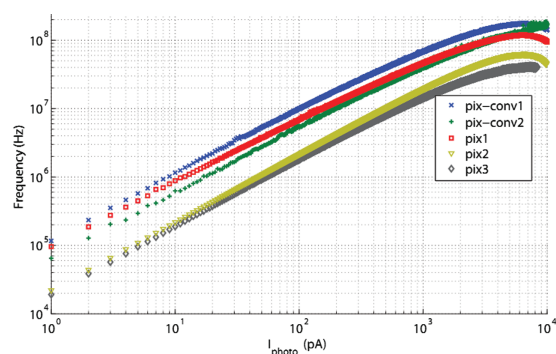


Fig. 3. Dynamic range of the PFM pixels within the range of 1pA to 10nA photocurrent (plus dark current). Clearly, the ratio of the low and high frequencies for all the circuits indicate very close results in terms of dynamic range. Therefore, the pix2 can be considered as a design that provides comparable dynamic range with lower power consumption.

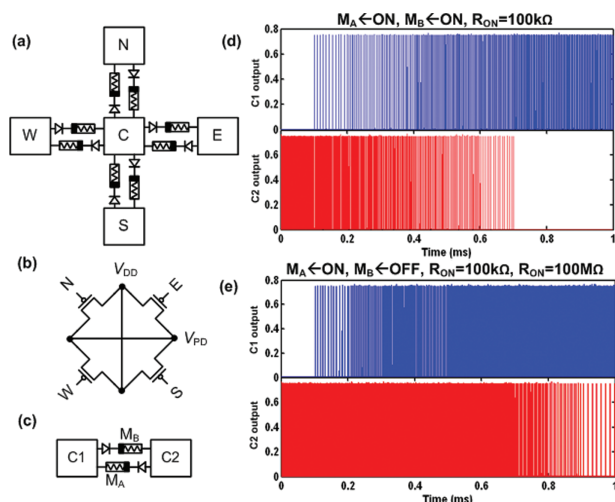


Fig. 4. Mutual inhibitory interconnection in a memristive device based PFM network. (a) The interconnection network as seen by the cell C . The cell C (Center) is connected to E (East), W (West), N (North), S (South) through a memristive device. The diode acts as a selective device to reduce parasitic currents in a crossbar network. (b) The transistors required to connect one cell (C) to four of the surrounding cells (E , W , N , S). V_{PD} is the photodiode node in Figure 1(e). Two pixels are connected using two memristive devices and simulation results are illustrated in (d) and (e). (d) Memristor A and B are ON. $R_{ON} = 100 \text{ k}\Omega$. (e) Memristor A is ON and Memristor B is OFF. $R_{OFF} = 100 \text{ M}\Omega$.

interconnections. Each pixel contains a network of PMOS reset transistors that is connected in parallel with its internal reset transistor between the supply node V_{DD} and the photodiode node V_{pd} . Connections between either E , W , N , or S cells and C are between node X in Figure 1(e) and E , W , N , or S PMOS's gates in Figure 4(b). For simulations, two cells, $C1$ and $C2$, are connected together using two memristive devices, M_A and M_B , that are initially programmed as ON with an $R_{ON} = 100 \text{ k}\Omega$. Cell $C2$ responds to a range of incident lights ranging from high to low, corresponding to high frequency and low frequency outputs, respectively. While cell $C1$ responds to a constant light intensity equal to the average light intensity for cell $C2$. Simulation allows 1 ms time to collect responses. Normally, during the simulation time, $C1$'s output should result in a constant pulse-frequency, while $C2$ output varies from a high pulse-frequency to a low pulse-frequency compare to the $C1$ output. However, because of the given setup and mutual inhibitory interconnections, both outputs should be suppressed each other. This is clearly demonstrated in Figure 4(d), where both memristors are ON.

It is observed that like conventional inhibitory interconnections, firing rates in the two cells suppress each other. When $C2$ firing rate is high, $C1$ firing rate is suppressed and consequently when $C2$ firing rate is low, its output rate is suppressed. To show the flexibility of our approach, we programmed Memristor B on its OFF state, $R_{OFF} = 100 \text{ M}\Omega$ (Fig. 4(e)). This allows the firing rate of $C2$ to suppress firing rate of $C1$ (through Memristor A), the connection between $C2$ and $C1$ can be seen as an open circuit.

Different resistance level programming can therefore result in different mutual inhibitory scenarios. Design of such network requires an extensive analysis of time constant due to the inherent parasitic gate capacitance of PMOS transistor and memristive device's resistance, which set the response time of the transistor in order to suppress firing rate of adjunct cells. In the current approach the memristor's state must stay unchanged. Therefore, utilising a low voltage PFM sensor is important and prevent programming the memristor during operation.

6. CONCLUSION

This paper proposes a programmable inhibitory interconnection network between an array of novel low-voltage Schmitt-trigger-based PFM sensor. The low power Schmitt-trigger circuits helped in reducing the supply voltage requirements down to 0.75 V and at the same time retain the output signal characteristics, such as a constant pulse width, and also dynamic range of the response. The total power dissipation reduced by around 60% and the standard deviation of power consumption is also significantly improved.

The inhibitory interconnections in the proposed sensor uses of a new nanodevice named memristor, which promises a new generation of applications that are not possible using standard bulk CMOS technology. The memristor can be integrated with current CMOS technology. The characteristics of the memristor-based inhibitory interconnections was verified through simulations using an experimentally verified memristor model.

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