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Very high speed differential optoelectronic algorithmic ADC using n–i(MQW)–n SEED technology

S. Al-Sarawi[a,*], N. Burgess[a], W. Marwood[b], P. Atanackovic[b,c], D. Abbott[a]

[a]*Department of Electrical and Electronic Engineering, The Centre for High Performance Integrated Technologies and Systems (CHiPTec), The University of Adelaide, SA 5005, Adelaide, Australia*

[b]*Communications Division, Defence Science and Technology Organisation, P.O. Box 1500, Salisbury, SA 5108, Australia*

[c]*Ginzton Laboratory 1, Stanford, CA 94305-4085, USA*

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Abstract

This paper describes the design of a very high speed optoelectronic analog digital converter based on a digital division algorithm called SRT division using n–i(MQW)–n Self Electro-Optic Effect Device (SEED) technology. The proposed structure is a pipeline ADC. The SRT algorithm was chosen because it provides a redundancy at each stage of the pipeline. The amount of redundancy is dependent on the *radix* of the SRT algorithm and the *number set* chosen. The relation between the SRT *radix*, *number set* and the division full range is given in this paper. Also a macro-model for the n–i(MQW)–n device was developed and used to simulate all the circuitry and algorithmic operations needed for the ADC. These included analog addition, analog subtraction and integer multiplication. Based on the developed macro-model and n–i(MQW)–n SEED circuit modules a basic unit of the algorithmic ADC was designed.

Keywords: Optoelectronic data converter; Very high speed data converter; Algorithmic data converter; Photonic data converter; SRT division

1. Introduction

Ultrahigh speed data converters are becoming a necessity in very high frequency applications such as wideband surveillance systems and digital radio receivers. The common approach is to perform such conversion using electronic components implemented in mature technologies such as CMOS. Although the speed of operation of CMOS circuitry can go up to several GHz, it is still not fast enough to implement data converters that run at or above several gigasamples per second. Another approach is to utilise GaAs circuitry to perform the conversion [1]. However, the bandwidth of such converters is still limited by the bond wire interconnects used for data input as well as the switching speed limitation of MESFET transistors. These limitations have caused researchers to examine both the optical and electro-optical domains rather than just the electronic domain. Examples in the literature where photonics have been used to overcome the limitations of electrical interconnect and switching speeds are Bhushan et al. [2–4] and Cai and Taylor [5]. The use of a Self Electro-Optic Effect Device (SEED) in a time quantised ADC and oversampled ADC has been demonstrated in Refs. [5,6], respectively. New electro-optic devices made with n–i(MQW)–n SEED technology have great potential for these and other high speed applications as they can be integrated with either CMOS [7], GaAs [8] or MMIC [9] technology and can have low operating energy densities. The motivation for this paper is to utilise the n–i(MQW)–n SEED technology in designing very high speed analog to digital converters.

In this research, an algorithmic approach has been adopted for the implementation of the ADC. The reason for choosing the Sweeney, Robertson and Tocher (SRT) division algorithm in contrast to direct binary division is related to the hysteresis characteristics that exists in a SEED quantiser. In particular it is a result of the dependence of the switching speed on the difference between the input powers and will be discussed in Section 4.3. The extremely high speed of SEED technology allows a large number of comparisons to be done relative to common algorithmic ADC structures, leading to better estimates despite the inaccuracy of the quantiser. In addition, the speed can be further increased as there is no need for the quantiser to wait an extended amount of time to ensure that its output has settled to the right logic state.

* Corresponding author. Tel.: +61-8-8303-4705; fax: +61-8-8303-4360.

E-mail address: alsarawi@eleceng.adelaide.edu.au (S. Al-Sarawi).

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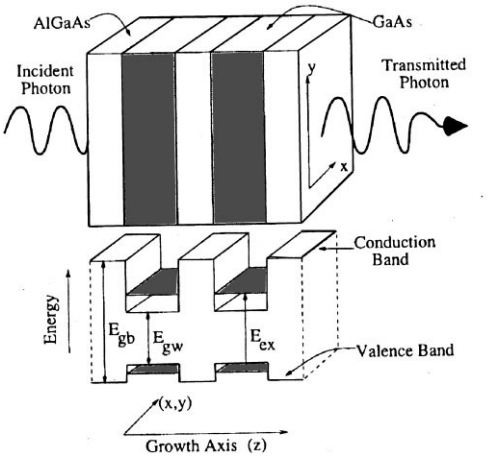

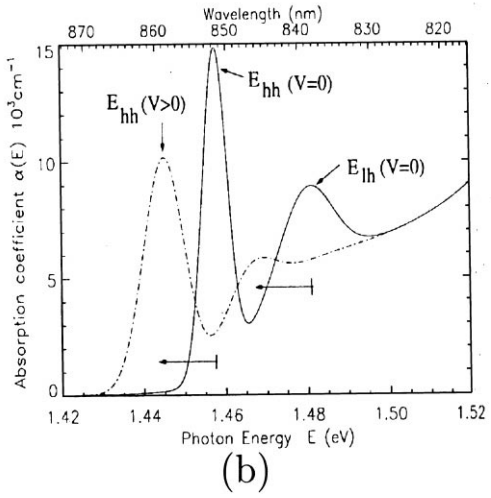

Fig. 1. (a) A MQW device structure with its energy band diagram shown in the lower portion as function of the growth direction. (b) Excitonic absorption spectrum at room temperature for $30 \times Al_{0.3}Ga_{0.7}As/GaAs/Al_{0.3}Ga_{0.7}As$ quantum wells. The zero bias absorption spectrum is shown as the solid curve and the redshift absorption spectrum due to the applied perpendicular electric field is shown as the dashed curve.

As SEEDs modulate power, an unsigned quantity, and the SRT algorithm assumes signed numbers, there is a need to devise SEED circuits in which signed numbers can be represented. Section 2 presents briefly the operation of the SEED and its characteristics. The SRT algorithm and appropriate SEED circuits which implement it are discussed in Section 3. Section 4 presents and discusses new circuit modules that are needed for the ADC and finally, Section 5 presents the basic unit for the differential optoelectronic ADC.

2. MQW device operation

SEEDs [9,10] are fabricated using molecular beam epitaxy (MBE) techniques to grow a series of layers of GaAs and AlGaAs with nanometer thicknesses. The resulting multiple quantum well (MQW) structure can be used to provide a voltage controlled optical non-linearity which allows the device to behave both as a modulator and photo-detector. Fig. 1a shows the energy band diagram versus growth direction for an MQW device, where E_{gb}, E_{gw} and E_{ex} are the barrier bandgap, well bandgap and exciton bandgap, respectively. The absorption spectrum of an unbiased intrinsic 100 Å GaAs/35 Å $Ga_{0.7}Al_{0.3}As$ MQW with 30 periods is shown in Fig. 1b. The two peaks that appear are the heavy- and light-hole exciton peaks, labelled E_{hh} and E_{lh}. The heavy-hole exciton is lower in energy due to its heavier mass. The SEED device usually consists of p–i(MQW)–n diode with quantum-well layers in the *i*-region. It has been demonstrated that a SEED device consisting of an n–i(MQW)–n diode with quantum-well layers in the *i*-region [9] can provide a contrast ratio of 12 dB [11] similar to the p–i(MQW)–n diode with quantum-wells [12]. Hence, good logic states can be obtained optically using n–i(MQW)–n SEEDs with wide analog input/output dynamic range. Further, a difficulty in III–V material is achieving electronic grade p-type dopants, as MMIC technology seldom uses microwave p-type dopants due to poor microwave device performance. Therefore, by using n-type dopants only, a MMIC compatible SEED technology can be realised.

The total photocurrent and dark current contributions, J_T can be written as the sum of the current density due to the MQW, $J_{ex}(V)$ and the thermionic emission of carriers due to dark current and breakdown effects, $J_{therm}(V)$— where $J_{ex}(V)$ and $J_{therm}(V)$ are given by Eqs. (1) and 2. P_{in} is the input power and σ, β and Γ are the width, strength and position of the excitonic response respectively. V, q, k and T are the bias voltage across the device, electron charge, Boltzmann constant and temperature in Kelvin respectively, while θ and ρ are related to an effective barrier height:

$$J_{ex}(V) = \beta P_{in} \ln\left(\frac{1 + e^{(\sigma+V)q/kT}}{1 + e^{(\sigma-V)q/kT}}\right) \times \left[\frac{\pi}{2} + \tan^{-1}\left(\frac{E_{ex} - \frac{qV}{2}}{\Gamma}\right)\right] \quad (1)$$

$$J_{therm}(V) = \theta(e^{\rho qV/kT} - 1) \quad (2)$$

Based on the above analytical model a macro model was implemented in HSPICE [13]. The n–i(MQW)–n device was modelled as a current controlled current source as shown in Fig. 2a. The power dependent I–V characteristics of the n–i(MQW)–n SEED device based on the developed model is shown in Fig. 2b. This model is used to simulate the proposed ADC modules in the next section.

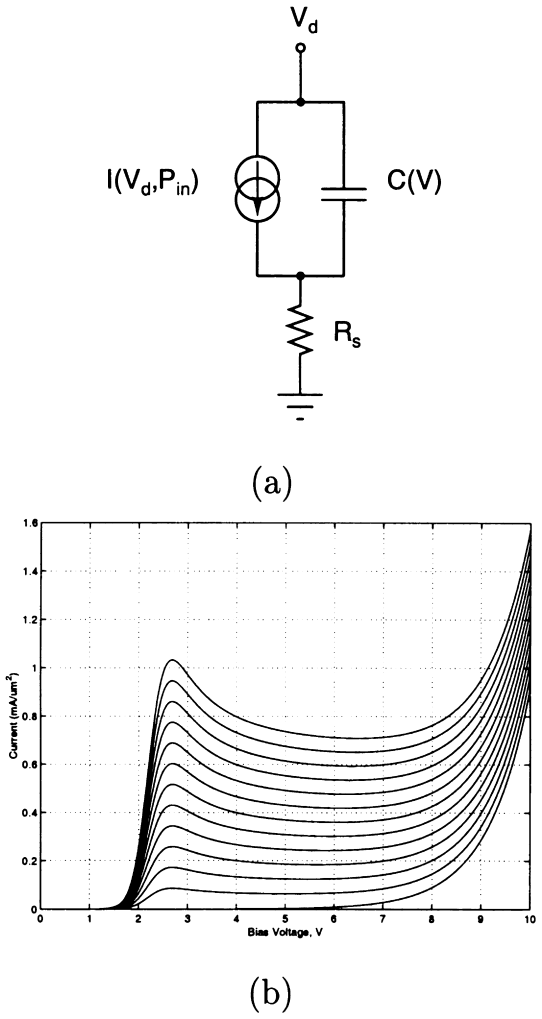

Fig. 2. (a) An equivalent circuit of n–i(MQW)–n SEED device and simulation results using HSPICE simulator.

3. The ADC algorithm

The SRT division algorithm is a digital division algorithm that is named after Sweeney, Robertson and Tocher, who quite independently published separate papers describing it. The radix-2 algorithm for division computes the *i*th-bit of the quotient Q_i, by attempting to reduce the corresponding partial remainder R_i to zero. The basic iteration of the SRT division algorithm (R_0/D) is

$$R_i = \begin{cases} 2(R_{i-1} - Dq_i) & W/2 < R_{i-1} \quad q_i = 1 \\ 2R_{i-1} & -W/2 \le R_{i-1} \le W/2 \quad q_i = 0 \\ 2(R_{i-1} + Dq_i) & R_{i-1} < -W/2 \quad q_i = -1 \end{cases} \tag{3}$$

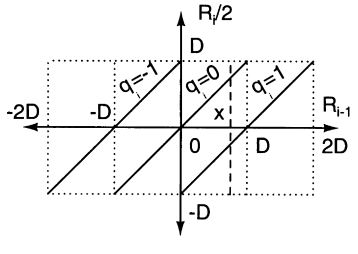

Fig. 3. Robertson diagram for radix-2 SRT division.

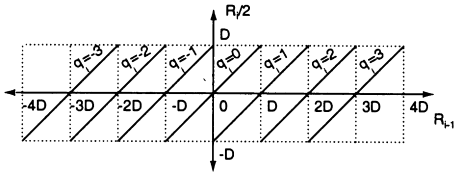

Fig. 4. Robertson diagram for radix-4 SRT division.

Fig. 3 shows the relation between R_{i-1} and $R_i/2$, which is commonly referred to as the Robertson diagram [14]. For the algorithm to converge, $-2D < R_i < 2D$, otherwise repeated subtraction or addition will not reduce the remainder to zero. For radix-2 division $1 \le D < 2$. The above equation can be implemented in hardware as a cyclic ADC as shown in Fig. 5. V_{in}, V_{r} and V_{D} correspond to R_i, W and D, respectively, in Eq. (3). Higher-radix SRT division is also possible at the expense of increasing the hardware complexity. For example, if a radix-4 algorithm is employed with $D = 1$, the basic iteration of the SRT division is

$$R_i = \begin{cases} 4(R_{i-1} - 3q_i) & 6/2 \le R_{i-1} \quad q_i = 3 \\ 4(R_{i-1} - 2q_i) & 4/2 \le R_{i-1} \le 5/2 \quad q_i = 2 \\ 4(R_{i-1} - 1q_i) & 2/2 \le R_{i-1} \le 3/2 \quad q_i = 1 \\ 4(R_{i-1}) & -1/2 \le R_{i-1} \le 1/2 \quad q_i = 0 \\ 4(R_{i-1} + 1q_i) & -2/2 \ge R_{i-1} \ge -3/2 \quad q_i = -1 \\ 4(R_{i-1} + 2q_i) & -4/2 \ge R_{i-1} \ge -5/2 \quad q_i = -2 \\ 4(R_{i-1} + 3q_i) & R_{i-1} \le -6/2 \quad q_i = -2 \end{cases} \tag{4}$$

Fig. 4 shows the Robertson diagram for radix-4 division. The D for radix-4 can range between 1 and 2, but for $D \neq 1$ the boundaries for R_i have to be changed accordingly [15]. The overlap between q_is in Figs. 3 and 4 represent the introduced redundancy into the quotient. For example, for the value of $R_{i-1} = x$ in Fig. 3 one may select q_i to be either 0 or 1 without affecting the quotient digit. The redundancy in the algorithm relaxes the full precision requirement of the division circuit and restricts it to fewer bits in the remainder in the case of radix-2 division. This is analogous to performing coarse quantisation of an analog signal. The redundancy is proportional to the number of the overlap regions and is obtained at the cost of increasing the hardware complexity and the time needed to convert the quotient representation

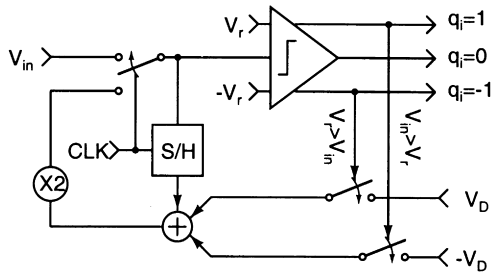

Fig. 5. A possible hardware implementation of Eq. (3).

back to binary numbers. However, although the hardware needed is increased, the time needed to perform each division cycle or stage is fixed as the required number of comparisons are performed in parallel. The time needed for the conversion to binary representation is small as it is composed of simple digital addition and subtraction. Using radix-2 division provides 1 bit representation of the analog input signal and 0.5 bit redundancy, which is used for error correction in the next cycle of the algorithm. In case of radix-4 division with number set $\{\pm 0, \pm 1, \pm 2, \pm 3\}$, the number of bits obtained per cycle is 2 bits with 0.5 bit redundancy. More redundancy can be obtained by using a larger number set such as $\{0, \pm 1, \pm 2, \pm 3, \pm 4\}$ for the same radix resulting in 2 bits per cycle and 2/3 bits redundancy. The relation between the SRT radix, the number set and the redundancy per cycle is given in Eq. (5). According to this equation, the redundancy can be increased by using larger D and a larger number set $q_{\max}$. To minimise hardware complexity, it was decided to use radix-2 SRT division with a $\{0, \pm 1\}$ number set in our ADC design

$$\text{Redundancy} = \frac{\text{Number of overlap regions}}{\text{Full range}} = \frac{D\left(2\dfrac{q_{\max}}{r-1} - 1\right)}{2q_{\max} + 2} \tag{5}$$

As stated earlier, implementing Fig. 5 in a SEED technology imposes a number of difficulties as SEED circuits modulate optical power, an unsigned quantity, whereas the SRT algorithm requires signed operations. To overcome this implementation problem, a differential approach is adopted where the magnitude of all the signals is encoded as the difference between two optical signals. Using this approach, the SRT algorithm can be implemented directly. The conversion *speed* of the ADC can be increased by expanding the cyclic form of the ADC shown in Fig. 5 into a pipeline structure. This approach is discussed later in this section.

The transformation into differential form can be performed if R_i, W, q_i and D are mapped into $(R_{i_H} - R_{i_L})$, $(W_H - W_L)$, $(q_{i_H} - q_{i_L})$ and $(D_H - D_L)$, respectively. Hence, Eq. (3) can be rewritten as:

$$(R_{i_H} - R_{i_L}) = \begin{cases} 2[(R_{i_{H^{-1}}} - R_{i_{L^{-1}}}) - (D_H - D_L)(q_{i_H} - q_{i_L})] & \text{for } (R_{i_H} - R_{i_L}) > (W_H - W_L) \\ 2(R_{i_{H^{-1}}} - R_{i_{L^{-1}}}) & \text{for } (W_L - W_H) \le (R_{i_{H^{-1}}} - R_{i_{L^{-1}}}) \le (W_H - W_L) \\ 2[(R_{i_{H^{-1}}} - R_{i_{L^{-1}}} + (D_H - D_L)(q_{i_H} - q_{i_L}))] & \text{for } (R_{i_H} - R_{i_L}) < (W_L - W_H) \end{cases} \tag{6}$$

The above equation shows that the algorithmic operations needed by the ADC are integer multiplication, which in this case involves multiplication by 2 as we are using radix-2 SRT division, addition, subtraction and comparison. The implementation of these operations in SEED technology and the role of Eq. (6) will become clear through the discussion in Section 4. Eq. (6) can be implemented in hardware as shown in Fig. 6. The architecture can be expanded to form a pipeline ADC while still preserving the redundancy of the

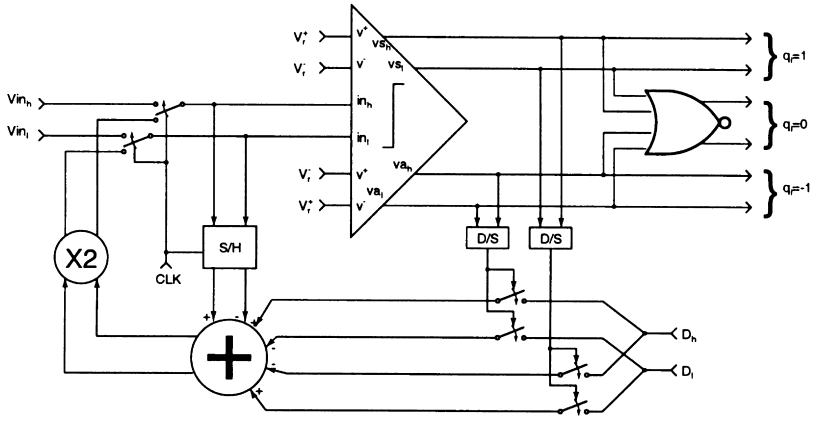

Fig. 6. A possible hardware implementation of Eq. (4).

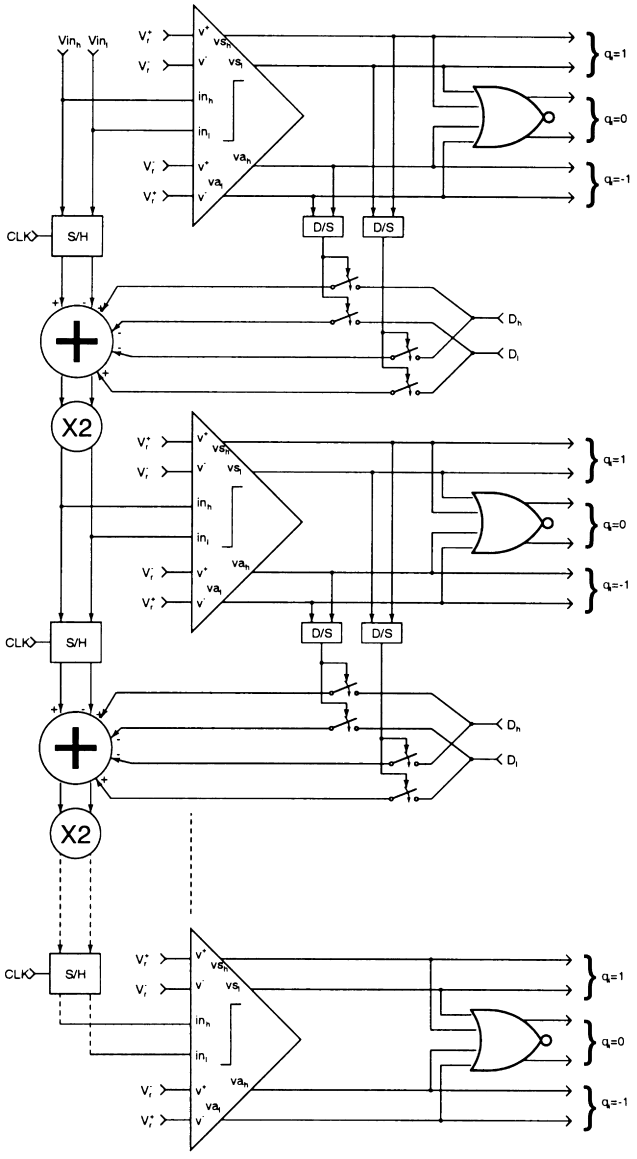

Fig. 7. A pipeline implementation of Eq. (4).

SRT division as shown in Fig. 7. The delays needed to synchronise the digital output and the digital decoder are not shown in the interest of simplicity.

4. MQW circuit modules

From the previous discussion in Section 3 the required algorithmic operations are addition, subtraction, integer multiplication, comparison, differential to single ended conversion, track-and-hold and digital logic circuits. The implementation of these operations are discussed in the following section. For the digital logic circuits the papers of Lentine et al. [2–4] and Atanackovic et al. [9] discuss the design of digital logic circuits using p–i(MQW)–n and n–i(MQW)–n devices respectively, and these circuits will not be discussed here. All other operations are discussed. In the circuit simulations presented, input and output optical powers are relative. In addition, the dynamic performance of the presented circuits is not considered as some of the parameters for the model are yet to be extracted from fabricated test structures. In the following schematics, solid lines represent optical paths through optical wave guides.

4.1. Optical addition and subtraction

The paper published by Miller [16] presented and discussed the implementation of differential optical addition and subtraction circuits using p–i(MQW)–n devices. This paper demonstrates with SPICE simulation that the circuits can also be implemented using n–i(MQW)–n devices. The circuits are discussed in this paper not only to give insight into their operation but also because they are essential for the implementation of the ADC. As stated above, the circuits proposed by Miller are composed of photodiodes and self-linearised p–i(MQW)–n modulators. A schematic circuit for a differential addition and subtraction circuit is shown in Fig. 8. The principle of operation of this circuit can be described as follows: by directing differential optical powers onto the photodiodes, an equivalent current is generated. The direction of this current depends on the sign of the difference. If $P_{\mathrm{in_h}} > P_{\mathrm{in_l}}$ the current will be sourced to the two self-linearised modulators, while if $P_{\mathrm{in_h}} < P_{\mathrm{in_l}}$ the node joining the two photodiodes will sink the difference current. The relation between the differential optical output power and the generated current is given by

$$D_{\mathrm{out}} = D_{\mathrm{os}} + \frac{\hbar\omega}{e} I_{\mathrm{d}} \tag{7}$$

where $\hbar\omega$ and e are the photon energy and the electron charge, respectively. The differential output power, D_{out} is defined as $P_{\mathrm{out_h}} - P_{\mathrm{out_l}}$ and the differential optical supply power, D_{os} is defined as $P_{\mathrm{os_h}} - P_{\mathrm{os_l}}$. Substituting the value of the current as a function of the differential input powers, the above equation can be written as

$$D_{\mathrm{out}} = D_{\mathrm{in}} + D_{\mathrm{os}}. \tag{8}$$

As D_{in} and D_{os} are signed quantities, Eq. (8) shows that addition and subtraction are easily achieved using the presented circuit. In addition, the circuit presents a way to reset the bias level of a differential signal with large offset power into an equivalent differential optical signal with weaker optical supply power. The bias resetting of this circuit is very important as will be seen later in the following section. The circuit will operate as described as long as the input signal power is within the allowable absorption range of the modulators.

Using the developed macro-model, the circuit shown in Fig. 8a was simulated using the HSPICE simulator. The simulation results are shown in Fig. 8b. During the first 20 ps of the simulation the encoded input signal a has a value of 4, and a value of 2 for the rest of the simulation.

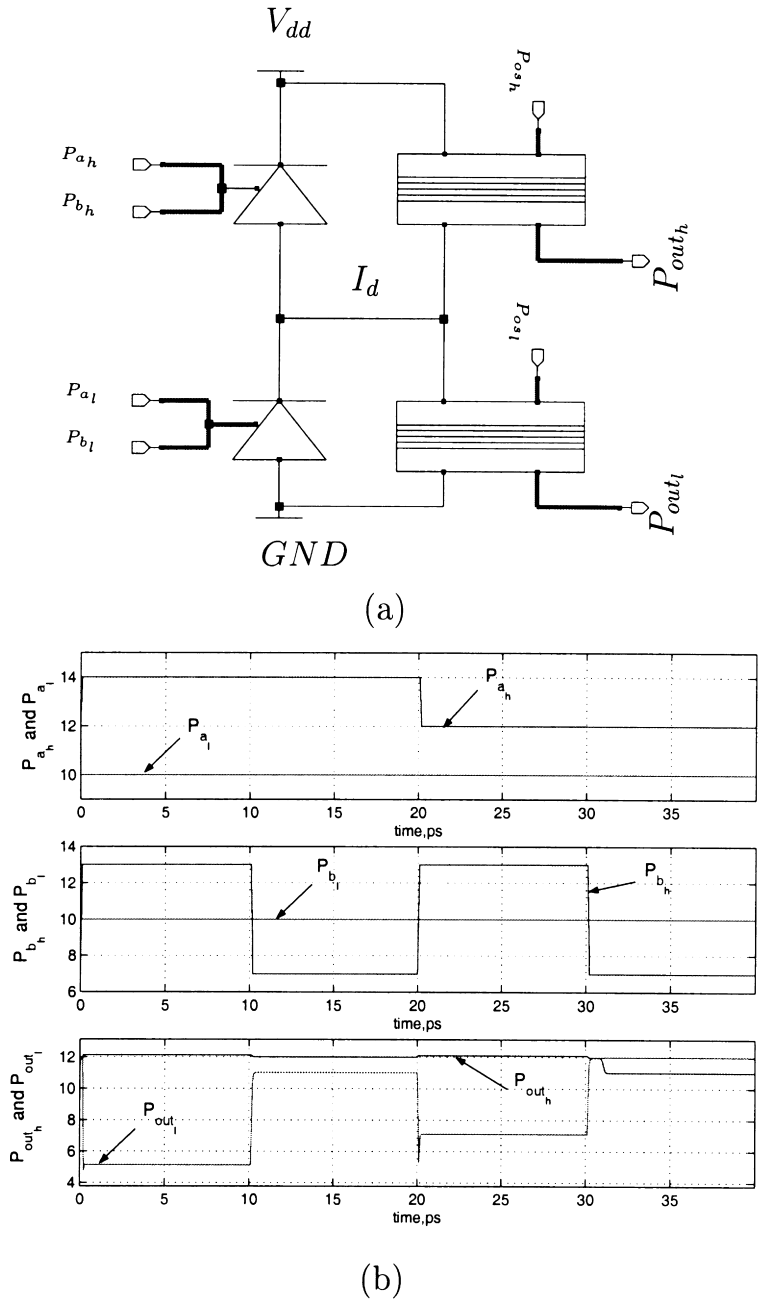

Fig. 8. (a) Self-linearised differential optical addition and subtraction. (b) Simulation results of the differential optical addition subtraction.

Signal *b* was encoded as 2 for the first 10 ps and −2 for the next 10 ps. The bottom panel shows the result of addition and subtraction of the two differential optical signals.

4.2. Optical integer multiplication

Optical integer multiplication is possible (see Miller [16]) by biasing a number *N* of self-linearised modulators using the same current and illuminating each device with its own optical input power. This arrangement can be achieved by connecting all of the self-linearised modulators in series with a current source. Hence, the total optical power from all the diodes is $N \times P_{\text{out}}$ of each modulator. This approach can be seen as a way of generating multiple copies or *replicas* of an optical signal. Another two arrangements are also presented and discussed in Ref. [16] and are referred to as *transmissive* and *reflective* stacks. In all these arrangements, a differential approach is possible. Fig. 9a shows a differential integer multiplication by 2 circuit that uses a transmissive approach. The differential output power can be written as

$$D_{\text{out}} = 2D_{\text{in}} + D_{\text{os}} \tag{9}$$

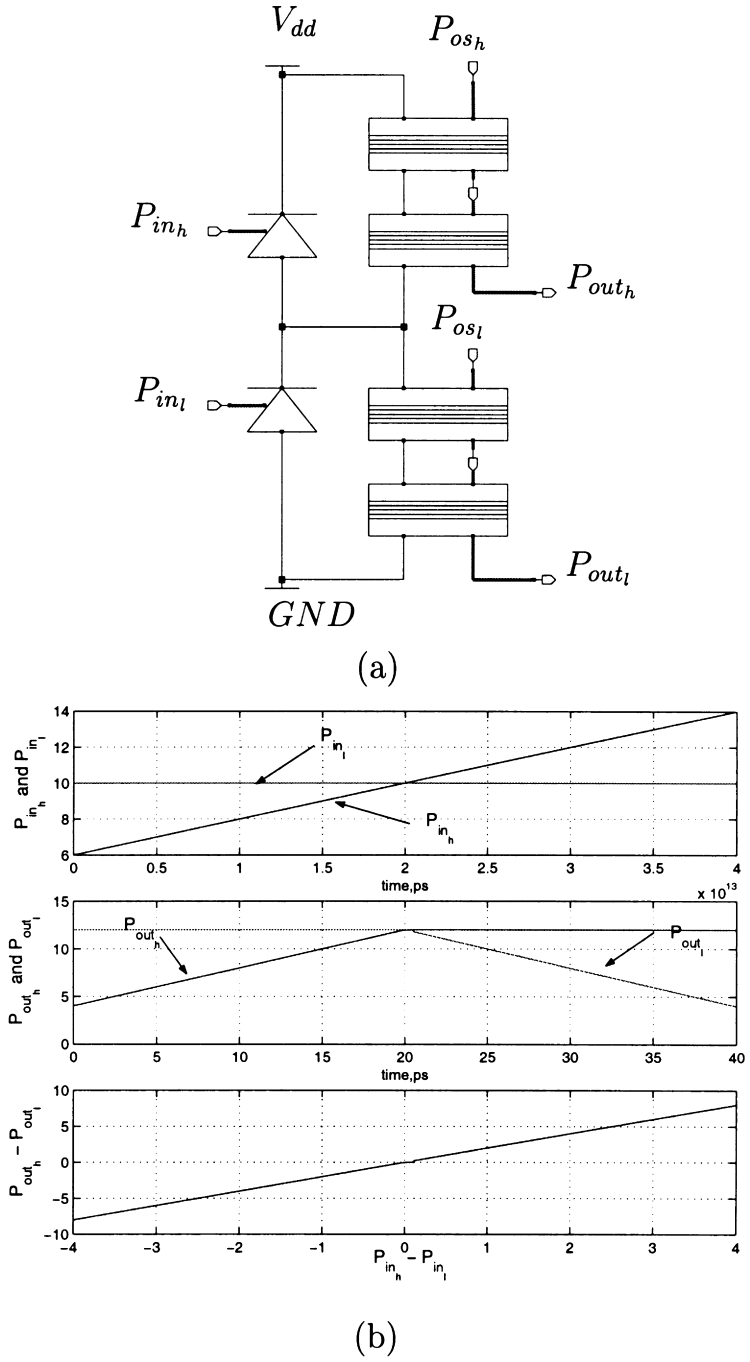

Fig. 9. (a) Self-linearised differential optical integer multiplication by 2. (b) Simulation results.

The simulation results shown in Fig. 9b are in agreement with the above equation, with the exception that the simulation shows a non-linearity when the differential input power changes sign. The non-linearity is likely to be due to dynamic behaviour implemented in the complete model but not shown in the simple form of Eq. (9).

The principle of addition and subtraction described in the previous section can be combined with integer multiplication by illuminating the input photodiodes with the differential signals that are to be differentially added or subtracted, when the resulting differential output signals will be integer multiplied by 2.

4.3. Optical quantiser

The common technique for performing optical quantisation of an optical signal is to connect two p–i(MQW)–n [17] or n–i(MQW)–n diodes between the supply terminals as shown in Fig. 10a. The signal to be quantised is directed onto one diode while the other reference signal is directed

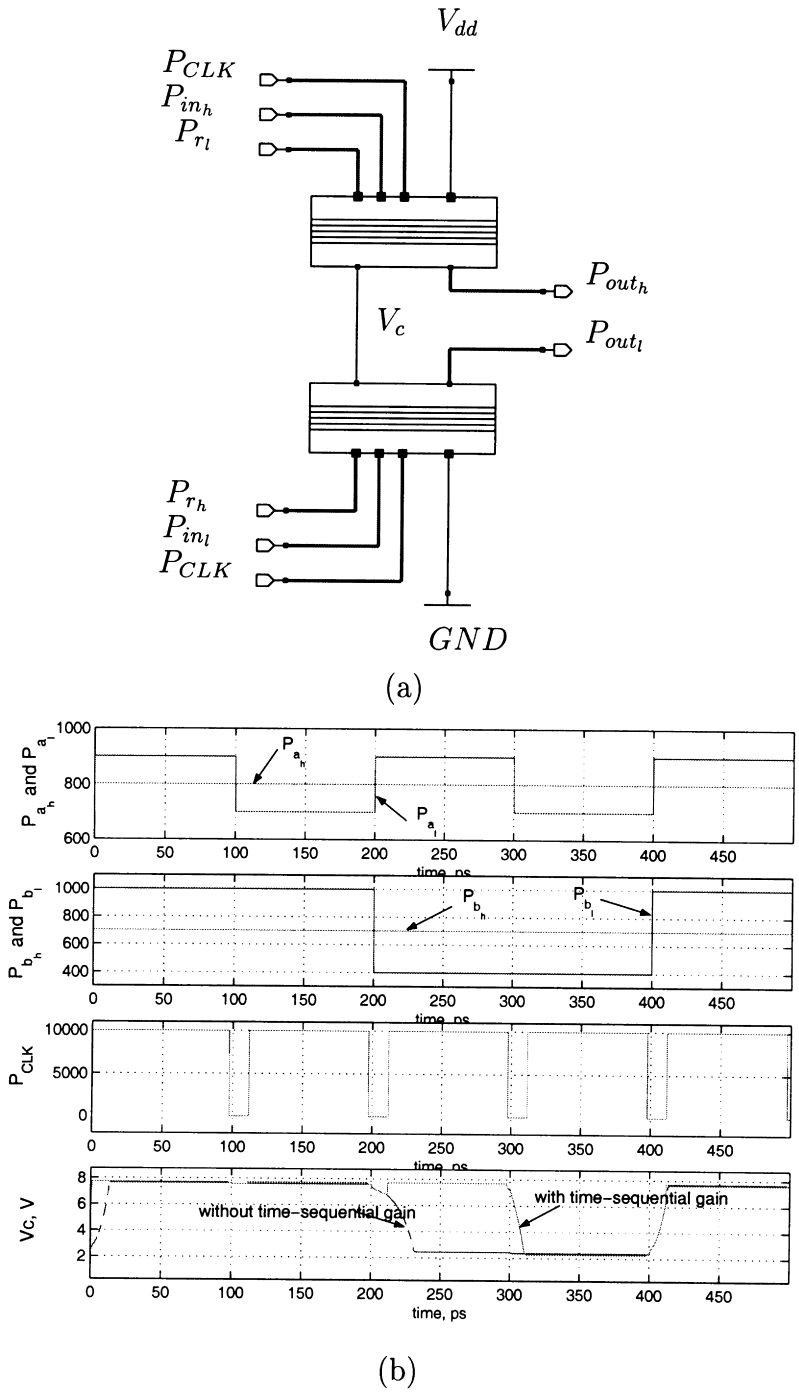

Fig. 10. (a) A differential optical quantiser with (b) its simulation results.

onto the second diode. Based on the relative intensity between the optical signals the circuit switches either high or low. The switching from high to low or vice versa can be accelerated using *time-sequential gain* [17]. Simulation results of the quantiser with and without *time-sequential gain* using the developed macro-model is shown in Fig. 10b. As expected, the simulation shows that the quantisation result can be in error if the quantiser is in a metastable state, was not given enough time to determine its state during the off time of the strong beam.

Because of the inherent negative resistance region in the n–i(MQW)–n and p–i(MQW)–n devices, the switching path from high to low is different from low to high or vice versa. Loh and LoCicero [12] proposed three techniques to reduce the hysteresis. The first is to de- and re-energise the quantiser before performing the comparison. This will result in clearing the state of the quantiser and bias it in an unstable

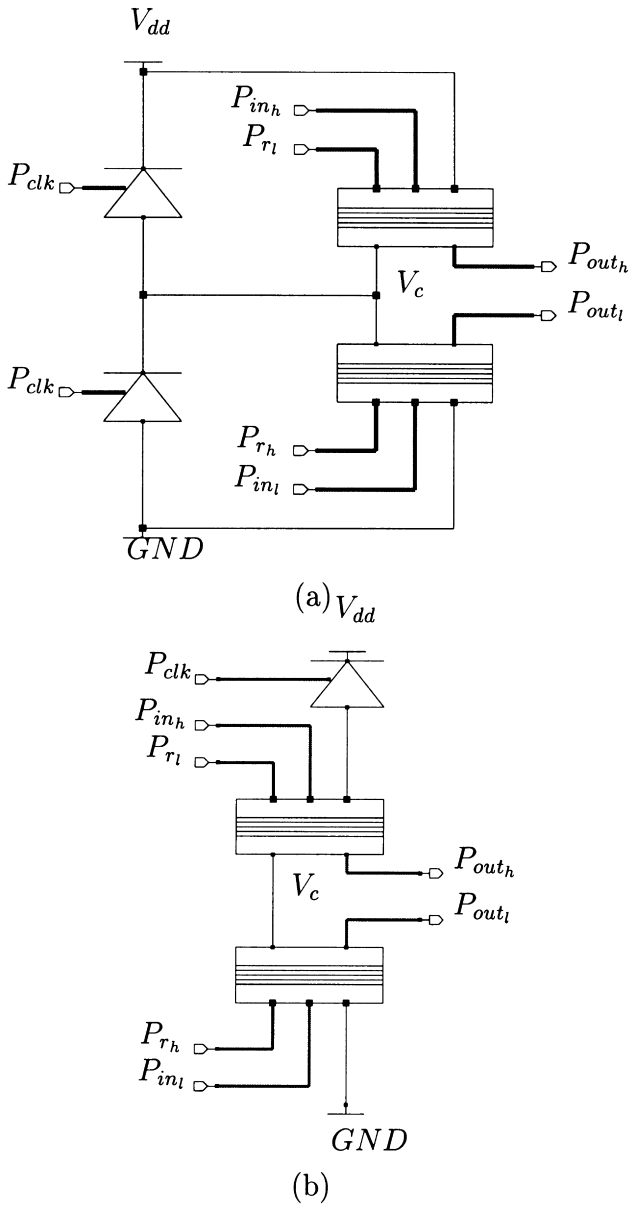

Fig. 11. (a) The first and (b) second techniques for hysteresis elimination in differential optical quantiser.

operating point. A small difference in the input signal optical energy and the reference signal optical energy will result in the quantiser being driven into one of its stable operating points. The second technique relies on operation of the p–i(MQW)–n or n–i(MQW)–n diodes at shorter wavelengths where the p–i(MQW)–n or n–i(MQW)–n diodes operate as photodiodes. Then the two diodes will have one stable operating point and a small difference in the input and reference signals will cause the quantiser to move to a stable operating point after the removal of the short wave length beam. The third technique uses a state-preset pulse operating at a wavelength several nanometers from the optimum wavelength. At this wavelength the I–V characteristics of the two diodes will tilt inward and produce a single point of intersection between the two diode characteristics. A high intensity state-preset pulse whose intensity is greater than that of the applied signals is used to put the quantiser into an unstable operating point. The input and reference optical beams are then applied to the corresponding diodes. Any difference in powers will result in the quantiser moving to a stable operating point after the removal of the state-preset pulse. The problem with the first technique is that it is slow and requires an electrical pulse to control the supply terminals of the quantiser, while the second and third techniques require the use of a different wavelength optical signal, which can complicate the quantiser design.

Two techniques to reduce the hysteresis width are proposed in this work. The first relies on forcing the voltage across each diode in the quantiser to be equal to half the supply voltage. This is achieved by loading node V_c in Fig. 10 with two photodiodes and illuminating them with equal optical powers, as shown in Fig. 11a. The second method, also shown in the figure, is similar to the first method proposed by Loh and LoCicero except that the switching of the quantiser supply voltage is done optically by connecting a photodiode in series with p–i(MQW)–n or n–i(MQW)–n diodes and the control of this photodiode is done by an optical control beam called P_{clk}. In both methods, the P_{clk} beam is used to clear the state of the quantiser. Immediately following the application of P_{clk} the input and reference beams are applied simultaneously to the corresponding n–i(MQW)–n diodes. When the P_{clk} beam is removed, the difference in the input and reference beam will drive the quantiser to either of its stable operating points.

In order to accelerate the switching speed of the quantiser, the second technique for eliminating the hysteresis can be combined with *time-sequential gain*. This is achieved as follows. If a large resistor is placed in parallel with the photodiode in order to slightly bias the two diodes when P_{clk} is *OFF*, the state of the two n–i(MQW)–n diodes will be determined by the difference in the input and reference signals applied when the quantiser has only a small voltage across it. Once P_{clk} is ON, the photodiode will conduct and restore the supply voltage across the quantiser to the full supply voltage. The quantiser will still take some time to move to one of its stable operating points after supply restoration. This switching time can be accelerated by directing P_{clk} onto both the n–i(MQW)–n diodes. The new quantiser is shown in Fig. 12a. The resistor can be removed if the photodiode leakage current is large enough to provide sufficient current to the weakly conducting quantiser's n–i(MQW)–n diodes. The new quantiser was simulated using the HSPICE macro-model with the photodiode replaced by a voltage controlled resistor that has an *OFF* resistance in the order of 10 MΩ and an *ON* resistance of 10 Ω. The simulation results are shown in Fig. 12b. The simulation was conducted with and without *time-sequential gain*. The results shows that the switching speed of the quantiser is effectively the same with and without the

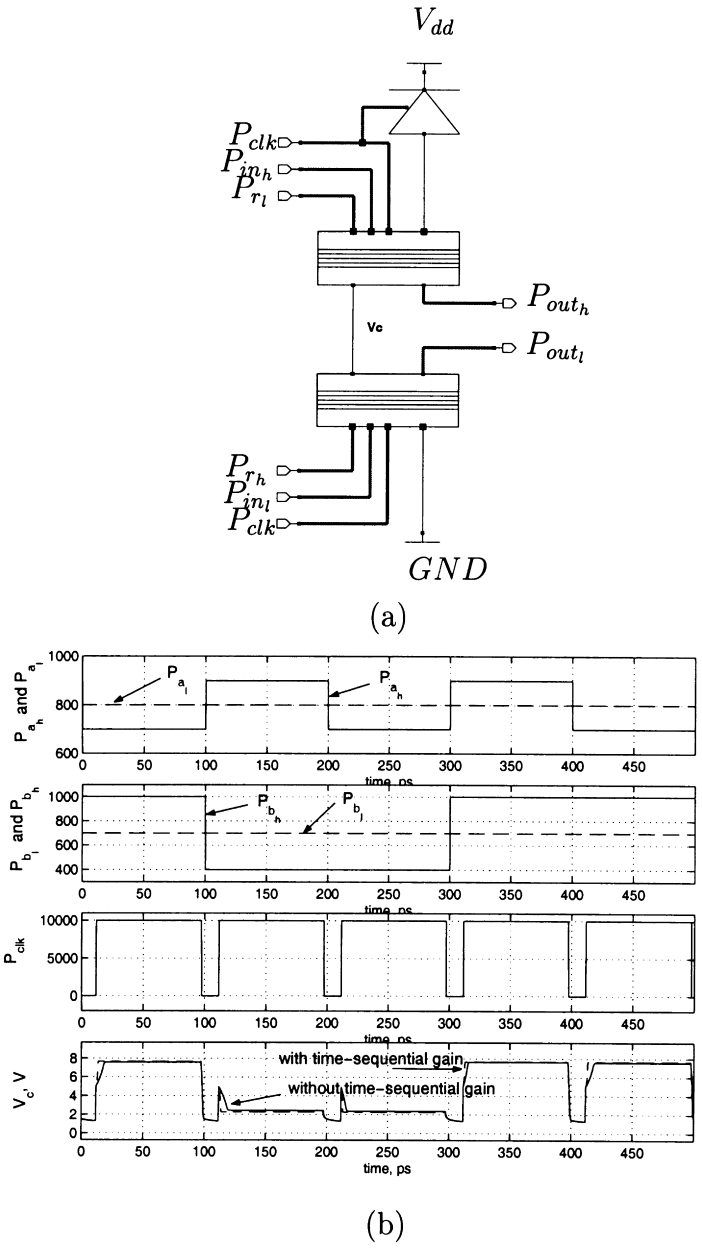

Fig. 12. (a) A differential optical quantiser with eliminated hysteresis and accelerated switching. (b) Simulation result of the differential quantiser with and without *time-sequential gain*.

time-sequential gain. However, some gain advantage may be needed when the difference in the quantiser input signal is very small.

4.4. Differential to single ended optical circuit

Either $D_h - D_l$ or $D_l - D_h$ may be selected for either addition or subtraction with a differential input signal based on the quantiser output. This is achieved using photodiodes to enable the electrical supply terminals of the photodiodes that generate the equivalent current for $D_h - D_l$ or $D_l - D_h$, and as before performs the addition and subtraction in the current domain. As the optical output from the quantiser is in an differential form there is a need to convert it to a single ended form to either switch *ON* or *OFF* the supply terminals of the photodiodes for $D_h - D_l$ and $D_l - D_h$. A circuit to convert a differential optical signal to a single ended form that uses a self-linearised modulator is presented and discussed in Ref. [16]. This circuit is shown in Fig. 13. The relation between the differential optical power beams (P_{in_h} and P_{in_l}), the optical supply beam, P_{os} and output optical beam, P_{out} is given by Eq. (10). For the circuit to work P_{in_h} has to be larger than P_{in_l} and P_{os} has to be larger than the difference $P_{in_h} - P_{in_l}$

$$P_{out} = P_{os} - (P_{in_h} - P_{in_l}). \tag{10}$$

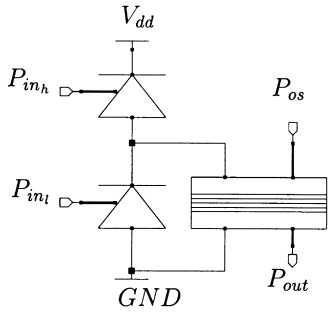

Fig. 13. A differential to single ended optical circuit.

4.5. Optical track-and-hold circuit

Track and hold circuits are considered the *bottle neck* in designing Nyquist rate ADCs as the dynamic performance of these circuits limits the overall performance of ADCs. The design of circuits for very high-speed applications is carried out using GaAs/AlGaAs HBT technology. It has been demonstrated that an 11 bit, 1 GS/s track-and-hold circuit [18] can be designed in such a process. Jitter in the sampling signal has a degrading effect on the performance of the track-and-hold circuits. If a very low jitter optical signal is used to control the track-and-hold circuit proposed in Ref. [18] the number of samples per second can be increased further as sampling time uncertainty is reduced.

The work discussed in this paper has direct application to high performance track-and-hold circuits. Simulation is currently underway of the operation of a fully differential optical track-and-hold circuit. It has a structure similar to the differential light-by-light modulator with two photodiodes acting as switches and a load capacitor to store the input optical sample as an electronic charge. The results of this simulation will be reported in future publications.

5. Optical ADC schematic

Based on the modules presented and discussed in Section 4 the basic unit of the algorithmic optoelectronic ADC is shown in Fig. 14. To fully utilise the optoelectronic technology in the ADC design, the interconnect must be achieved using optical techniques. It is proposed that optical waveguides be integrated within the MMIC substrate for the purpose of optical interconnections.

Final simulations of the optoelectronic ADC in terms of conversion speed and linearity are currently incomplete. Some of the parameters for the n–i(MQW)–n SEED are still to be derived from test structures fabricated at the Commonwealth Scientific and Industrial Research Organisation (CSIRO). However, simulation of the ADC based on estimated parameters, macro-model and modules developed in this paper has been performed and reported.

6. Conclusion

A design for an algorithmic differential optoelectronic ADC based on the SRT digital division algorithm was presented and discussed. An overview of the theory of the n–i(MQW)–n SEED technology together with a description of an HSPICE macro-model suitable for designing analog and digital optoelectronic circuits has been presented. The model was used to simulate basic circuits and good agreement was obtained between simulation and analytical results for a *time-sequential gain* quantiser. In addition, a new quantiser circuit was designed and its operation was

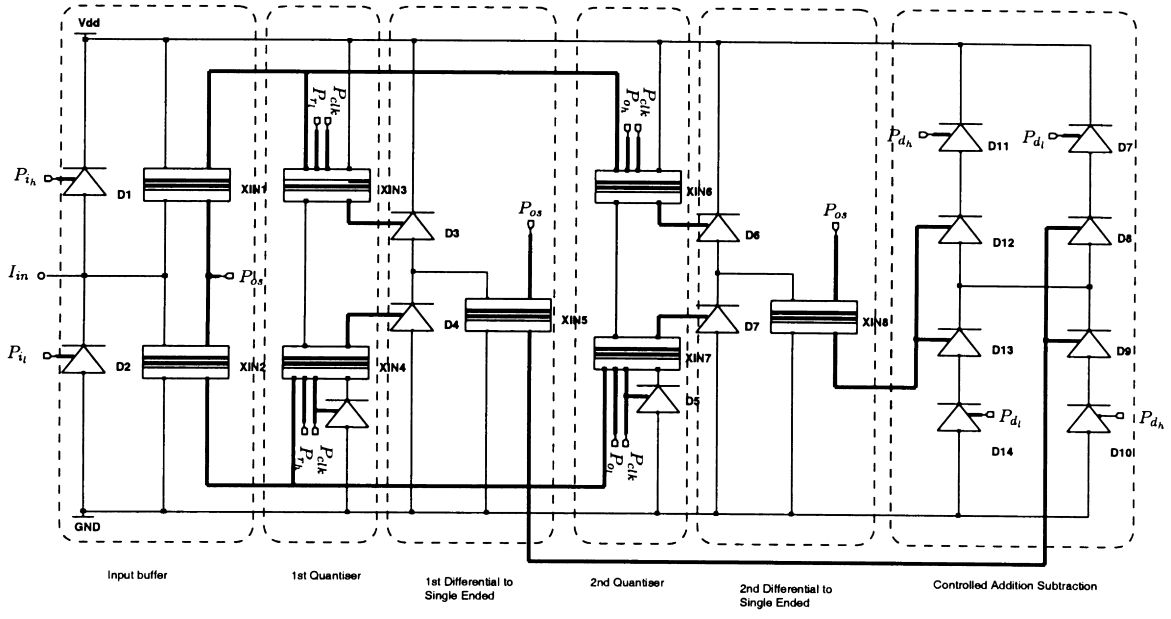

Fig. 14. The basic unit for the differential algorithmic ADC.

verified using the developed macro-model. Using the analytical and HSPICE SEED circuit model a design for an algorithmic SRT ADC was discussed.

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