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Novel extension of neu-MOS techniques to neu-GaAs

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Abstract

The neuron-MOS (neu-MOS) transistor, recently discovered by Shibata and Ohmi in 1991 [T. Shibata, T. Ohmi, International Electron Devices Meeting, Technical Digest, 1991] uses capacitively coupled inputs onto a floating gate. Neu-MOS enables the design of conventional analog and digital integrated circuits with a significant reduction in transistor count [L.S.Y. Wong, C.Y. Kwok, G.A. Rigby, in: Proceedings of the 1997 IEEE Custom Integrated Circuits Conference, 1997; B. Gonzales, D. Abbott, S.F. Al-Sarawi, A. Hernandez, J. Garcia, J. López, in: Proceedings of the XIII Design of Circuits and Integrated Systems Conference (DCIS'98), 1998, pp. 62–66]. Furthermore, neu-MOS circuit characteristics are relatively insensitive to transistor parameter variations inherent in all MOS fabrication processes. Neu-MOS circuit characteristics depend primarily on the floating gate coupling capacitor ratios. It is also thought that this enhancement in the functionality of the transistor, i.e. at the most elemental level in circuits, introduces a degree of flexibility that may lead to the realisation of intelligent functions at a system level [T. Ohmi, T. Shibata, in: Proceedings of the 20th International Conference on Microelectronics, vol. 1, 1995, pp. 11–18]. This paper extends the neu-MOS paradigm to complementary gallium arsenide based on HIGFET transistors. The design and HSPICE simulation results of a neu-GaAs ripple carry adder are presented, demonstrating the potential for very significant transistor count and area reduction through the use of neu-GaAs in VLSI design. Preliminary simulations indicate a reduction of a factor of four in transistor count for the same power dissipation as conventional complementary GaAs. The small gate leakage is shown to be useful in eliminating unwanted charge build-up on the floating gate.

Keywords: Neu-MOS; Neu-GaAs

1. Introduction

Complementary GaAs has a number of highly desirable properties for low-power, high-speed digital and mixed RF/digital applications. These include low-voltage operation (0.9–1.5 V), very low static power dissipation using CMOS-like designs and significantly higher operating speeds than CMOS.

The neuron-MOS transistor (neu-MOS or νMOS for short) was originally developed at Tohoku University in 1991 [1]. The structure of a neu-MOS transistor is identical to an ordinary MOS transistor, but with a number of additional inputs capacitively coupled onto a floating gate, as shown in Fig. 1. MOSFET-style transistor symbols have been used to emphasise the semi-insulating nature of the HIGFET transistor gate. The floating gate potential is a weighted sum of the inputs, the weightings being determined by coupling capacitor ratios.

The use of neu-MOS transistors provides additional functionality which allows, for example, the design of a full adder cell with only eight transistors as compared to 28 in CMOS and an area of 55% of the CMOS design [2].

The goal of this article is to extend the neu-MOS paradigm to the complementary GaAs technology. In particular, we demonstrate the suitability of 0.5 μm HIGFET transistors for application to neu-GaAs [3], present a basic neu-GaAs circuit structure and the simulation results of a neu-GaAs 4-bit ripple carry adder, for the first time.

2. Neu-GaAs basic structure

The neu-GaAs transistor is shown in Fig. 1. Although the gate of a HIGFET transistor is, strictly speaking, not a floating node as in an MOS transistor, the analysis of this structure is identical to that of the neu-MOS transistor given

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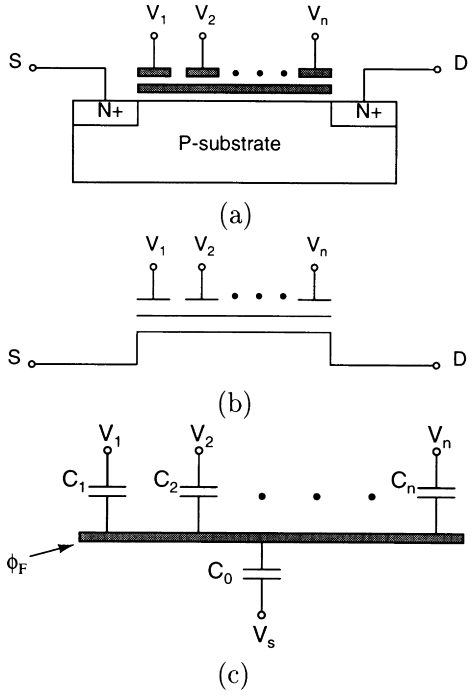

Fig. 1. (a) The structure of an n-type neu-MOS transistor. (b) Its electronic symbol. (c) The capacitance model.

in Ref. [1], and the floating gate potential is given by:

$$\phi_F = \frac{C_1V_1 + C_2V_2 + \cdots + C_nV_n}{C_T} \tag{1}$$

where C_T is the sum of the coupling capacitors C_1 to C_n and $C_0 \cdot C_0$ is the sum of all parasitic capacitances from the floating gate to the substrate, including the floating gate to source and drain capacitances.

A basic variable threshold neu-GaAs inverter structure is shown in Fig. 2. This neu-GaAs inverter is a fundamental building block in digital neu-GaAs design and is similar to an ordinary CMOS-like ratio-less inverter consisting of a p-type GaAs pull-up and an n-type pull-down transistor. The gates of the two transistors are connected and two inputs that are capacitively coupled to this floating gate are added. When the floating gate potential exceeds the inverter threshold, the inverter output becomes low and vice versa. By using two inputs, one of which is to be inverted, V_{in}, and one as a threshold control, V_{ref}, the effective neu-GaAs inverter threshold (as seen from the input V_{in}) can be made variable. The simulation results for three values of V_{ref} are shown in Fig. 3.

3. Choice of GaAs technology

The realisation of neu-GaAs circuits requires that the floating gate voltage remain stable for periods of time depending on the clock frequency being used. This means that a low gate leakage current is required. The HIGFET uses a semi-insulating AlGaAs layer to reduce gate leakage currents (to approximately 2 nA/μm^2 of gate area) and it appears, at least in the short term, as the most viable option for complementary neu-GaAs applications.

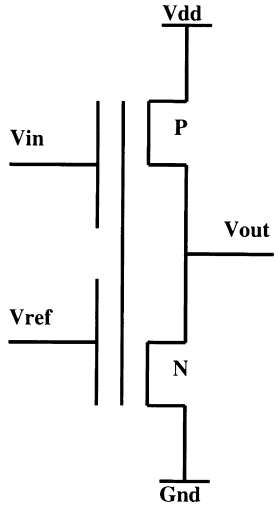

Fig. 2. Basic neu-GaAs inverter structure.

Due to the proprietary nature of the complementary GaAs parameters, Table 1 lists the composite set of HSPICE (level 3, JFET) parameters based on a number of complementary GaAs processes, including Honeywell [4], Sandia [5], University of Lille [6] and MIT [7].

4. A 4-bit neu-GaAs ripple carry adder

A 4-bit RCA was chosen as a simple circuit to demonstrate the feasibility of circuit design using neu-GaAs. Ripple carry adders have relatively low power dissipation, but the delay for computing the final carry depends on the number of bits to be added because the carry propagates successively from the first stage to the last. The basic neu-GaAs full adder (FA) is implemented based on the following expressions obtained from the truth table for addition:

$$c_i = 1 \Leftrightarrow a_i + b_i + c_{i-1} \geq 2 \tag{2}$$

$$s_i = 1 \Leftrightarrow a_i + b_i + c_{i-1} - 2c_i \geq 1 \tag{3}$$

where a_i and b_i are the two bits at the ith position and c_i the carry generated at the ith position. The $+$ symbol denotes algebraic addition, and a_i, b_i, c_{i-1} and c_i take values of 0 or 1 corresponding to 0 V and V_{dd} in the actual circuit, respectively.

As there are no negative voltages in the circuit (there is only a 1.5 V supply), $-2c_{i+1}$ must be converted into $2(\overline{c_{i+1}} - 1)$, hence:

$$c_i = 1 \Leftrightarrow a_i + b_i + c_{i-1} \geq 2 \tag{4}$$

$$s_i = 1 \Leftrightarrow a_i + b_i + c_{i-1} + 2\overline{c_i} \geq 3 \tag{5}$$

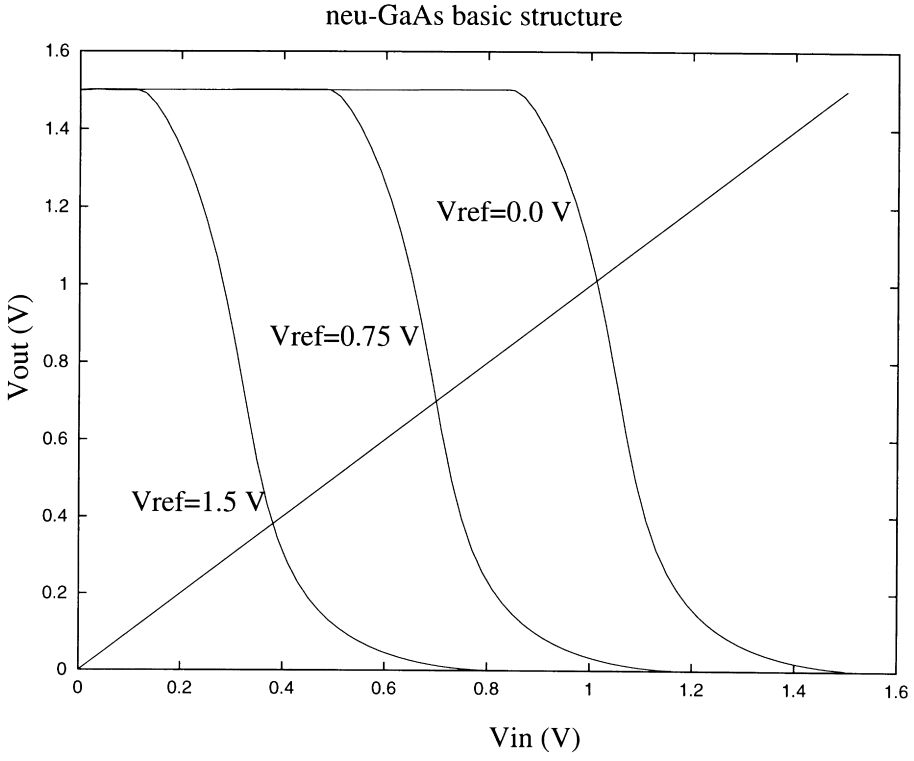

Fig. 3. Neu-GaAs inverter structure simulation results.

It should be noted that in order to compute s_i, $\overline{c_i}$ has to be pre-computed. The neu-GaAs realisation of the two inequality expressions for c_i and s_i is shown on the right-hand side of Fig. 4. The magnitudes of the coupling capacitors for each of the inputs may be found as follows. To evaluate $\overline{c_i}$ from a_i, b_i and $\overline{c_{i-1}}$, Eq. (4) is written in the following form:

$$\overline{c_i} = V_{DD} \Leftrightarrow \frac{a_i V_{DD} C_1 + b_i V_{DD} C_2 + c_{i-1} V_{DD} C_3}{C_1 + C_2 + C_3 + C_0} \geq \frac{V_{DD}}{2} \tag{6}$$

where C_1, C_2 and C_3 are the neu-GaAs structure coupling capacitor magnitudes for the inputs a_i, b_i and c_{i-1}, respectively, and C_0 is as defined in Section 2. Furthermore, C_0 is assumed to be very small compared the sum of the coupling capacitances C_1, C_2 and C_3. The right-hand side of inequality (6) is set to $V_{DD}/2$ which is equal to the threshold voltage of the inverter in the neu-GaAs structure. Comparing inequality (6) with Eq. (2), it becomes clear that by setting $C_1 = C_2 = C_3 = C$, inequality (6) may be rewritten as

$$\overline{c_i} = V_{DD} \Leftrightarrow \frac{a_i C + b_i C + c_{i-1} C}{3C} \geq \frac{1}{2} \tag{7}$$

or equivalently

$$\overline{c_i} = V_{DD} \Leftrightarrow a_i + b_i + c_{i-1} \geq \frac{3}{2}. \tag{8}$$

Since a_i, b_i, c_i and c_{i-1} may take on the values of either 1 or 0, inequality (8) may be written as

$$\overline{c_i} = 1 \Leftrightarrow a_i + b_i + c_{i-1} \geq 2. \tag{9}$$

Thus, the neu-GaAs circuit to evaluate c_i has equal coupling capacitances for each of the three inputs as shown in Fig. 4. The design of the circuit to evaluate s_i follows a similar procedure.

Fig. 4 also compares the full adder cell design in both conventional complementary GaAs and neu-GaAs and shows a significant transistor count reduction in the neu-GaAs design.

Table 1
Composite HSPICE parameters

Parameter name	n-Type (range/value)	p-Type (range/value)	Units
Is	2.4–2.6	2.3–2.6	pA
Cgs	5.5–6.0	7.5–8.0	fF
Cgd	1.8–2.4	3.7–4.1	fF
Vto	0.65	0.52	V
Beta	4.1–4.3	0.9–1.1	mA/V^2
Lambda	0.13–0.15	0.25–0.27	V^{-1}
Alpha	2.2–2.3	2.3–2.4	V^{-1}

5. Simulation results for the neu-GaAs RCA

HSPICE simulations for a single full adder were carried out (Fig. 5). Fig. 6 shows the simulation results for a single full adder while c_{in} is switched. The graph on the right in Fig. 6 shows that there is no degradation of the c_{out} output even when c_{in} is maintained high for an extended period of

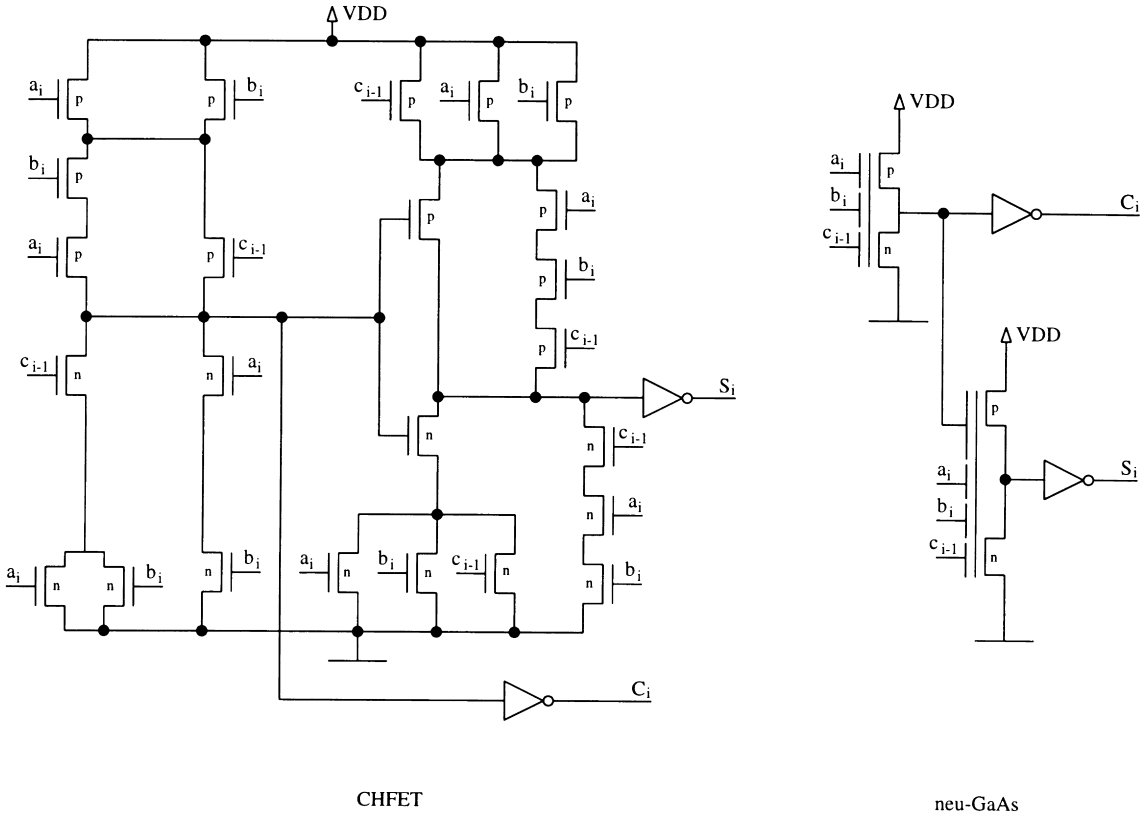

Fig. 4. Conventional GaAs and neu-GaAs full adder designs.

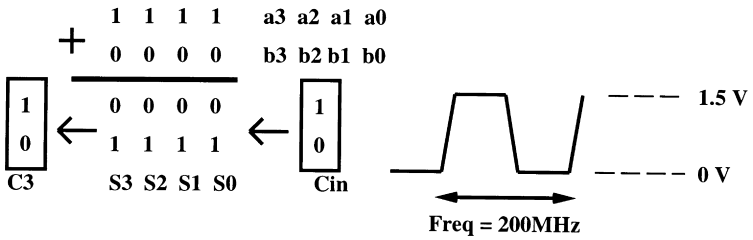

Fig. 5. Switching of c_3 during the HSPICE simulation.

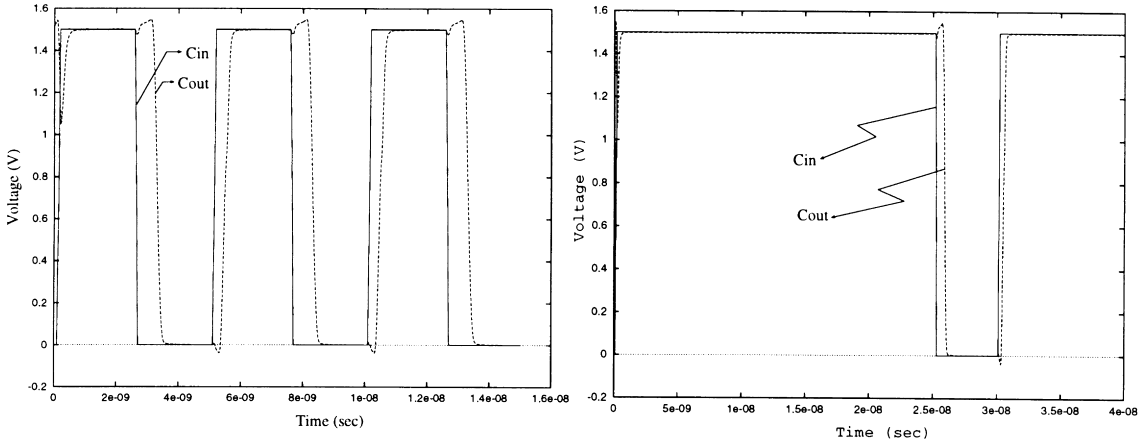

Fig. 6. c_{out} and c_{in} simulation for a neu-GaAs full adder.

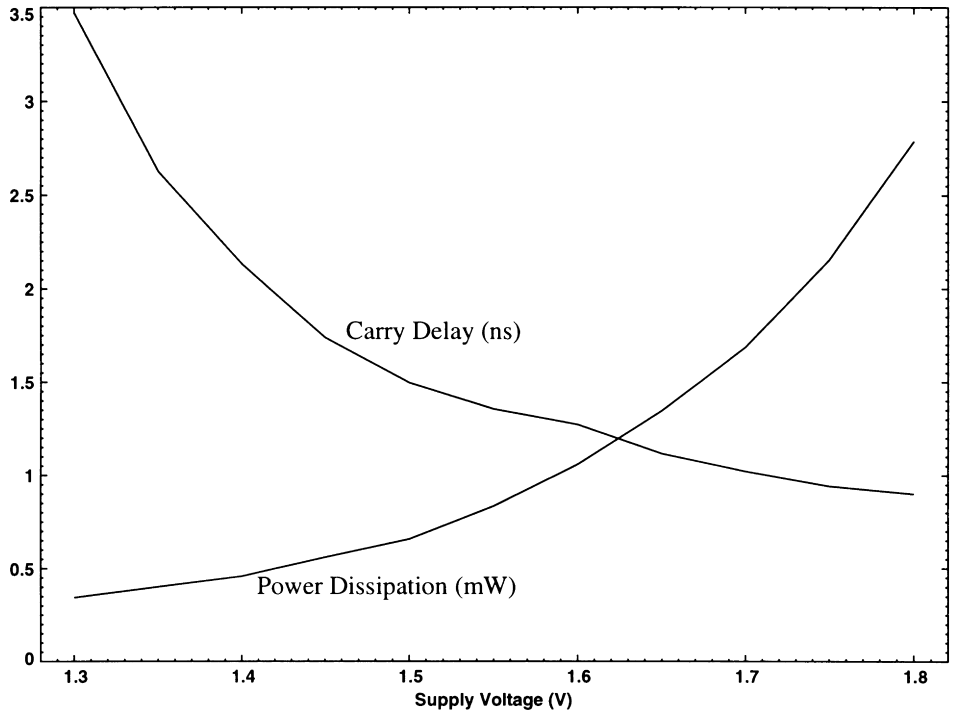

Fig. 7. Delay and power dissipation vs supply voltage for a 4-bit neu-GaAs RCA (vertical axis is power dissipation (mW) or carry delay (ns)).

time (25 ns). The coupling capacitors used were 30 fF for all inputs with the exception of the $\overline{c_i}$ intermediate output, which was 60 fF.

The technique used to simulate the RCA structure using HSPICE is as follows. The two input words were set to $(a_3a_2a_1a_0) = (0000)$ and $(b_3b_2b_1b_0) = (1111)$ as shown in Fig. 5. The c_{in} was switched from 0 to 1.5 V at a frequency of 200 MHz. This causes the output carry c_3 to switch when the input carry c_{in} propagates through the 4-bit slices.

The propagation delay and power dissipation of the carry signal through both the 4-bit neu-GaAs and the 4-bit conventional complementary GaAs ripple carry adders operating at 200 MHz were then measured as a function of the supply voltage. The results are plotted in Figs. 7 and 8. For a typical supply voltage of 1.5 V, the power dissipation and carry delay are approximately equal for both the 4-bit neu-GaAs and 4-bit conventional adders based on the designs shown in Fig. 4.

Table 2 shows the carry delay and power dissipation for both the 4-bit neu-GaAs and 4-bit conventional complementary GaAs adders for a supply voltage of 1.5 V. For completeness, the carry delay and power dissipation for 4-bit RCAs designed in neu-MOS and CMOS using a 3.3 V supply voltage have also been included in the table. For comparison purposes, we have used both 0.5 μm CMOS and complementary GaAs.

Table 2
4 bit RCA simulation results

Adder type	Power dissipation (mW)	Carry delay (ns)
Neu-GaAs (1.5 V)	0.66	1.5
Complementary GaAs (1.5 V)	0.68	1.4
Neu-MOS (3.3 V)	9.0	3.7
CMOS (3.3 V)	0.34	1.9

6. Effects of gate leakage current

Net charge present on the floating gate after the fabrication process in neu-MOS transistors causes fluctuations in transistor inversion threshold voltage [1]. The residual charge on the floating gate can be removed by irradiating the neu-MOS structure with ultraviolet (UV) light. This, however, is an additional step necessary in the construction of neu-MOS circuits. Alternatively, transistor switches connected to the floating gate may be used to set the floating gate potential to a known value and to refresh the floating gate potential periodically.

The proposed neu-GaAs transistor structure does not require a specific procedure to remove residual floating gate charge or floating gate potential initialisation. The reason for this is the presence of a small gate leakage current. This is of the order of 2 nA/μm^2 of gate area.

7. Conclusion

A complementary neu-GaAs structure has been proposed and a 4-bit ripple carry adder based on this structure has been simulated. It has been shown that using neu-GaAs, a very significant reduction in the number of transistors is

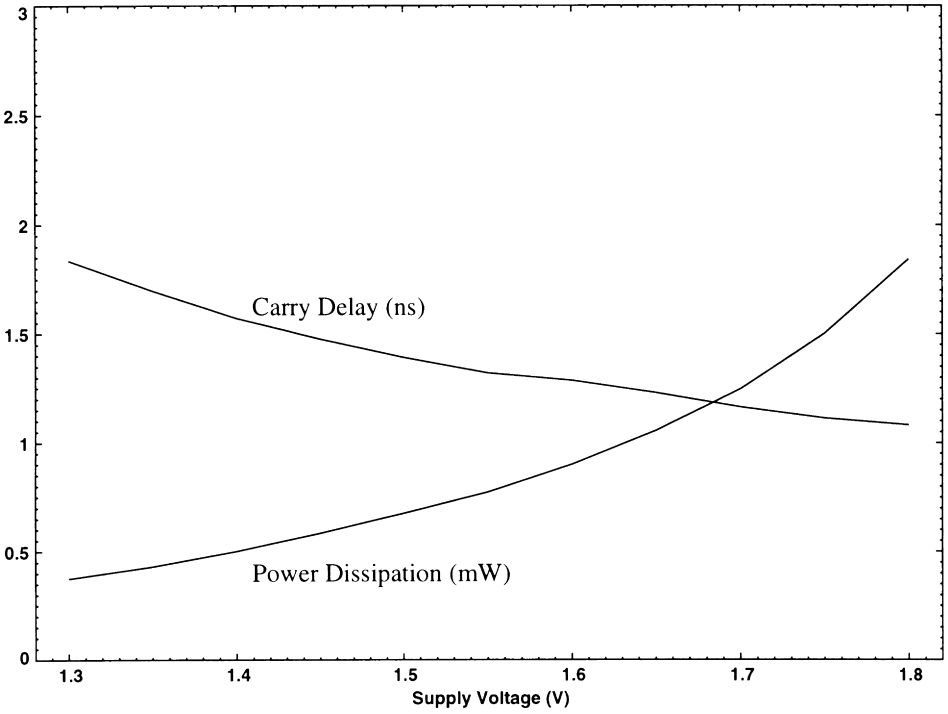

Fig. 8. Delay and power dissipation vs supply voltage for a 4-bit conventional GaAs RCA (vertical axis is power dissipation (mW) or carry delay (ns)).

attainable over conventional complementary GaAs adder designs despite the presence of a small gate leakage current. Moreover, it is anticipated that the gate leakage removes the need for UV erasure of residual floating gate charge as is required in CMOS.

The use of neu-GaAs techniques in HIGFET transistor designs promises to give VLSI designers more freedom in designs where area, delay and power dissipation are critical and provides a step forward towards boosting the effective integration level.

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References

[1] T. Shibata, T. Ohmi, An intelligent MOS transistor featuring gate-level weighted sum and threshold operations, International Electron Devices Meeting, IEEE, New York, 1991 (December technical digest).

[2] K. Hirose, H. Yasuura, Comparison of parallel multipliers with neuron MOS and CMOS technologies, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems 96, IEEE, New York, 1996, pp. 488–491 (November).

[3] D. Abbott, S. Al-Sarawi, B. Gonzalez, J. Lopez, J. Austin-Crowe, K. Eshraghian, Neu-MOS (MOS) circuits for smart sensors and an extension to a novel neu-GaAs (GaAs) paradigm, in: IEEE ICECS98, Lisbon, vol. 3, 1998, pp. 379–404.

[4] D. Fulkerson, S. Baier, J. Nohava, R. Hochhalter, Complementary heterostructure FET technology for low power, high speed, digital applications, Solid-State Electronics 39 (4) (1996) 461–469.

[5] A. Baca, J. Zolper, D. Dubbert, V. Hietala, L. Sloan, R. Shul, M. Sherwin, M. Hafich, Complemetary HFET technology for wireless digital and microwave applications, in: Proceedings of the Symposium on High Speed III–V Electronics for Wireless Applications and the 25th State of the Art Program on Compound Semiconductors.

[6] J. Thiery, H. Fawaz, N. Bourzgui, L. Nuyen, G. Salmer, Temperature dependence of pseudomorphic complementary HIGFET devices electrical characteristics, in: M.S. Shur, R.A. Suris (Eds.), (Proceedings of the 23rd International Symposium on Compound Semiconductors), IOP Publishing, UK, 1997, pp. 523–526.

[7] C. Chen, L. Mahoney, K. Nichols, E. Brown, Self-aligned complementary GaAs MISFETs using a low- temperature-grown GaAs gate insulator, Electronics Letters 32 (4) (1996) 407–409.