GaAs Pseudodynamic Latched Logic for High Performance Processor Cores

J. F. López, K. Eshraghian, R. Sarmiento, A. Núnez, and D. Abbott

***Abstract*— A novel GaAs logic family, pseudodynamic latched logic (PDLL), is presented in this paper. It is composed of a dynamic circuit where the logic is performed and a static latch whose function is to permanently refresh the stored data on a dynamic node. Because of this hybrid structure, PDLL takes advantage of both static and dynamic families and thus, permits implementation of very complex structures with good speed-area-power tradeoff. Moreover, the inclusion of the latch permits this class of logic family to be highly efficient for pipelined systems working even at high temperature without loss of data due to leakage currents. Barrel-shifters, programmable logic arrays (PLA's), and carry lookahead adders (CLA's) were verified by simulations demonstrating its feasibility for the development of high-performance very large scale integration (VLSI) systems.**

***Index Terms*— Gallium materials/devices, logic design, MESFET integrated circuits.**

I. Introduction

THE introduction of GaAs MESFET devices for digital IC design in the past decade, featuring high electron mobility and current gain, led designers to define speed as the main design goal for their GaAs circuits. Analog GaAs quickly established itself as a mainstream technology in high-frequency designs for RF and monolithic microwave integrated circuit (MMIC) applications. However, logic families developed for digital GaAs designs, although demonstrating operational frequencies above 1 GHz, have failed to establish themselves as mainstream and have remained confined to niche or very specialized markets.

Nevertheless, present advanced CMOS technology is far from becoming operational in the GHz clock frequency range, even for deep submicrometer processes [1], and higher power consumption will be a major problem as the technology approaches these clock speeds in the future.

The reason for this failure in competitiveness—other than those related to the large industrial base of foundries and semiconductor manufacturing and design equipment installed for CMOS processes worldwide—has been the power consumption of digital GaAs designs, which is not sufficiently low to allow high integration density as required by today's digital systems. Furthermore, signals having to propagate offchip in a multicomponent system quickly loose their speed at the driver and pad circuitry, which further contributes toward degradation of performance.

Not surprisingly, the present decade has witnessed a change in the design goal of digital GaAs circuits. Low power consumption has become a major issue for industrial success. This has been demanded by the high-performance processor market—in order to meet the high density requirements of advanced very large scale integration (VLSI) processors—the low power circuit market—of exponential growth and bright future in many application domains—and by reliability, packaging, cooling, and cost characteristics related to power consumption. GaAs digital IC designers have come to realize that, in the 500 MHz–1 GHz clock frequency range, by sacrificing some speed performance, large improvements can be obtained in power consumption. The question is whether GaAs can really deliver this new design goal for digital applications. Dynamic logic is one of the options.

In this paper, in Section II we first give a brief background of the different attempts made in order to develop GaAs dynamic logic. Special emphasis is placed upon leakage current problems that arise when operating at high temperature. In Section III, pseudodynamic latched logic (PDLL) is introduced. Complex PDLL structures are shown in Section IV followed by the implementation of different functional blocks presented in Section V.

II. Background and Related Work

Most GaAs designs are restricted to static logic, which suffers from high power dissipation because, unlike CMOS, static GaAs gates have continuous current flow from the supply to ground. In these type of circuits, the load device must be correctly ratioed with the pull-down MESFET's in order to obtain sufficient noise margin and proper circuit operation. This usually means that the design is restricted to the use of NOR gates or in any case no more than two FET's in series can be used in the pull-down network, limiting the complexity of logic that can be implemented per gate.

In an attempt to reduce these two problems related to power dissipation and complexity, there are two options available today. The first entails either improvements in fabrication processes as well as scaling of devices, or, alternatively, the use of complementary heterostructure FET (CHFET) technology [2], which shows promising results in terms of power dissipation. The second approach requires the development of new dynamic logic families, which significantly increases integration density and reduces total power dissipation. The central design principle when implementing dynamic logic is the storing of charge on circuit nodes that can be isolated temporarily from the rest of the circuit. However, in GaAs MESFET devices, the inherent problem of forward gate conduction and high

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subthreshold leakage current reduce the storage time in the isolated nodes.

A. GaAs Dynamic Logic

Up to now, some direct translations of CMOS dynamic logic, mainly domino logic and variations of this structure, have given good results in GaAs. Capacitively coupled domino logic (CCDL) [3] is derived from the dynamic domino configuration by adding a coupling capacitor between the dynamic node and the inverting stage, eliminating the problem of leakage from the forward-biased gate junction and performing level shifting. This results in a greater voltage swing on the dynamic node and a larger noise margin. However, this type of logic needs multiple threshold voltage devices as well as different power supplies. Moreover, the inclusion of an additional capacitor requires additional chip area.

GaAs trickle transistor dynamic logic (TTDL) [4] uses a high-impedance device (the trickle transistor) connected to the dynamic node to compensate for charge lost due to gate leakage currents. In addition, the trickle transistor helps alleviate the effects of charge redistribution and extends operation to low frequencies. The TTDL gate can be considered as a pseudostatic circuit since the trickle transistor behaves as a pull-up device. However, the performance of the logic gate can be affected by variations in an external voltage reference which controls the operation of a diode, and once again the necessity for several voltage supplies introduces new complexities in the design.

Another dynamic circuit is differential pass-transistor logic (DPTL) [5], which uses simple multiplexer-based switching circuits to implement various logic gates. This type of topology achieves some advantages in area and speed compared to static logic [6]. Furthermore, because of its differential characteristic, good noise immunity is obtained. However, the main drawback is the requirement of signal buffering at regular intervals to minimize signal and speed degradation. This introduces additional static power dissipation which limits circuit complexity.

More recently, two-phase dynamic FET logic (TDFL) [7], [8] and split-phase dynamic logic (SPDL) [9] have been presented. TDFL presents an extremely low power dissipation, high density, and a full spectrum of logic functions [10]. SPDL eliminates the external voltage reference used in TTDL and simplifies the logic design. The output voltage swing is automatically adjusted by a split-phase inverter. Although these two topologies have shown promising results, still the leakage currents introduce problems mainly when operating at low frequency and high temperature.

B. Leakage Current

Leakage currents in GaAs MESFET's are a few orders of magnitude higher than those encountered in their silicon counterparts. The metal/semiconductor junction (Schottky barrier diode) is used as the gate electrode of the switch in most of the cases, but also as a diode for both level-shifting and logic applications [11]. This Schottky barrier introduces some problems in both static and dynamic GaAs logic families.

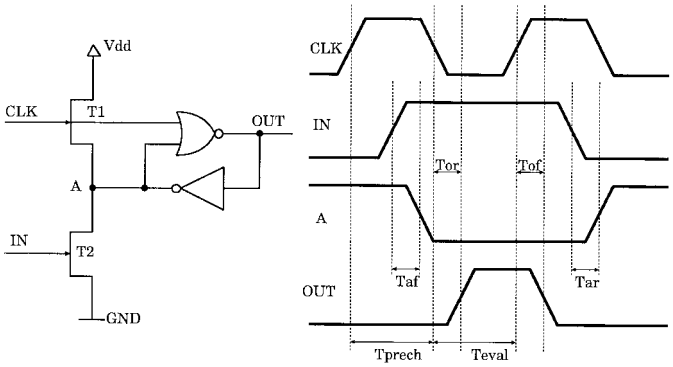

Fig. 1. PDLL latch and operation.

With static logic, noise margins are reduced when an output is connected to a gate which clamps the high level to 0.7 V. On the other hand, dynamic logic is based on isolating a dynamic node from the rest of the circuit—but the current finds a path to ground through the gates of any MESFET's connected to this node, thus degrading the logic value stored. Consequently, the GaAs Schottky gate electrode is not as useful for charge storage as is the case for MOS gates, unless special techniques are introduced in order to avoid this situation. Furthermore, as long as temperature increases, so does the forward-biased leakage current.

It is also well known that in both MOSFET's [12] and MESFET's [13] small amounts of current continue to flow from drain to source for V_{GS} values below the pinch-off voltage. This subthreshold leakage current of the GaAs MESFET is five to six orders of magnitude larger than that of the Si MOSFET. Therefore, the subthreshold leakage current easily becomes an issue in circuit operation.

Because of these two types of leakage current, GaAs dynamic logic gates do not achieve as good performance as their silicon counterparts in terms of storage time. This restricts the applications of the dynamic logic families mentioned before to special cases in which the storage time is sufficiently small (or inversely, when operating at high clock frequency) and when temperature range is limited.

III. Pseudodynamic Latched Configuration

PDLL gates are composed of a dynamic circuit where the logic is performed and a static latch whose aim is to permanently refresh the data stored in the dynamic node. Such a structure allows PDLL to take the full advantages offered by both static and dynamic GaAs logic families featuring low operating frequencies, an increase in functional complexity, and low power dissipation [14]. Because of the PDLL self-latching characteristic, the implementation of highly efficient pipelined circuits becomes possible.

A. Theory and Operation

The basic structure for a PDLL gate (in this case a PDLL latch) together with its timing diagram are shown in Fig. 1.

Transistors T_1 and T_2 form the logic while the NOR gate and inverter form the static latch which is implemented using direct coupled FET logic. It should be noted that the dimensions

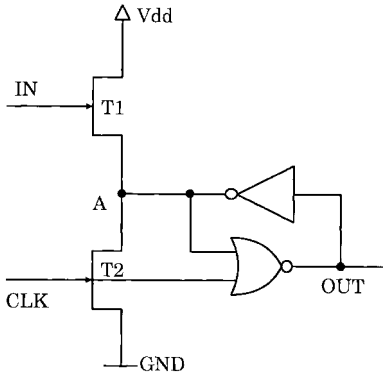

Fig. 2. PDLL inverter stage.

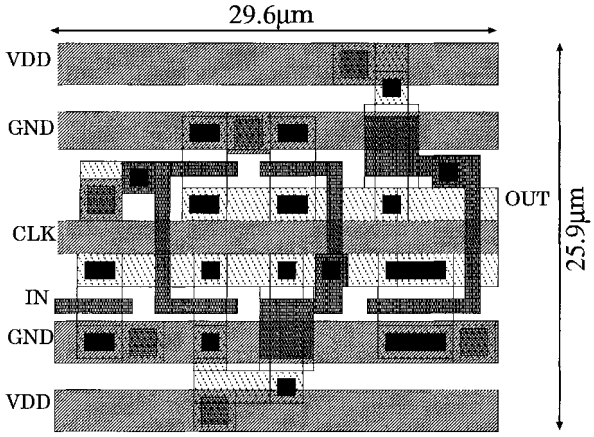

Fig. 3. PDLL latch in ring notation layout style.

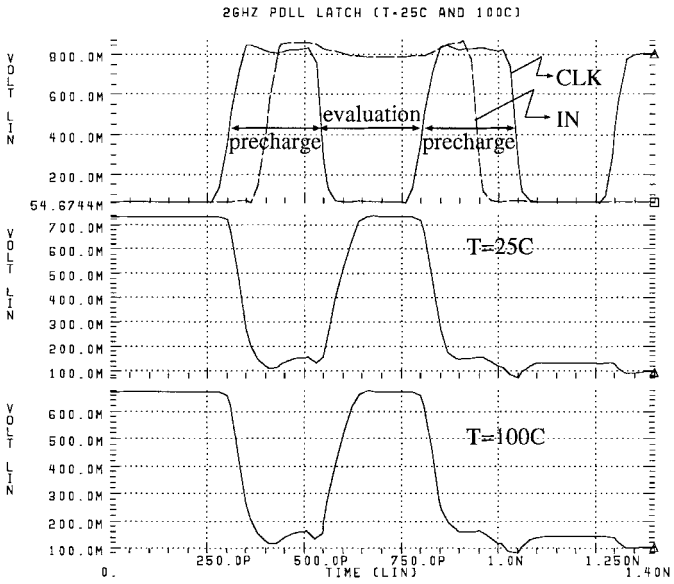

Fig. 4. PDLL latch simulation.

of the latch can be much smaller than normal DCFL gates, thus dissipating less power and reducing area. The operation of this basic gate is synchronized by the clock signal which differentiates between precharge and evaluation phases of the clock cycle. The operation is as follows: when in the precharge cycle ($\Phi = 1$), T_1 is conducting and commences to charge the internal node, A, unless the input is at high level. Because of the forward conduction of the gate-to-source Schottky diode in the NOR gate, the voltage in the internal node is limited to around 0.7 V. When evaluation takes place ($\Phi = 0$), the output of the NOR gate evaluates a logic 0 or logic 1 depending on whether input level was at logic 0 or logic 1, respectively, during precharge.

The structure of a PDLL inverter is shown in Fig. 2, where the operation is very similar to the one described before, with a precharge cycle whenever $\Phi = 1$, and an evaluation cycle when $\Phi = 0$. The output is computed to be the complement of the input half a cycle before.

B. Physical Implementation

The communication paths between cells or groups of cells and the organization and positioning of power and ground buses have significant influence upon the performance of very high and ultra high-speed VLSI systems. Traditionally, nMOS layout style has been implemented placing the logic blocks between power supply, V_{DD}, and ground, GND. However, in very high-speed systems, fast transitions on a signal bus could introduce significant noise on the V_{DD} bus, and thus, special care has to be taken on how to lay out these type of systems. Ring notation [15], [16] has been shown to be an effective methodology, paying particular attention to organizational aspects of *Power* and *Ground* lines in relation to high-speed signal paths. In this approach, GND line is placed between the circuit and V_{DD} line forming two lateral supply buses as shown in Fig. 3 for the case of a PDLL latch.

C. Simulation

Basic gates using Vitesse H-GaAs III 0.6-μm technology, which makes use of enhancement and depletion mode transistors, were laid out and simulated using HSPICE. The MESFET devices have threshold voltages of 0.2 V and -0.8 V for E-MESFET and D-MESFET, respectively. Simulation of a PDLL latch at 25°C and 100°C with a 2 GHz clock frequency is shown in Fig. 4. The total average power with a 1 V power supply is 150 μW, which in terms of power/megahertz-gate gives only 75 nW/MHz-gate.

IV. Complex Gates

PDLL strategy allows the implementation of complex gates such as AND, OR, XOR, and multiple output gates. These structures are introduced in this section.

A. OR and AND Gates

The implementation of OR and AND structures is straightforward by duplicating the pull-down transistor either in parallel or in series as shown in Fig. 5.

B. XOR Gates

The schematic of a compact and high performance XOR gate is shown in Fig. 6 together with its layout using ring notation.

The operation of this XOR gate is similar to the one implemented using TDFL [8]. During the precharge phase,

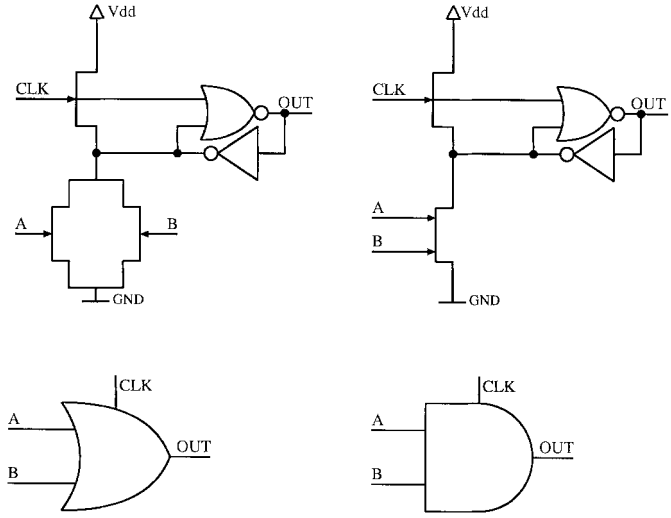

Fig. 5. PDLL OR and AND gates.

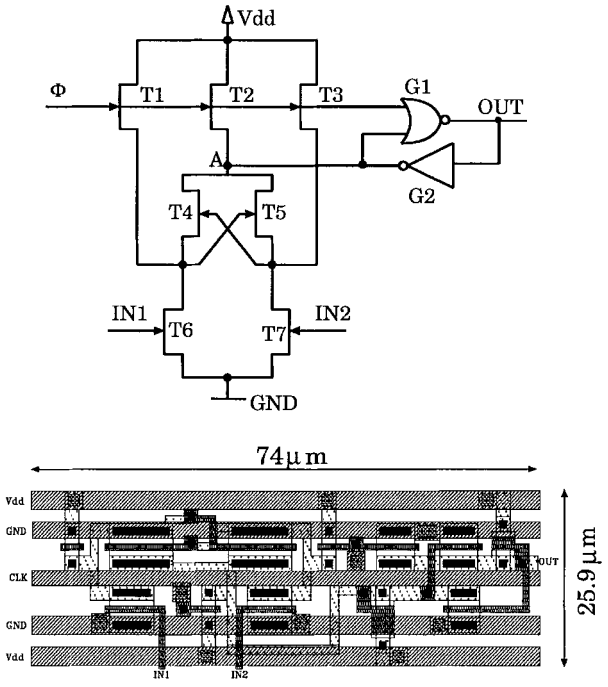

Fig. 6. PDLL XOR structure and layout.

the clock is at high level ($\Phi = 1$) and the output at low level; transistors T_4 and T_5 are both OFF or one of them ON depending on whether the two inputs IN_1 and IN_2 are at the same or different level. This will produce a charge or discharge at node A. When $\Phi = 0$, node A is evaluated and the output will be logic 0 or logic 1 depending on the inputs half a cycle before. For proper operation, transistor pairs T_4 and T_5 and T_6 and T_7 must be reasonably matched. Simulations of the XOR gate predict operation at 1 GHz with a power dissipation of 250 μW. Results also indicate that a 25% transistor sizing mismatch can be tolerated in the design.

C. Multiple Output Gates

Multiple output domino logic (MODL) [17] is adopted with some changes in order to create PDLL structures. The main

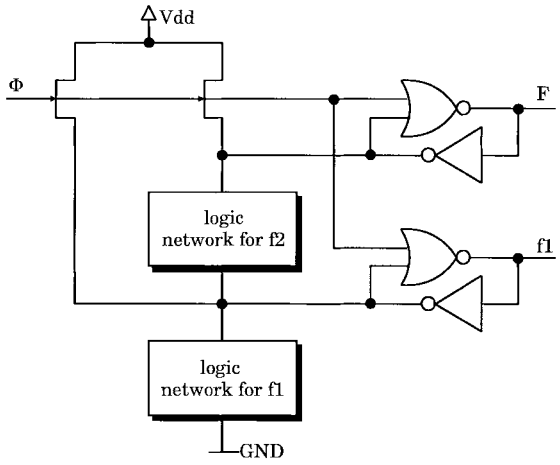

Fig. 7. Multiple-output PDLL structure.

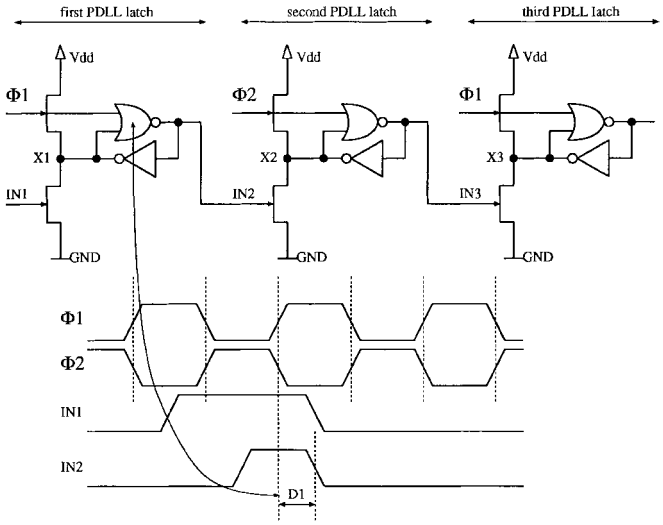

Fig. 8. Switching through a cascade connection.

concept of this type of gate is to exploit the Boolean recurrence presented in the circuit. Reduction in the number of logic stages improves both the speed and power consumption in the overall system. Multiple outputs are obtained by adding precharge devices and static latches at the corresponding intermediate nodes of the logic tree, as is shown in Fig. 7.

In this case, a function F has a subfunction f_1 such that $F = f_1 \cdot f_2$. This type of structure allows simultaneous evaluation of F and f_1. The prime objective is to maximize the use of functional parts which implement the subfunctions, so that the degree of recurrence in the logic functions implemented can be fully exploited. Highly recurrent circuits, such as carry-generating circuits, can exploit this degree of recurrence providing a considerable area reduction in the design. For example, the carry generator block of a 4-b carry lookahead adder using single-output PDLL gates would need 58 devices, while using multiple-output gates requires only 33 devices.

D. Cascade Connection

Since inputs are not allowed to change during the evaluation phase, when a cascade connection such as the one shown

in Fig. 8 is made, differential clock signals are needed, and because of the delay D_1 due to the NOR gate in the first PDLL gate, it is possible to produce a change at the input of the second gate while being evaluated. This does not present a problem at all, because in case there is a change, it always will be from high-to-low transition. If this happens during D_1 ($\Phi_2 = 0$ and $IN_2 = 1$) the static latch will produce a logic 1 at IN_3 due to the logic 1 at the input IN_2 half a cycle before. This forces node X_2 to be low, which is totally compatible with having IN_2 high. After D_1, IN_2 switches to low, and X_2 becomes isolated and controlled by the value stored in the latch which continues holding a high level at the output.

V. PDLL Applications

Different circuits have been designed using the Vitesse H-GaAs III process in order to demonstrate the feasibility and performance of PDLL gates. All of the designs are based on cascading stages and the use of two-clock phases. In the first one, barrel shifters are presented where complex gates are introduced in order to overcome the lack of pass transistors, which is the basic element to implement this type of circuit in CMOS technology. The second example is a programmable logic array (PLA). Finally, a 4-b carry lookahead adder is designed where multiple output PDLL gates are used in order to obtain the benefit of the recurrence in the algorithm for generating the carry signals.

A. Barrel Shifter

When implementing barrel shifters in MOS technology, the designer takes advantage of the capability to use pass transistors and transmission gates in order to save power and layout area [18]. However, pass transistors in GaAs technology introduce difficulties when used in designs, basically because of their nonrestoring capability which produces a loss in logic swing demanding regeneration circuitry after one or two stages. An alternative solution is illustrated in Fig. 9 by incorporating PDLL structures.

The barrel shifter is made of only one basic primitive cell, shown at the top of Fig. 9, which is basically a multiplexer. It is composed of two two-input AND gates connected to a two-input OR gate. The operation of the first stage differs from the second one. In the former, no shift is produced if CTR0 $= 0$, and 1-b down shifting is produced if CTR0 $= 1$. The second stage can shift 1-b down or up depending on whether CTR1 is set to 0 or to 1, respectively. With this scheme, all the possible control vectors for shift operations are shown in Table I.

The total power dissipation for this structure is 4.4 mW operating with a clock frequency of 0.5 GHz.

B. Programmable Logic Array (PLA)

PLA's are common submodules in control systems and are offered as a parametizable part in most VLSI CAD libraries. The complexity of designing VLSI systems can be partially simplified by using these types of arrays, representing an elegant solution to the mapping of irregular combinational logic functions into regular structures [19]. Moreover, because

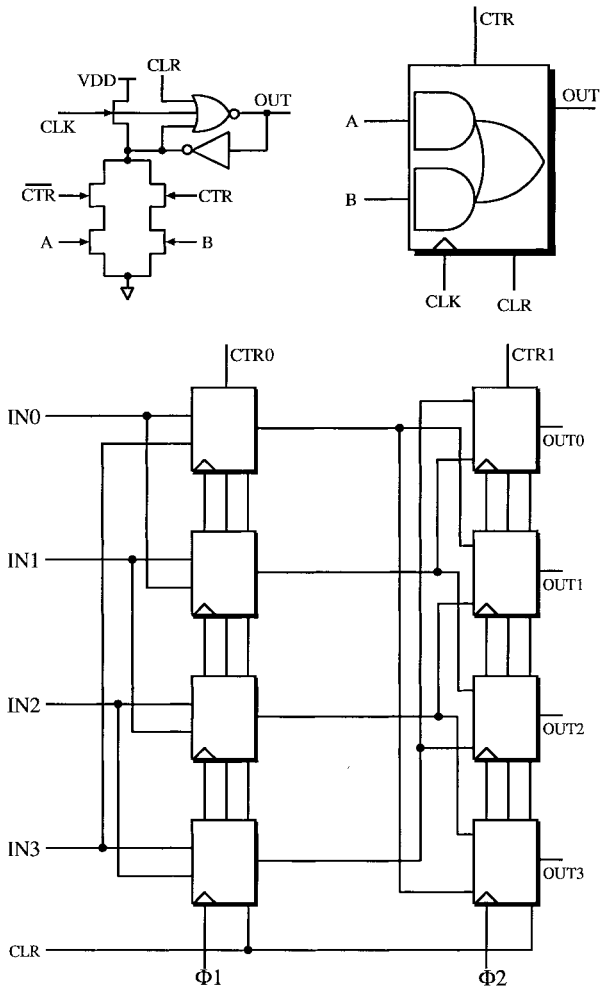

Fig. 9. A 4-b PDLL barrel shifter.

TABLE I
Control Vectors for Shift Operations

CTR0	CTR1	OPERATION
1	1	No shift
0	0	Shift 1 bit
1	0	Shift 2 bits
0	1	Shift 3 bits

of the small number of cell designs required and its rapid expandability, they are attractive options to designers.

The general arrangement of a PLA consists of a programmable two-level AND/OR structure, which implements multiple output functions of n variables in sum of products (SOP) form. The structure can be clearly expanded in any of its dimensions—the number of input variables v, the number of product (AND) terms p, and the number of output (OR) terms, z. However, it has to be noted that for v input variables, there must be AND gates with v inputs, and for p product terms, each output OR gate must have p inputs. Because of fan-in restrictions in GaAs static gates, PLA's solutions have not been explored in depth up to now. However, PDLL-based PLA's are possible because of the capability of implementing large fan-in OR and AND gates.

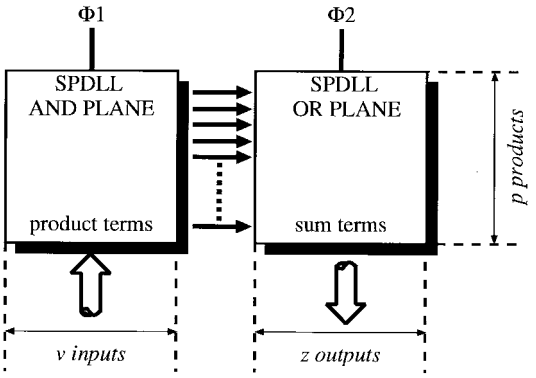

Fig. 10. SPDLL programmable logic array.

Due to its simplicity and low power dissipation, direct coupled FET logic (DCFL) is the logic family used in the implementation of the static latch in any of the PDLL structures presented. However, DCFL does not perform well as fan-out and/or load capacitance are increased. In these cases, other static logic families rather than DCFL are used, as is the case for super-buffered FET logic (SBFL). With this topology, PDLL structures have a higher power dissipation but are not restricted to stringent conditions at the output. This leads to the concept of super-buffered PDLL (SPDLL) gates. SPDLL latches designed to drive 0.1 pF of load capacitance dissipate 0.7 μW/MHz. For comparison with representative silicon VLSI technology, a 0.8-μm CMOS gate operating at 5 V requires approximately 5 μW/MHz for the same loading conditions, while BiCMOS is in the order of 8 μW/MHz.

The SPDLL concept is applied to the implementation of PLA's in order to be able to support the high fan-out and load capacitance at the output of each of the two planes, as can be seen in Fig. 10.

Here, each of the two blocks is controlled by differential clock signals (Φ_1 and Φ_2), and there are as many products as AND gates (each of them with up to v inputs) and as many outputs as OR gates (each of them with up to p inputs).

As an example, a $4 \times 8 \times 8$ PLA has been simulated at 25°C, typical process, with a clock frequency of 0.5 GHz giving a power dissipation of approximately 10 mW.

C. Carry Lookahead Adder (CLA)

Since addition is a fundamental arithmetic operation in processor designs, improving the efficiency of addition is always an attractive research topic. The CLA is one of the fastest algorithms [20], [21]. Improvements are possible on the implementation of this algorithm by exploiting its recurrence characteristic using multiple output PDLL gates [22].

The block diagram of the adder is shown in Fig. 11, where three different blocks are distinguished: the gp block, the carry-generate block, and the sum block.

Each block is controlled by a differential clock signal, ϕ_1 or ϕ_2, and PDLL latches are introduced in order to ensure proper timing due to the sequential nature of the structure. Since signals propagate through three PDLL gates, the latency of the adder is one-and-a-half clock cycles (half a clock cycle per gate).

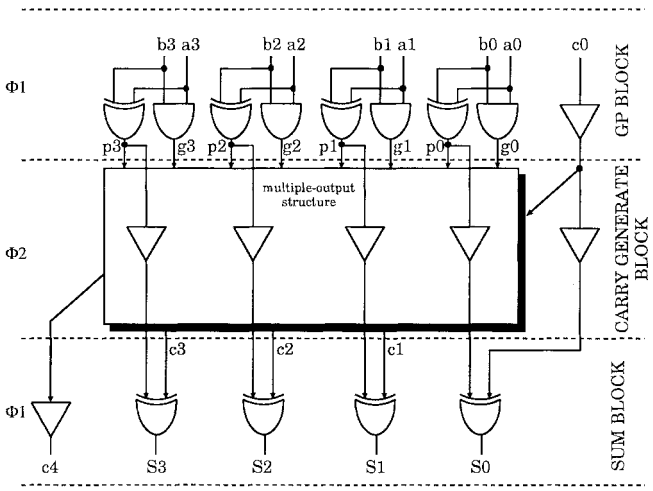

Fig. 11. A 4-b carry lookahead adder configuration.

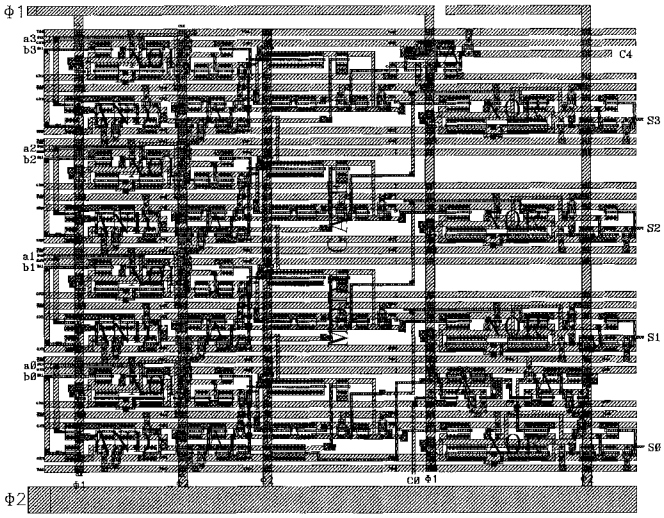

Fig. 12. A 4-b PDLL carry lookahead adder.

The 4-b CLA has been designed and simulated up to 833 MHz, in temperature range from 0 to 100°C, giving a power dissipation of 5.2 mW with a 1-V power supply that corresponds to 0.15 μW/MHz-gate. The design is composed of 210 transistors occupying an area of 0.05 mm^2. This gives a density of 4200 transistors per mm^2. Fig. 12 shows the layout of the 4-b adder, where clock lines are optimized in order to have the same parasitic load for both phases.

Comparison of the CLA implemented in PDLL with other GaAs static and dynamic logic families such as DCFL, buffered FET logic (BFL), CCDL, TTDL, DPTL, TDFL, and SPDL is shown in Table II, where a figure of merit, η, is introduced to represent the performance in terms of $frequency/area \cdot power$.

It can be seen that in terms of power dissipation, area, and figure of merit, TDFL and PDLL are by far the best choice. However, due to the low noise margin levels and the use of pass transistors, circuit operation in TDFL is critical at high temperature because of leakage currents, as discussed in Section II. SPDL presents as its main characteristic a

TABLE II
COMPARISON OF PERFORMANCE FOR SEVERAL GaAs LOGIC FAMILIES

Logic family	Area (mm^2)	F_{max} (MHz)	Power (mW)	η ($MHz/mm^2 \cdot mW$)
DCFL [23]	0.32	714	47	47
BFL [23]	0.75	500	190	3
CCDL [23]	0.70	900	96	13
TTDL [4]	0.55	1250	130	17
DPTL [6]	0.35	1000	228	13
TDFL [10]	0.16	770	1.7	2831
SPDL [9]	0.30	1520	40	127
PDLL	0.05	833	5.2	3204

high operating frequency, but its power dissipation and area utilization, close to DCFL, makes its figure of merit η to be in a low range. PDLL is located in between these two options, offering an extremely low chip area with low power dissipation and moderate operating frequency. Compared to the rest of the possibilities, it gives the highest figure of merit and permits a wide range of temperature and frequencies. BFL, CCDL, TTDL, and DPTL are not suitable for VLSI applications because of their high power dissipation.

VI. CONCLUSIONS

Today's high-performance processors can no longer be based exclusively on speed but must also be based on low power dissipation. PDLL structures have been created in order to offer a good area-power-delay tradeoff by taking benefits of both static and dynamic GaAs logic families, allowing the implementation of VLSI circuits working in a wide range of frequency and temperature. Its ability to be fully compatible with other low-power static gates together with its self-latching characteristic permits the implementation of high-performance VLSI architectures where the sequential part is constructed based on PDLL while the rest can be a mix of DCFL/SBFL gates. Different examples of primitives for data-path structures and processor cores have been presented, solving the lack of complex static gates and exploring new avenues in the implementation of advanced GaAs systems.

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