CICC showcases first-published innovative analog and digital circuit techniques covering a broad spectrum of technical topics.

**Wireless Designs**: circuits for cellular, connectivity, broadband, ultra low power...

**Wired Communications**: high speed electrical and optical, LAN, WAN, Ethernet, SONET, SerDes, modems, broadband, PLLs, DLLs...

**Analog Design**: amplifiers, filters, converters...

**Signal and Data Processing**: image compression; speech recognition; multimedia; graphics; encryption & error correction; bioinformatics...

**Manufacturing and Test**: advanced processing and packaging, reliability & failure analysis, test infrastructure IP, at-speed test, RF & GHz characterization and standards...

**Digital Circuits, SoC/ASIC/SIP Design and Methodology**: complex practical examples and case studies...

**Sensors, MEMs, and Emerging Technologies**: biomedical, imaging, carbon nanotubes, displays...

**Custom Applications and Power Management**: solar energy harvesting, wireless power transmission, biomedical circuits...

**Simulation and Modeling**: Analog, RF, mixed-signal...

**Programmable Devices**: FPGAs, programmable I/Os...

**Embedded Memory**: scalability, GHz speed, low leakage...

*Technical Education* on new, state-of-the-art developments is the core of CICC. *Over 160 papers*, addressing a broad range of circuits, applications, design techniques, tools, test, reliability, and system-on-a-chip. *Awards for Best Paper* will be given for regular, invited, student, and poster submission categories. Top-rated CICC papers are eligible to be considered for the IEEE Journal of Solid State Circuits.

*Sept 16 Educational Sessions*: three in-depth, full-day tutorials instructed by recognized invited speakers.

- High Speed Serial IO Design Techniques
- Mixed Signal SOC Design Methodology
- Sub 1-Volt Analog Converter Design

An opening Keynote address, Exhibits, interactive Poster-papers and Demonstrations, lively and controversial *Panel Discussions*, and a Luncheon with guest speaker rounds out the program.

The *DoubleTree Hotel Conference Center* is minutes from SJC airport. San Jose offers easy access to many California destinations such as San Francisco, the Monterey peninsula on the Pacific, Wine Country, and Yosemite National Park.
**Programmable Devices:** Logic block, routing fabric, system architecture, and circuit design for FPGAs, PLDs, and structured arrays. Programmable I/O structures, configurable cores, interaction between configurable logic and processors/memories/fix-function cores. Programmable analog architectures. CAD tools targeting these devices. Power efficient architecture, power modeling and optimization for programmable devices. Architecture and CAD for nano-scale FPGAs.

**Analog Circuit Design:** Amplifiers, voltage references and regulators, opamps, sample-and-hold circuits, continuous and discrete-time filters, oversampled and Nyquist-rate data converters, non-linear analog circuits, power supply management ICs, mixed analog/digital IC applications. Analog circuits for sensor interfaces.

**Custom Applications and Power Management:** Analog and digital circuit design emphasizing energy scavenging and power harvesting techniques, solar power, wireless power transmission, RF MEMS, biomedical sensors, micro and nanofluidics chips, and high temperature circuits. Innovative circuits for automotive, biomedical, robotics, and specialized custom and industrial products. Advanced sensor circuits, regulators, IOs, and DC-DC converters.

**Digital Circuits, SoC/ASIC/SiP Design and Methodology:** Solutions to today’s complex digital and mixed-signal design problems, in particular practical examples and case studies involved with system level design using SoC/ASICs/SiPs (“how we did it”). Multiple power domains with multi-threshold and power shutoff, managing multiple clock to clock domains, managing noise or bridging the digital to analog chasm. In addition, hardware/software tradeoffs, co-design and co-verification, signal integrity challenges and optimizations of all the above including DFM.

**Embedded Memory:** Memory circuits, architectures, and methodologies addressing scalability, GHz performance, manufacturability, reliability, and the advancement of emerging memory technologies. Also of interest are redundancy, BIST, SER, cell stability, and low voltage/leakage design.

**Manufacturing and Test:** Advanced manufacturing techniques using any combination of bulk/SOI CMOS, bipolar, non-silicon, and optoelectronics technologies. Special focus on challenges of and alternatives to CMOS scaling. Evolving chip packaging such as chip stacking, lead-free, flip-chip, and System-in-Package. Design for manufacturability/test/reliability, built-in self-test for IC and system, low-cost techniques, design for at-speed test, RF characterization and production test, jitter and high-speed SerDes standards, IEEE 1149.6 boundary scan, hardware and firmware silicon debug and diagnosis, new reliability and failure mechanisms in nanometer technologies, ESD protection, latch-up and soft errors. Tutorial papers on the design impact of process-technology selection or packaging and high-speed serial I/O testing are encouraged.

**Signal and Data Processing:** General purpose, application specific and configurable data processing architectures, circuits and systems. Digital signal processing for communications and data storage; image processing; speech recognition; multimedia and graphics; encryption and error correction. Special purpose architectures and circuits for novel data processing applications. Digital implementation of previously analog functions.

**Simulation and Modeling:** Compact active and passive device models, behavioral modeling, and signal integrity modeling and simulation. System, circuit, functional, timing and logic modeling and simulation. Parasitic extraction and reduction; simulation techniques for analog, RF, and mixed-signal circuits. Package modeling, process variation and statistical modeling.

**Wired Communications:** Circuits and systems for electrical and optical networks, including; peripheral IO buses, LAN, WAN, Ethernet, SONET, xDSL, SATA, HDMI, PCIe, USB, cable modems, power-line/phone-line home networks, serial links, backbone, high-speed memory and graphic interfaces, chip-to-chip interconnects, on-chip clocking and high-speed low-power blocks for broadband applications. Circuit blocks including Serializers/Deserializers, Equalizers, PLLs, DLLs, CDRs, Drivers and Amplifiers.

**Wireless Designs:** Integrated wireless transceiver architectures and sub-circuits for cellular, connectivity, broadband and millimeter-wave communication, low-power and biomedical, smart antennas and MIMO, software-defined radio. Papers on RF circuit solutions targeting emerging wireless applications and techniques are particularly encouraged.
Submission of Papers

Paper Submission Deadline is April 9, 2007

Papers must report original and previously unpublished work, including specific results. Papers may be up to 4 pages in length including illustrations, charts, tables and references. Successful submissions concisely explain how the work advances the state of the art and include schematics, measured results, and technical detail sufficient to be understood. **Circuit-design papers intended for traditional lecture presentation must include measured experimental results that substantiate performance claims.** Circuit-design papers using only simulation to substantiate performance claims are usually rejected for traditional lecture presentation, but may be considered for poster presentation.

Papers are submitted electronically. **Prior to preparing your paper for electronic submission, please read the paper preparation and submission guidelines on the CICC website (www.ieee-cicc.org).** The submission instructions will be available by February 16. The submission page will be active beginning March 9.

When submitting a paper, please indicate a preference for **traditional lecture** or **poster presentation**, although CICC may assign presentations to either category.

Appropriate company and government clearances MUST be obtained prior to submission. Authors of accepted papers will be notified by email by June 8, 2007.

**ACCEPTED PAPERS WILL BE PRINTED IN THE PROCEEDINGS WITHOUT OPPORTUNITY FOR FURTHER CHANGE.**

Accepted papers will be used for publicity purposes and portions of these papers may be quoted in pre-conference magazine articles and also via the Web. If this is not acceptable, authors must email CICC at cicc@his.com to decline publicity.

**Papers for Poster Presentation**

Poster presentations encourage in-depth discussions with the audience and are ideal for the presentation of ongoing research. The Poster Session will be held in an extended informal setting accompanied by food, inviting all CICC attendees to engage in discussions with authors. The acceptance criteria for papers for poster presentation are identical to those for traditional lecture presentation except that the requirement for measured experimental results may be relaxed for papers intended for poster presentation.

**Tutorial Papers**

Tutorial papers may be up to 8 pages. Those interested in submitting a tutorial paper must contact the Technical Program Chair, David Nairn (nairn@ecemail.uwaterloo.ca) in advance. This should be as soon as possible, as the number of tutorial slots is limited.

**Poster Session Demonstrations**

Lecture or poster presenters may apply to present a demonstration of their research. Visit the CICC website for additional details.

Visit our web site at www.ieee-cicc.org
for complete instructions on submitting a paper, registration information, and general inquiries.

Or you can contact the Conference Office:  IEEE Custom Integrated Circuits Conference, 16220 South Frederick Road, Suite 312, Gaithersburg, MD, 20877, Telephone: 301/527-0900 x101, Fax: 301/527-0994, email: cicc@his.com,