Abstract: This paper considers the implementation of a digital receiver suitable for a Transmit/Receive (T/R) module in phased array radars. In particular, the achievable SNR performance of an L-band RF sub-sampling receiver will be investigated as a function of the Analogue to Digital Converter (ADC) sample rate. The SNR is measured per unit bandwidth, as it is assumed that the ADC is followed by a digital filter which limits the spectrum to the desired signal bandwidth. The SNR performance of a direct RF sub-sampling receiver is also compared against a single-conversion receiver using a mixer stage prior to ADC conversion.

1. Introduction
Reducing the size and cost of digital receivers allows more digital T/R modules to be used in a phased array, which results in smaller analog sub-arrays and improved overall system performance. One way of potentially reducing the size and cost of digital receivers is to digitize earlier in the RF chain, thus removing analogue components otherwise required for frequency conversion. In the extreme case the signal could be digitized directly at the antenna, which will be termed RF sub-sampling in this paper. However, sampling the signal directly at the antenna also introduces other problems such as less selectivity, and a higher sensitivity to phase noise, which will limit the maximum dynamic range achievable by the receiver.

Several experimental systems have been built to implement and test RF sampling receivers [1],[2], which demonstrate the feasibility of this approach. This paper investigates the achievable system dynamic range of such a system in more detail. Dynamic range will be defined as the maximum achievable signal to noise power ratio (SNR), where the noise power is defined to be the total noise power in the signal bandwidth. The dynamic range of the direct RF receiver will be compared with a receiver architecture that uses a single mixer stage.

The main factors limiting the SNR that will be considered include: jitter on the sampling clocks, phase noise on the local oscillator, noise in the ADC converter and jitter in the ADC sample and hold circuit. Harmonic distortion also potentially limits the dynamic range, but has not been considered in this paper. Basic models will be developed to estimate the dynamic range of the combined receiver as a function of the ADC sample rate and basic parameters of the critical components.

2. Receiver Model
To focus the results in the paper, a radar system with a carrier frequency of 1.5 GHz will be considered. Two basic system architectures will be considered: Direct RF sampling and a single IF mixer stage. The direct RF sampling architecture samples the signal directly at L-band as shown in Figure 1. The band-pass filter will limit the signal spectra to lie within one of the Nyquist zones of the ADC. The signal is then aliased to the first Nyquist zone by sub-sampling. After A/D conversion, the signal is band-limited to the signal bandwidth with a digital decimation filter.
The dynamic range limit imposed by the main components in figure 1 will be considered including the ADC, Sampling clock, Sample/Hold and mixer (for the single IF receiver).

3. ADC Converter Resolution
The best achievable ADC resolution depends on its power consumption and sample rate. A useful figure of merit (FOM) that relates all three variables is [3]:

\[
FOM = \frac{P}{2^{\text{ENOB}} f_s}
\]

Where \(P\) is the power consumption of the ADC, \(\text{ENOB}\) are the effective number of bits in the ADC and \(f_s\) is the ADC sampling rate. The above FOM has units of Joules per conversion and a smaller number indicates a higher performance ADC. Current state of art ADC converters achieve a FOM of around 4 pJ/conversion, although for sample rates below 100 MHz a FOM below 1 has been achieved [4]. Most ADCs that met the 4 pJ/Conversion FOM have a power consumption under 1W. In the remainder of this paper, an ADC with a FOM of 4 pJ/Conversion and a power consumption of \(P = 1\)W will be assumed. The SNR in a signal bandwidth of \(B\) Hz is thus given by:

\[
\text{SNR}_{\text{ADC}} = 20\log_{10}\left(\frac{1}{\text{FOM}}\right) + 1.76 - 20\log_{10}(f_s) + 10\log_{10}(f_s/2B)
\]

4. Sampling Clock Phase Noise
The phase noise on the sampling clock is modulated onto the incoming signal after being amplified by the sub-sampling factor, thus the dynamic range of the receiver will be limited by the SNR of the sampling clock signal according to [5]:

\[
\text{SNR}_{\text{clock}} = \left(\frac{f_s}{f_a}\right)^2 \text{SNR}_{\text{clk}}
\]

Where \(f_a\) is the input frequency to the ADC and \(\text{SNR}_{\text{clk}}\) is the SNR of the sampling clock. The noise power on the clock signal is integrated over the entire encode bandwidth of the ADC, which can be several GHz. In this paper an encode bandwidth of 2 GHz will be assumed.

The sampling clock is assumed to be derived from a crystal oscillator, and it will be assumed that the wide-band noise floor is the dominant noise source. For fundamental crystal oscillators (typically ranging up to 100 MHz), the achievable wideband noise floor tends to be independent of the crystal frequency and is around \(-180\) dBc/Hz for a very high quality source [6]. For higher sampling frequencies the crystal oscillator would need to be multiplied, which increases the phase noise by \(20\log(N)\), where \(N\) is the multiplication factor. Higher clock frequencies can also be achieved by phase-locking a Voltage Controlled Oscillator (VCO) to a crystal oscillator, in which case the broadband noise floor is established by the VCO. However, VCOs operating above 1 GHz tend to have noise floors above \(-160\) dBc/Hz [6], which is similar to that obtained by multiplying up a crystal reference. Thus it will be assumed that the phase noise floor of the oscillator is approximated by: \(-180 + 20\log(f_s/100\text{MHz})\), where \(f_s\) is the oscillator frequency, and the overall SNR of the clock signal is given...
by: \( \text{SNR}_{\text{clk}} = 180 - 10 \log_{10}(2 \times 10^6) - 20 \log_{10}\left(\frac{f_s}{100 \times 10^6}\right) \), assuming a 2 GHz encode bandwidth.

The SNR limitation imposed on the sampled signal by the phase noise of the sampling clock is thus given by:

\[
\text{SNR}_{\text{signal}} = 20 \log_{10}\left(\frac{f_s}{f_s}\right) + 247 - 20 \log_{10}(f_s) + 10 \log_{10}\left(\frac{f_s}{2B}\right)
\]

\[
= 247 - 20 \log_{10}(f_s) + 10 \log_{10}\left(\frac{f_s}{2B}\right)
\]

5. Sample/Hold Circuit Jitter

The sample-hold circuit will degrade the SNR by introducing timing jitter. This will essentially modulate broadband noise onto the signal. The SNR of the sampled signal is related to the standard deviation of the sample-hold jitter \( \sigma_t \), according to [7]:

\[
\text{SNR}_{\text{signal}} = -20 \log_{10}(2\pi \sigma_t f_{\text{s}}),
\]

thus the dynamic range of the signal is given by:

\[
\text{SNR}_{\text{signal}} = -20 \log_{10}(2\pi \sigma_t f_{\text{s}}) + 10 \log_{10}\left(\frac{f_{\text{s}}}{f_{\text{THz}}}\right)
\]

Recent ADC converters have achieve jitter figures below 1 ps RMS. The TS83102G0B ADC has an RMS aperture jitter of 200 fs, and an input bandwidth of 3.3 GHz. Two dedicated sample and hold chips from Rockwell, the RTH010 and RTH050 have an input bandwidth of 9 GHz and 15 GHz respectively and an RMS aperture jitter of less than 100 fs. Thus an aperture jitter of 100 fs RMS will be assumed in this paper.

6. Mixer

The single IF receiver uses a single mixer stage. The dynamic range of the mixer will be limited by the phase noise on the local oscillator, which is modulated onto the incoming signal. Harmonic distortion products will also potentially limit the dynamic range, but are not considered in this paper. The phase noise on the local oscillator will be modelled in the same way as the sampling clock. The key differences are that in this case the sub-sampling factor is unity and the noise bandwidth is equal to the signal-bandwidth, rather than the encode bandwidth of the ADC. Thus:

\[
\text{SNR}_{\text{signal}} = 180 - 10 \log_{10}(B) - 20 \log_{10}\left(\frac{f_{\text{LO}}}{100 \times 10^6}\right)
\]

6. Combined Receiver Performance

This section compares the overall SNR achievable in direct conversion and single conversion receivers using the basic models introduced in the previous sections for current state-of-art receiver components. The SNR limitation due to each of the main receiver building blocks is shown in Figure 2 along with the overall SNR limitation for both the direct RF sampling and single IF receiver. The results in this figure assume a signal bandwidth of 50 MHz, and an IF frequency of 75 MHz in the single stage IF receiver.

Figure 2 indicates that a single mixer stage can still achieve a significantly higher dynamic range than direct RF sampling. In the single IF receiver, the ADC limits the dynamic range, while for the direct RF receiver, the Sample/Hold jitter and clock phase noise will begin to limit the dynamic range at lower ADC sample rates. The maximum SNR of the direct RF sampling receiver is achieved at sample rates around 500 MHz. The dynamic range for larger bandwidths were also considered, and there was found to be minimal difference in dynamic range for bandwidths above 250 MHz.
There are a number of additional factors that need to be considered when choosing the ADC sample rate in a direct RF sampling receiver. Increasing the ADC sample rate will increase the computational load of the digital decimation filter increasing power consumption, while lowering the ADC sampling rates introduces significant design challenges, as it is very difficult to achieve low jitter in the Sample/Hold circuits with a low frequency clock signal, due to the low clock slew rates.

**Figure 2: Dynamic Range Limitation for Direct RF and single IF Receiver**

### 7. Conclusion

This paper has considered the dynamic range limitation imposed on an L-band receiver by clock phase noise and the ADC. Both direct RF sampling and single IF receivers were considered. Based on current state of art components, it was found that a single IF stage is still useful for increasing the SNR of the receiver for bandwidths of 50 MHz. As the signal bandwidth increases a higher ADC sample rate and IF frequency are required in the single IF receiver and its dynamic range approaches that of the direct-RF sampling receiver.

### Reference: