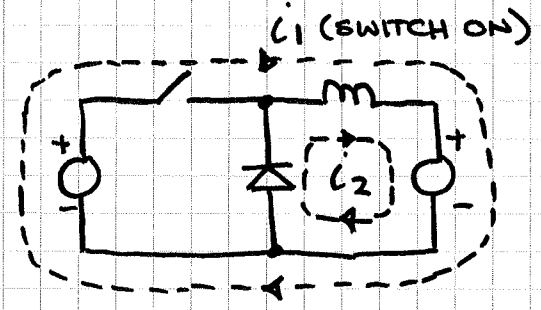
12R002 - MINIMISING STRAY INDUCTANCE

19-JAN-12

SUMMARY - WHEN DESIGNING POWER ELECTRONIC CIRCUITS IT IS IMPORTANT TO MINIMISE STRAY INDUCTANCE TO PREVENT OVER-VOLTAGES DAMAGING SWITCHES

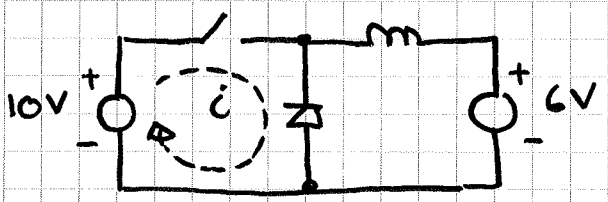
1. EXAMPLE CIRCUIT



THERE ARE TWO CURRENT PATHS DEPENDING ON THE STATE OF THE SWITCH:

SWITCH ON → i_1
SWITCH OFF → i_2

THE ISSUE IS THAT THE CURRENT CHANGES RAPIDLY IN THE LEFT VOLTAGE SOURCE, SWITCH AND DIODE.



NEED TO MINIMISE THE INDUCTANCE IN THIS LOOP TO AVOID LARGE INDUCED VOLTAGES IN THE "STRAY" INDUCTANCE.

$$v(t) = L \cdot \frac{di(t)}{dt}$$

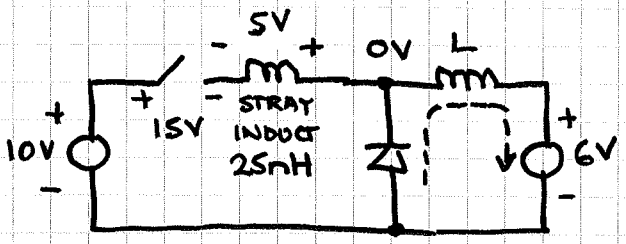
FOR EXAMPLE A MOSFET SWITCHES IN SAY 100nS. CONSIDER A CURRENT OF 20A. THIS IS A

$$\frac{di}{dt} = \frac{\Delta i}{\Delta t} = \frac{20A}{100nS} = 200\,A/\mu S$$

ASSUME AN ALLOWABLE (induced) VOLTAGE OF 5V

THIS GIVES MAX (allowable) STRAY INDUCTANCE:

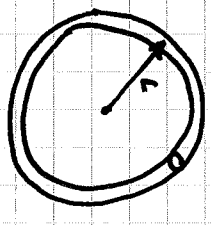
$$L_{MAX} = \frac{5V}{200A/\mu S} = 25nH$$



THE LARGER THE STRAY INDUCTANCE, THE LARGER THE VOLTAGE THE SWITCH SEES WHEN IT IS TRYING TO TURN-OFF → too large, will destroy switch

2. EXAMPLE INDUCTANCES

2.1 CIRCULAR LOOP



r = radius of loop
a = radius of conductor

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$$L \doteq r\mu_0\mu_r\left[\ln\left(\frac{8r}{a}\right) - 2\right]$$

E.G. $r = 5cm$, $a = 0.1cm$, $\mu_R = 1$

$$L = 0.05 \times 4\pi \times 10^{-7}\left[\ln\left(\frac{8 \times 0.05}{0.001}\right) - 2\right]$$

$$= \underline{251nH}$$

reducing $r = 1cm \Rightarrow L = \underline{30nH}$

using $r = 1cm$, $a = 0.05cm$
$\Rightarrow L = \underline{39nH}$

lowest inductance with:

- small loop (primary factor)
- thick wires (secondary factor)

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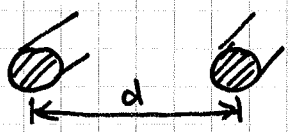
2.2. TWO PARALLEL CIRCULAR WIRES

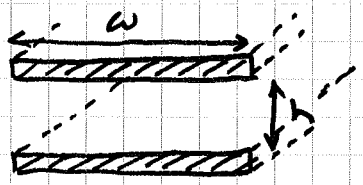


inductance $L = \frac{\mu_0}{\pi} \ln \frac{d-a}{a}$

use $d = 2cm$, $a = 0.1cm$

$L = 1.2\mu H/m$ or $12nH/cm$

2.3 TWO PARALLEL PLATES



$L = \mu_0 \cdot \frac{h}{w}$

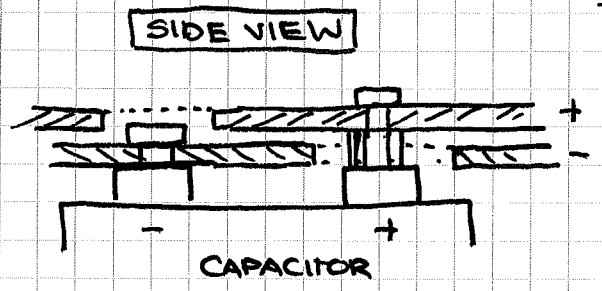
for $h = 2cm$ $w = 2cm$

$L = 1.3\mu H/m$ or $13nH/cm$

but if can place plates close together e.g. reduce h from 2cm to 0.1cm

$L = 63nH/m$ or $0.63nH/cm$

thus high power rating units in power electronics normally use "bus bars" - two wide copper strips with a thin insulating layer between

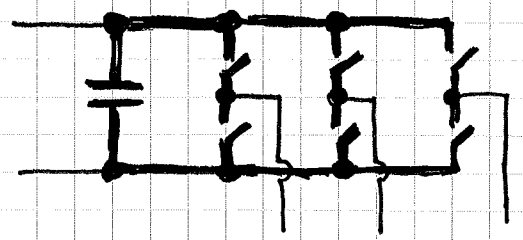


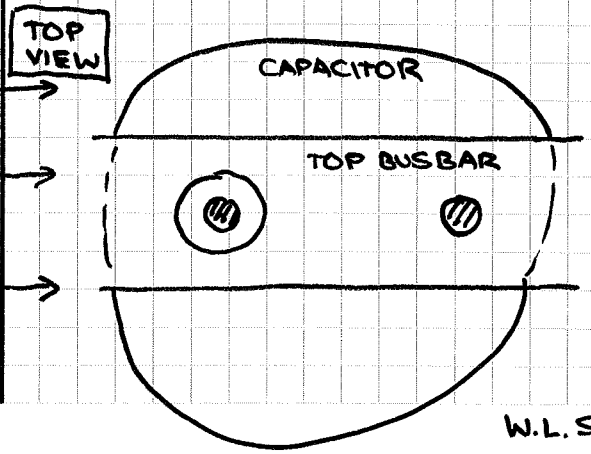
3. DESIGN PRINCIPLES

- minimise the physical size of the loop in the circuit where the current changes rapidly
- use larger conductors, preferably flat plates with only a small gap between them
- can reduce effects of stray inductance by slowing down the switch turn-off and on times but this will increase switching losses
- the higher the current and the faster the switching time, the more careful one needs to be

4. KEY CIRCUIT LOOPS

for a 3ph inverter, it is important to minimize the stray inductance in the loop shown below in bold





"GOD HAS PLACED ETERNITY IN THE HEARTS OF MEN"

W.L. SOONG