12R013 - DEBUGGING GATE DRIVERS

28-FEB-12

Aim - suggestions for testing inverters and fault finding issues with gate drivers

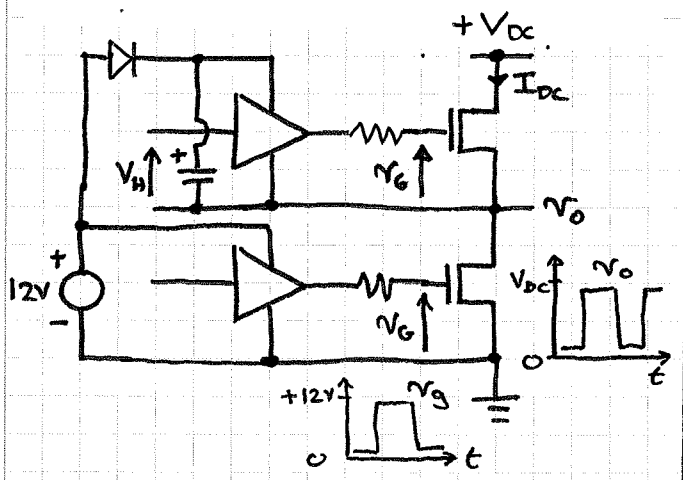
1. NO-LOAD TESTING

Set-up the following:

- disconnect load from inverter output (zero output current)
- power dc link from a low-voltage power supply e.g. 10V, with a current limit set to a low value compared to the switch ratings e.g. 1A
- drive phase legs with a fixed duty-cycle, e.g. 50% in the range 20-80%

Examine the following:

a) phase-leg output voltage v_o
b) low-side gate drive signal
c) high-side capacitor and gate drive signal (need to use a differential probe as signals are referenced to output voltage)
d) dc link current I_{DC}



the phase-leg output voltage v_o should swing within a volt or two of ground and $+V_{DC}$

the gate drive signals should have a maximum of say 10V or more and a minimum value of less than 1V

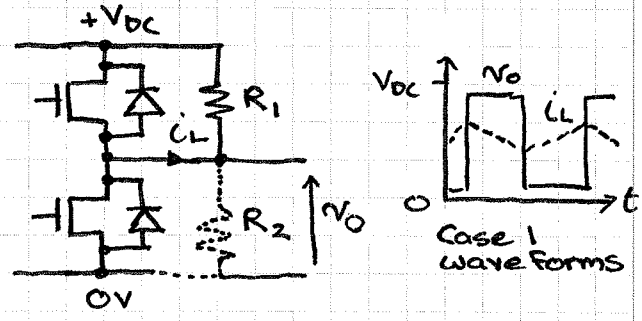
the transition times for the gate drive signals should be less than 1μs

the high-side gate drive bootstrap supply should be at least 10V

the dc link current should be small, e.g. average <0.1A

2. RESISTIVE LOAD TESTING

The next step is to test the phase-leg with a resistive load in two configurations.



Case 1: only R_1, remove R_2
- this tests the low-side switch and the high-side diode

Case 2: only R_2, remove R_1
- this tests the high-side switch and the low-side diode

preferably
the resistors should be large wire-wound variable resistors as these have significant stray inductance

choose a large enough resistor value to limit the switch current to a low value, e.g. 1A and ensure the dc link power supply is also current limited to an appropriate safe value e.g. 2A

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