Fat-tree Network on Chip Implementation Using Rotary Routers

Author: Aidan Foord
Supervisors: Assoc. Prof. Michael Liebelt
Cruz Izu

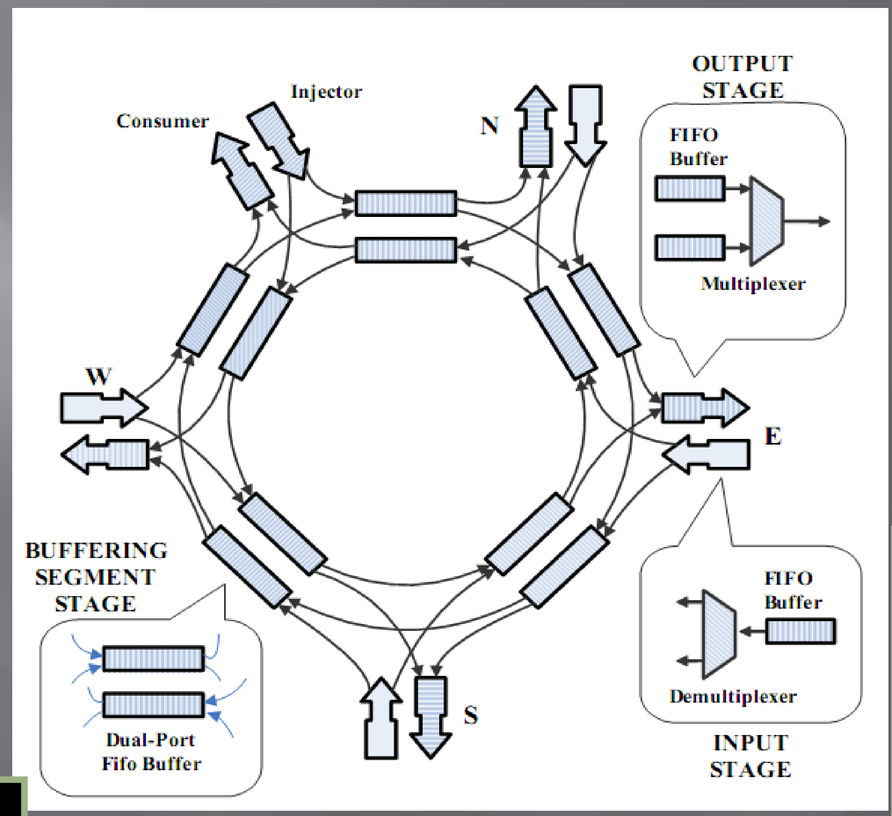
SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING
THE UNIVERSITY of ADELAIDE

Background

The aim of the rotary router is to improve the overall throughput of Network on Chips used in multi-core processors.

Significance

The Project looks to overcome the bottleneck that is experienced in multi-core processors. Using rotary routers as a Network on Chip to transfer information from memory to computer processors.



Aims

The aims of the project are:

- To design a rotary router using verilog
- To synthesize the rotary router onto a FPGA board
- To test the rotary router against the crossbar switch

Outcomes

The rotary router still needs to be finished. This involves completing the signals with in the rotary router that control how it works.

verilog

```
module EightBit_Counter(
output [0:1] Q,
input [0:1] D,
input ce,
input reset,
input clk);

reg [0:1] q;

always @ (posedge clk)
if (reset)
q = 2'b00;
else if (ce)
q <= D + 1;
else
q = D;

assign Q = q;

endmodule
```

Test bench

```
module EighBit_Counter_tb();
 reg ce, reset, clk;
reg [0:1] D;
wire [0:1] Q;

EightBit_Counter dut(Q, D, ce, reset, clk);
 initial begin
clk = 1'b0; ce = 1'b0; reset = 1'b0; D = 2'b00; #10;
if (Q!= 2'b00) $display("set up is wrong");
D = Q; ce = 1'b1; reset = 1'b0; #10;
if (Q!= 2'b01) $display("wrong 1");
D = Q; ce = 1'b1; reset = 1'b0; #10;
if (Q!= 2'b10) $display("wrong 2");
D = Q; ce = 1'b1; reset = 1'b1; #10;
if (Q!= 2'b00) $display("wrong reset");
end
always begin
#5 clk = ~clk;
end
 endmodule
```

Components

For the rotary router to be built it required a number of components to be designed in verilog.
These were:

- Multiplexer and De-multiplexer
- FIFO Buffer
  - Counter
  - SSRAM

References

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